A 3.1~10.6 GHz CMOS Cascaded Two-stage Distributed Amplifier for Ultra-Wideband Application

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ABSTRACT

In this paper, a CMOS cascaded two-stage distributed amplifier for ultra-wideband (UWB) application is presented. The circuit using two-stage cascaded topology achieves better gain-bandwidth product performance than conventional CMOS distributed amplifiers. The simulated gain is 18dB with ±1dB gain flatness over 3.1~10.6 GHz bands. Input and output are matched to 50Ω, and the return losses of input and output are below -10dB and -9dB respectively. The power dissipation is 54mW with 1.8V power supply. The circuit was fabricated in 0.18-μm 1P6M RF CMOS process.

I. INTRODUCTION

UWB is an emerging technology for wireless communication. Unlike narrow-band system, UWB has capability for high data rate communication applications, such as imaging systems, vehicular radar systems, and ground penetrating [1]. Although the standard of UWB has not been finalized, many proposed researches target at the band between 3.1 and 10.6 GHz. In this work, the design goal is to achieve an amplifier with gain of 18dB over 3.1 to 10.6 GHz [12].

Distributed amplification, characterized by wide bandwidth, has been prevalent over sixty years. Lots of distributed amplifiers are fabricated on the compound semiconductor processes for applications of mini-meter wave. However, the CMOS technology is less expensive than compound semiconductor processes and has higher potential for integration with the digital part, especially for silicon-on-chip solutions. Researches on the CMOS distributed amplifiers have made considerable progress in the recent years.

Of these researches, one accomplished a gain of 5 ± 1.2dB from 300 kHz to 3 GHz, and 4.7 GHz unity-gain cutoff frequency [2]. In another work, a 0.5 to 8.5 GHz CMOS fully differential distributed amplifier was realized with a gain of 5.5 ± 1.5dB in a 0.6-μm CMOS process [4]. Lastly, a 0.5 to 14 GHz with 10.6 ± 0.9dB gain and a 0.6 to 22 GHz with 7.3 ± 0.8dB gain distributed amplifier using 0.18-μm CMOS RF process were proposed [7]-[8]. Among these, amplifier's gain does not exceed 10.6dB, which is not high enough for advance applications, such as UWB system. The cascaded single-stage distributed amplifier (CSDA) topology was brought out for increasing the amplifier's gain [6]. In that work, the CSDA has 21dB gain and 5 GHz bandwidth but the CSDA needs more complicated dc-wise setup than conventional distributed amplifiers.

In this paper, a cascaded two-stage distributed amplifier (CTDA) is proposed, and it possesses the high gain property of CSDA without complicate dc-wise setup. This paper is organized as follows. Some basics of the conventional distributed amplifier design are described in Section II. Section III covers the topology of CTDA and some comparisons between the conventional distributed amplifier, CSDA and CTDA. Section IV shows the simulation results, and conclusions are given in section V.

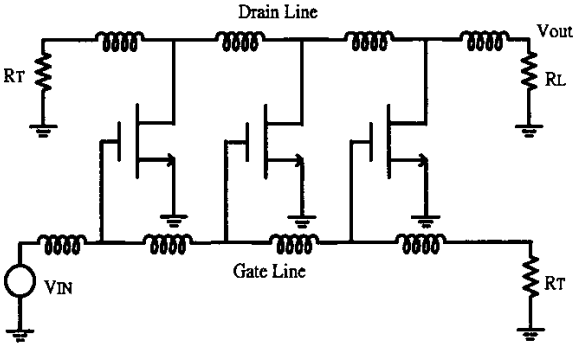

Fig. 1 Conventional distributed amplifier

II. BASICS OF DISTRIBUTED AMPLIFIER DESIGN

Distributed amplifiers employ the topology that several gain stages are in parallel and series-inductors are introduced to separate capacitances of the input and output node of adjacent gain stages. This topology builds two artificial transmission lines, gate line and drain line. Output current is combined additively by the current flowing from each gain stage. The additive characteristic results in a relatively low gain, while the distributed nature of capacitance can achieve very wide bandwidth. Fig. 1 shows a three-stage conventional distributed amplifier. Design equations can be referred to [10], [11]. The voltage gain can be written as [11]:

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$$A_V = -\frac{g_m}{2\sqrt{1-(\omega/\omega_c)^2}}\sqrt{\frac{L}{C}}e^{-\frac{N}{2}(\theta_d+\theta_g)}\frac{\sinh N\frac{(\theta_d-\theta_g)}{2}}{\sinh\frac{(\theta_d-\theta_g)}{2}} \quad (1)$$

where

N	number of stages;
g_m	gain stage transconductance;
ω_c	cutoff frequency of transmission lines;
θ_g	propagation constant of gate line;
θ_d	propagation constant of drain line;

The cutoff frequency (ω_c) of transmission line is $2/\sqrt{LC}$. It can be derived that voltage gain becomes maximum when $\theta_g = \theta_d$, as shown in Fig. 2. The more the propagation constant of the gate line differs from that of drain line, the more the amplifier gain decays.

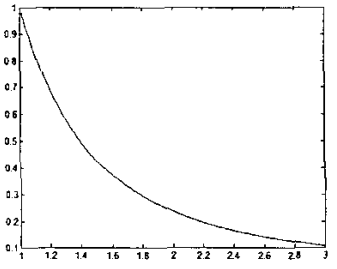

Fig. 2 Normalized gain vs. Ratio of θ_g and θ_d

When $\theta_g = \theta_d$, the equation of voltage gain can be simplified as:

$$A_V = -\frac{N \cdot g_m}{2\sqrt{1-(\omega/\omega_c)^2}}\sqrt{\frac{L}{C}}e^{-N\theta} \quad (2)$$

Intuitively, the voltage gain can be enhanced when large N is selected. Because the transmission lines are not ideal, some parasitic effects such as spiral inductor parasitic resistance make the propagation constant not purely imaginary, which leads to path loss. The voltage gain is not proportional to the number of stages anymore but achieves a maximum when the optimal value of N is used. The equation of optimal N is written as [11]:

$$N_{opt} = \frac{\ln\frac{\theta_{rd}}{\theta_{rg}}}{\theta_{rd}-\theta_{rg}} \quad (3)$$

where

θ_{rg}	real part of propagation constant of gate line;
θ_{rd}	real part of propagation constant of drain line;

For CMOS process, the N_{opt} is between 3 to 5. This is one of the substantial reasons that distributed amplifier gain can not be large.

In [6], the CSDA is proposed to enhance its gain. Assuming all the load resistance of each gain stage are the same, the equation of gain is:

$$A_V = \left(\frac{1}{2}g_m \cdot R_O\right)^N \quad (4)$$

where

N	number of stages cascaded;
g_m	gain stage transconductance;
R_O	output resistance of each stage;

This is a novel approach to increase the gain of the amplifier. The gain grows in proportional to the power of N. However, if the gain of each stage ($g_m \cdot R_O/2$) is not large, the amplifier gain can not grow very fast. In addition, extra components such as RF chock may be needed to setup dc operating voltage at each inter-connected node.

Therefore, we propose the cascaded two-stage distributed amplifier (CTDA) to solve these problems. Next session discusses the CTDA circuit topology.

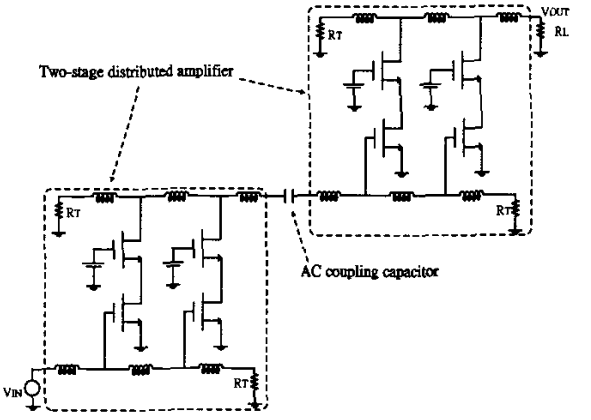

Fig. 3 Cascaded two-stage distributed amplifier

III. CTDA Topology and Gain Enhancement

The CTDA circuit topology is shown in Fig. 3. It could be regarded as two conventional two-stage distributed amplifiers cascaded. AC coupling capacitor is used for connecting these two conventional distributed amplifiers and DC setup can be accomplished in the same way as that of conventional distributed amplifier. The cascode gain cell configuration is used for its high maximum available gain, better input-output isolation, and high output impedance [8]. The gain of CTDA can be written as:

$$A_V = \left(\frac{1}{2}\cdot 2 \cdot g_m \cdot R_O\right)^N \quad (5)$$

where

N	number of two-stage distributed amplifier cascaded;

Assuming conventional distributed amplifier, CSDA and CTDA are all composed of four gain stages, the demanded transconductance per gain stage can be plotted respectively in different required gain, as shown in Fig. 4. When required gain is between 12dB~24dB, the transconductance of CTDA is the smallest among three of them. Power dissipation of the circuit is usually in proportion to the needed transconductance per gain-stage, so CTDA consumes the least power.

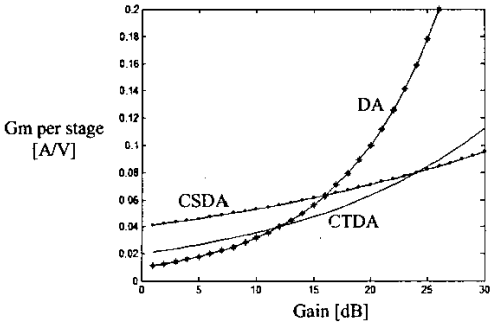

Fig. 4 Transconductance per stage versus Target gain

IV. Simulation Results

The CMOS CTDA was simulated by Advanced Design System (ADS). Fig. 5 and Fig. 6 show the S-parameters and the noise figure of the CTDA. The gain (S_{21}) is 18dB with 1.2dB ripple from 3.1 GHz to 10.6 GHz. The input and output return losses are less than -10dB and -9dB respectively. The reverse isolation S_{12} is 40dB or better over the whole bandwidth. The noise figure is between 5dB and 7dB. Power consumption of the CTDA is only 54mW. Die photo is shown in Fig. 7. Table 1 summarizes the performance of the CTDA. The recently reported performances of CMOS distributed amplifiers compared with this work are summarized in Table 2. This work demonstrates the highest gain-bandwidth production (GBP).

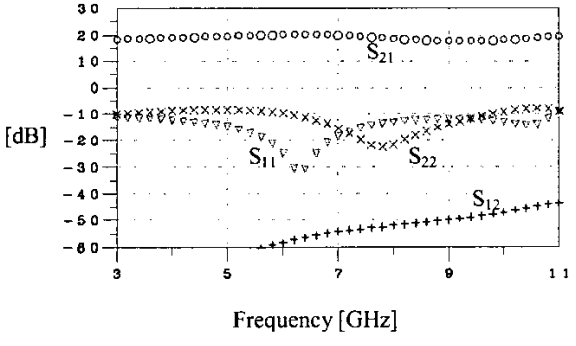

Fig. 5 Simulated S-parameters

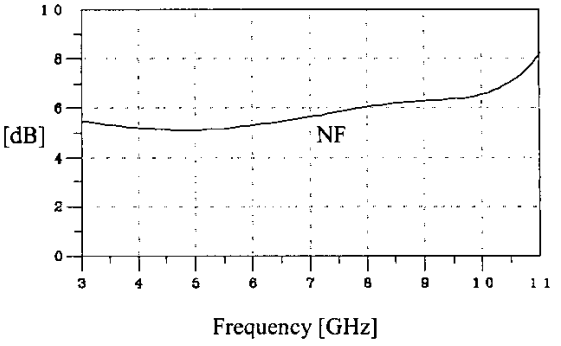

Fig. 6 Simulated Noise figure

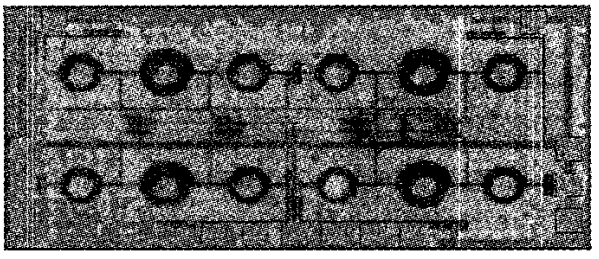

Fig.7 Die photo of CTDA

	Simulation Results
Technology	TSMC 0.18 um
Power Supply	1.8V
Frequency	3.1~10.6 GHz
Gain(S_{21})	18dB (1.2 dB ripple)
Input Return loss(S_{11})	< -10dB
Output Return loss(S_{22})	< -9dB
Isolation(S_{12})	< -40dB
Noise Figure	5~7 dB
Power Consumption	54mW
Area	2.2mm x 1mm

Table 1 Performance summary of CTDA

V. Conclusion

A CMOS cascaded two-stage distributed amplifier has been proposed. The conventional distributed amplifier, CSDA and CTDA have been compared under similar conditions. The CTDA can achieve a voltage gain of 12~24dB using less power consumption than those two. In this work, an 18dB voltage gain CTDA consuming only 54mW has been presented for UWB application. Comparing with other previously published CMOS DAs, this work demonstrates the highest gain-bandwidth production.

Reference	Process	Bandwidth (GHz)	Gain (dB)	GBP (GHz)	S11 (dB)	S22 (dB)	VDD (V)	Power Consumption (mW)
[3]	0.6 μm CMOS	4	6.5	8.5	-7	-10	3	83.4
[4]	0.6 μm CMOS	7.5	5.5	14	-6	-9.5	3	216
[6]	0.35 μm CMOS	5	21	56	-10	-10	2.2	132
[9]	0.18 μm CMOS	10	8	25	-	-	-	-
[7]	0.18 μm CMOS	22	7.3	51	-8	-9	1.3	52
[8]	0.18 μm CMOS	14	10.6	47.4	-11	-12	1.3	52
This work	**0.18 μm CMOS**	**3.1~10.6**	**18**	**84**	**-10**	**-9**	**1.8**	**54**

Table 2 Performances comparison

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