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Design and VLSI Implementation of MPEG Audio Decoder

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Abstract—The paper presents a chip design for MPEG audio decoder, with a new modified scheme. In the modified decoding scheme, the required computations can be reduced into half of the original one, and the storage demand too, i.e., the pseudo-QMF, a polyphase filter bank, only requires 512 words memory for 1024 points. The major operators include one adder-subtractor and one multiplier-accumulator. The chip is achieved by using the structure silicon compiler in the Genesil system, with 0.8-μm C-MOS technology.

Introduction

Data compression technique is an essential task for audio systems, which not only handles enormous amount of data, but also requires the high quality resolution. One of these audio coding techniques, MPEG (Moving Pictures Experts Group), a powerful audio compression standardization, undertakes the standardization of compression techniques for the associated audio [1]. It can significantly reduces the requirements of transmission bandwidth and data storage, but with low distorsion.

Recently, there are some researches for audio decoding system [2], [3]. Although achieved MPEG decoder by programming design method in a single chip, they also suffer from a considerable overheads of computation and control, based on the programmable demands.

In our paper, we design a decoder-chip to complete the decoding processes. According to our approach for simplicity and low-cost design, we take use of the dedicated hardware approach (ASIC), which provides a more efficient VLSI solution. Especially, based on the computation analysis of MPEG decoding algorithm, we can reduce the computation amount of inverse MDCT into one-forth of the original one, which yields half of the computation amount of the total MPEG decoding algorithm. Also, the proposed polyphase decomposition method only requires 512 words memory for 1024 points in inverse pseudo QMF. The proposed pipelined architecture of MPEG decoding algorithm satisfies the real-time requirements, with only one MAC and one adder/subtactor function units.

MPEG Audio Coding

The elementary concepts behind MPEG is achieved by use of the perceptual coding, which exploits the properties of the human ear. Laterly, Subband/Transform coding can be used to get the best performance at a very low bit rate [4].

The basic block diagram for MPEG audio encoder is shown in Figure 1. Main blocks include the analysis filter bank, quantization and coding in the frequency domain, psychoacoustics model and the assembly of output bit stream. The encoder accepts a continuous flow of input audio PCM samples. The analysis filter bank, a polyphase filter bank, also named Pseudo-QMF (Pseudo-Quadrature Mirror Filter) [5], creats a mapping of the audio data into the same number of coefficients (or subsampled samples) in the spectral domain representation, with 32 equal-spaced subbands [6]. At this level, they are scaled and quantized in blocks within the bit-allocation module. The relevant coding parameters are extracted and formatted into an encoded frame.

After the storage and/or the transmission, the

associated decoder recovers the encoded information frame by frame. After the process of the frame unpacking, the decoder performs an inverse quantizing (expansion process), and feeds the subband synthesis filter bank with a set of 32 scaled-up subband samples in order to reconstruct the output PCM audio signals, as shown in Figure 2.

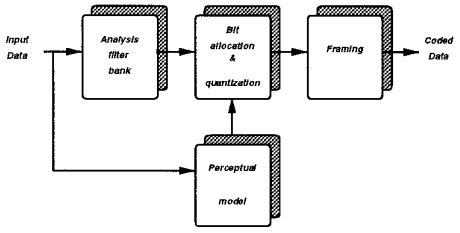

Figure 1: Block Diagram of the Encoder

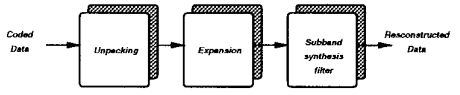

Figure 2: Block Diagram of the Decoder

The Modified Decoding Scheme

Starting from detail analysis about the computation complexity of MPEG decoder, we can improve the system performance by reducing the computation power, and schedule the data flow in order to get a more efficient algorithm. The MPEG decoding flow chart is shown in Figure 3. It includes some function block: decoding of side information, inverse quantization, synthesis subband filter bank, etc. Within the synthesis subband filter bank, the inverse Modified Discrete Cosine Transform (IMDCT), inverse Pseudo Quadrature Mirror Filter (IPQMF) will be realized, as shown in Figure 4.

For audio signal processing applications, one appropriate measure to represent the complexity of a system would be million operations per second (MOPS ,where a operation is defined as data access, store, add, shift, or multiply). Based on this definition, the required signal processing computation amount for various components of MPEG decoder process is illustrated in Table 1.

According to the illustration in Table 1, IMDCT is the most computationally intensive operation. This takes about two-third of the required signal processing computation of the MPEG decoder.

The original inverse MDCT of a sequence $S(k)$, is defined as following:

$$V_i = \sum_{k=0}^{31} \cos[\frac{(16+i)(2k+1)\pi}{64}] * S_k$$

$$i = 0, 1, ...63$$

$$k = 0, 1, ...31$$

Taking the advantage of the symmetric properties:

$$\cos\theta = \cos(2\pi - \theta)$$

The inverse MDCT definition equations can be leaded into a new formula with a reduction of the computation amount. Thus, the enhanced algorithm is listed as following:

$$V_i = \sum_{k=0}^{15} \cos[\frac{(32+i)(2k+1)\pi}{64}] * [S_k + (-1)^i * S_{31-k}]$$

$$i = 0, 1, ...31$$

$$k = 0, 1, ...15$$

This means that the size of summations is reduced from 32 to 16, and the number of summations is also reduced from 64 to 32. As a result, the number of multiplications and additions can be reduded by a factor of 4. That is,

Table 1: Computation Power for MPEG Decoder

Classification Function	Required Processing Power (MOPS)
IQ	0.384
IMDCT	12.288
IPQMF	6.96
Total	19.632

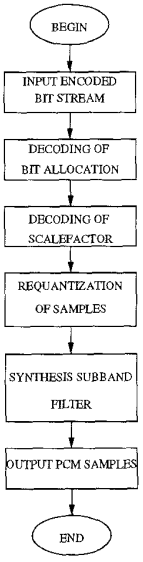

Figure 3: Decoding Flow Chart

the total computation amount for the decoding flow can be reduced into half of the original one. For the same reason, the required size for coefficient ROM can be reduced as a factor of 4. Besides, the required size for the RAM buffer in which the inverse transformed data V is stored can be reduced only to 512 words, instead of the original size of 1024 words. This algorithm is also based on our balance consideration between the high efficiency and simple implementation for VLSI solution.

Architecture Design and VLSI Implementation

Based on our approach for simplicity and low-cost design , dedicated hardware design (ASIC), which offers a more efficient VLSI solution, is provided for our hardware design methodology. Figure 5 describes the overall hardware structure for our proposed design. The data to be processed in the computation unit are held in 4 blocks of memory, as named: ROM0, ROM1, RAM0, RAM1. The ROM0 is stored the coefficients used in the inverse quantization pro-

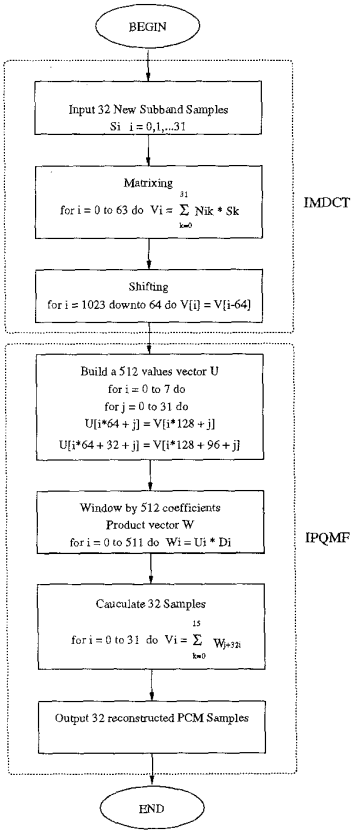

Figure 4: Synthesis Subband Flow Chart

cess. The ROM1 is mainly stored as the 512-word cosine coefficients, and 512-word window coefficients. As a result, it contains above 1 K words. The 32-word RAM0 is a dual-port data memory which can access two data simultaneously. Thus this design can be realized about the butterfly-pair computation of the IMDCT process with a reduced overhead for memory access. The 512-word RAM1 represents as the IMDCT output buffer and also the IPQMF input buffer. All these memory banks are designed as 24 bit word-lenght.

Besides, the proposed architecture can be scheduled as several function blocks. For the controller (CTR), we decide to take use of a

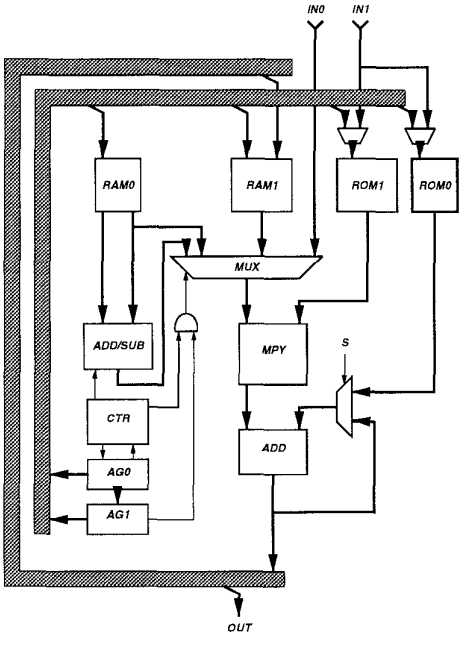

Figure 5: Overall Hardware Structure

hard-wired architecture design for our simple and high efficient approach. Then it doesn't need a program memory and the requirement of some decoding operation, too. Also, in order to enhance the throughput for the system, we take use of the pipeline schedule as a efficiently strategy [7]. For the computation unit, there are only one adder-subtractor (ADD/SUB) and one multiplier-accumulator (MAC) needed in this design. In addition, we design two address generators to supply the memory address, which also reduce the overhead of the controller. Meanwhile, the AG0 (Address Generator 0) provides the memory address for ROM0, ROM1 and RAM0. These address is continuously calculated and broadcasted to these three memory modules. By means of a multiplexer, the correct data would be passed successfully. In order to complete the shifting operations which represent the polyphase decomposition, we design a dedicated address generator to reduce the complexity of the operation. That is, the purpose for the AG1 (Address Generator 1) is to generate the correct memory address for RAM1.

The proposed design is implemented by the GENESIL silicon complier system, as shown in Figure 6. The chip takes use of the 0.8-μm CMOS technology. It consists of 174973 transistors in a size of 7.6 mm x 6.7 mm. The clock rate is 11.5 MHz, or 87 ns per cycle, which can match the requirements of the MPEG decoding flow. The chip specification is listed in Table 2.

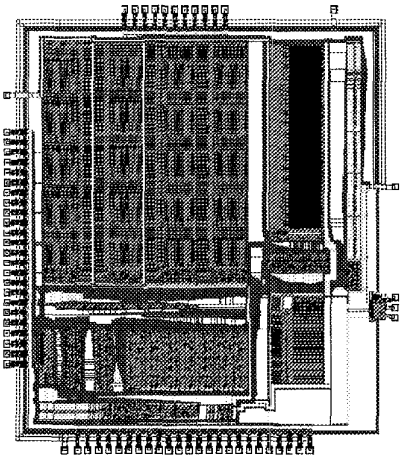

Figure 6: Layout for the Proposed Chip

Table 2: Chip Specification

Technology	0.8 μm
Die size	7.6 mm x 6.7 mm
Transistor count	174973
Power dissipation	952 mW
Pad count	66
Clock Rate	11.5 MHz

Conclusions

In this paper, we introduce the MPEG codec. Later, we describe the detail analysis about the function complexity of MPEG decoder system, and adopt the decoding system with our improvements in a lower rate of computation complexity. Based on the improved algorithm, the

goal for simplicity and low-cost designa is realized. Finally, the dedicated circuit with an efficient architecture of pipeline scheme is obtained. This proposed chip is verified and realized by the GENESIL silicon complier system.

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