Analysis and Application of Miniature 3D Inductor

Chia-Hsin Wu, Chih-Chun Tang, Chi-Kun Chiu and Shen-Iuan Liu

Department of Electrical Engineering
and Graduate Institute of Electronics Engineering
National Taiwan University
Taipei, Taiwan 10617, R.O.C

ABSTRACT

The structure of the miniature 3D inductors is presented in this paper. The proposed miniature 3D inductors have been fabricated in a standard 0.35-μm one-poly-four-metal (1P4M) CMOS process. According to the measurement results, the self-resonance frequency (f_{SR}) of the proposed miniature 3D inductor is at least 34% higher than the conventional stacked inductor. Moreover, the proposed miniature 3D inductor occupies only 16% area of the conventional planar spiral inductor with the same inductance. The analytical equations are derived and the capacitances distribution model is proposed to elucidate why the miniature 3D inductor has the higher self-resonance frequency. A CMOS voltage controlled oscillator (VCO), which utilized the proposed miniature 3D inductors, has also been demonstrated.

1. INTRODUCTION

Monolithic inductors are widely used in CMOS RF circuits, such as LNA [1] and VCO [2]. There are three mainly design considerations of the on-chip inductor, including the quality factor, the self-resonance frequency and the occupied area. The quality factor of the inductor significantly affects the performances of the RF circuits and systems, such as the gain/power ratio [3] and noise figure of LNA, and the phase noise of VCO. Usually, the wide metal width was adopted to achieve the high-Q inductor at the price of the lower self-resonance frequency. Also, the planar inductor occupies the large die area results in the increasing cost of RF IC. Therefore, One inductor with the high quality factor, small area and high self-resonance frequency will greatly benefit the CMOS RF circuit design in all aspects.

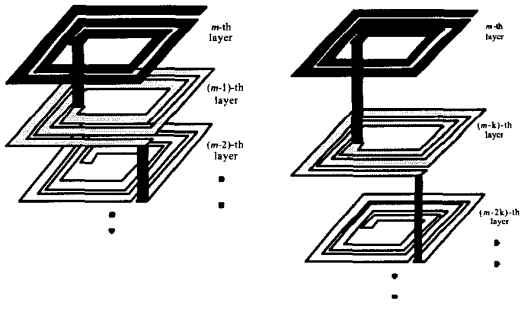
This paper presents a novel miniature 3D inductor structure and the test-keys have been fabricated in a 0.35-μm 1P4M CMOS process. In Section 2, the structures of the stacked and the proposed miniature 3D inductors are described. Analytical equations are derived to compare the self-resonance frequency of the stacked and the miniature 3D inductors in Section 3. We also propose the capacitances distribution model to explain the meanings of the derived expressions. Measurement results, including the characteristics of the proposed inductor, comparison of the self-resonance frequency between the stacked and the miniature 3D inductors, and comparison of the area between the stacked and the miniature 3D inductors, are shown in Section 4. A CMOS VCO, which utilized the proposed miniature 3D inductors, is also demonstrated in this section. After all, the conclusion remarks are given in Section 5.

2. STRUCTURES OF THE MULTI-LAYER INDUCTORS

2.1 Conventional Stacked Inductor

The structure of the conventional stacked inductor, as shown in Fig. 1(a), consists of the series connected spiral inductors in the different metal layers. Every spiral inductor in the different metal layers may have the same or different turns.

Because the stacked inductor utilizes the multi metal layers, it can achieve high inductance in the smaller area. Unfortunately, the more metal layers produce more metal-to-metal capacitances and the lower metal layer generates the larger metal-to-substrate capacitance; thus the stacked inductor suffers from the low self-resonance frequency.



(a) (b)

Fig. 1 Structures of stacked inductors (a).conventional (b) modified.

2.2 Modified Stacked Inductor

In order to reduce the equivalent capacitance of conventional stacked inductor, modified stacked inductor is proposed as shown in Fig. 1(b) [5]. Its structure and model are similar to those of conventional stacked inductor but it is implemented in non-sequent metal layers. The structure often needs three or above three metal layers, and there are somewhat trade-offs between available metal layers and equivalent capacitance reduction.

2.3 Proposed 3D Inductor

Our proposed miniature 3D inductor structure is illustrated in Fig. 2. The miniature 3D inductor consists of at least two or above stacked inductors by series connections and every stacked inductor has only one turn in every metal layer. For an example as shown in Fig. 2, if there are two stacked inductor with the different diameters, one of them is the one turn stacked inductor from the metal layer 4 to the metal layer 2 and the other is the one turn stacked inductor from the metal layer 2 to the metal layer 3, then the miniature 3D inductor is formed by connecting two stacked inductors at the metal layer 2.

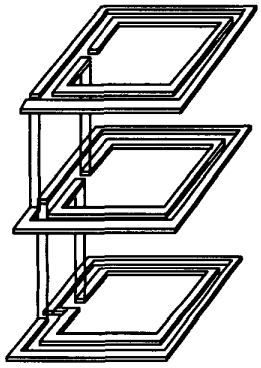


Fig. 2 Structure of the proposed 3D inductor.

3. THE ANALYTIC APPROACH

Stacked and miniature 3D inductors use the multi metal layers to achieve the required inductances in the small area. Unfortunately, using the lower metal layer also decreases f_{SR} of the inductor. In order to investigate f_{SR} of these two types of inductors, the analytical equations have been derived. For simplicity, the following assumptions are made:

1. Ignore the capacitances between the adjacent tracks [5].
2. Assume the wiring metal width is much larger than the spacing, i.e. ignoring the spacing while calculating inductor area.
3. Voltage distribution is proportional to the lengths of the metal tracks, i.e. more long metal track is with more voltage drop.
4. In the same turn, voltage is equal and is determined by averaging the beginning voltage and the ending voltage of the turn.

Suppose that a 2-layer stacked inductor with inner diameter r, metal width w, and n turns in each layer, the voltage profile across the inductor is shown in Fig. 3 and its equivalent capacitance can be expressed as:

$$C_{eqstacked} = \sum_{m=1}^{n}\{C_{m-thp2m}+C_{m-thp2s}\} \quad (1)$$

$$= \sum_{m=1}^{n}\left\{ C_{m2m}\times\pi w\times[2r+(2n-2m-1)w]\times\left[\left(\frac{n-m}{n}\right)\times\frac{2+(n-m-1)\frac{w}{r}}{2+(n-1)\frac{w}{r}}+\frac{1+(n-m)\frac{w}{r}}{n\times\left[2+(n-1)\frac{w}{r}\right]}\right]^2 + C_{m2s}\times\pi w\times[2r+(2n-2m-1)w]\times\frac{1}{4}\times\left[\left(\frac{n-1}{n}\right)\times\frac{2+(2n-m)\frac{w}{r}}{2+(n-1)\frac{w}{r}}+\frac{1+(n-m)\frac{w}{r}}{n\times\left[2+(n-1)\frac{w}{r}\right]}\right]^2\right\}$$

where C_{m2m} and C_{m2s} represent the metal-to-metal and metal-to-substrate capacitances per unit area, respectively. The voltage profile of the miniature 3D inductor is shown in Fig. 4 and the equivalent capacitance is described as:

$$C_{eq,3D} \quad (2)$$

$$= \sum_{m=1}^{n}\left\{ C_{m2m}\times\pi w\times[2r+(2n-2m-1)w]\times\left[\frac{1+(n-m)\frac{w}{r}}{n\times\left[2+(n-1)\frac{w}{r}\right]}\right]^2 + C_{m2s}\times\pi w\times[2r+(2n-2m-1)w]\times\left[\frac{\frac{1}{2}\left[1+(n-m)\frac{w}{r}\right]+(n-m)\times\left[2+(n-m-1)\frac{w}{r}\right]}{n\times\left[2+(n-1)\frac{w}{r}\right]}\right]^2\right\}$$

Based on Eq. (1) and Eq. (2), we develop 4-layer equivalent capacitance formulas. According to the manual provided by the foundry [4], $C_{M4,M3}$ is 4.49e-17 F/um^2, $C_{M3,M2}$ is 3.63e-17 F/um^2, $C_{M2,M1}$ is 3.76e-17 F/um^2 and $C_{M1,sub}$ is 6.2e-17 F/um^2. Fig. 5 shows the simulated equivalent capacitances of the 4-turn 2-layer stacked inductor and miniature 3D inductor with different sizes. It shows that the equivalent capacitances of the stacked inductors are larger than those of the miniature 3D inductors. Because the self-resonance frequency of the inductor can be defined as $f_{SR} = (2\pi\sqrt{L_{eq}C_{eq}})^{-1}$, where L_{eq} and C_{eq} are the equivalent inductance and capacitance, respectively, thus the analytical analysis indicates that the miniature 3D inductor has the higher f_{SR} than the stacked inductor.

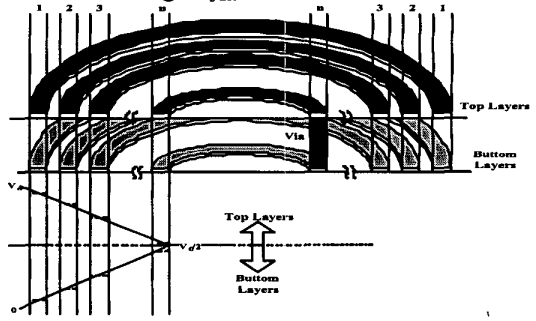


Fig. 3. Voltage profile of the stacked inductor.

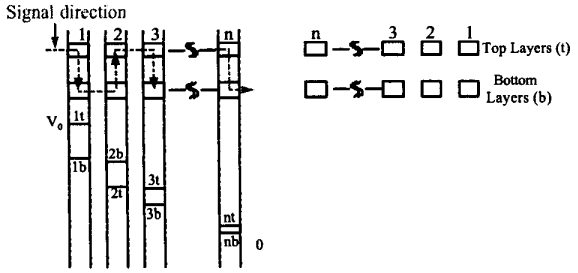
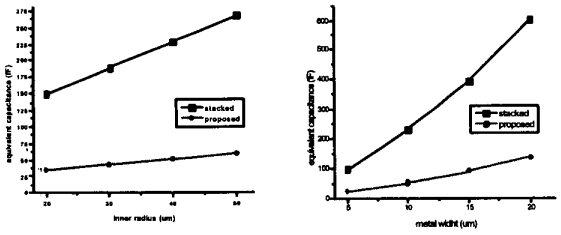


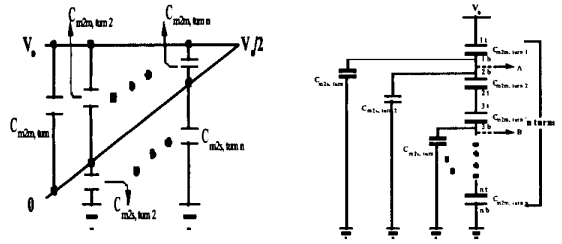
Fig. 4. Voltage profile of the miniature 3D inductor.



(a) (b)

Fig. 5. Simulated equivalent capacitance (a) different inner radiuses with w=10μm, (b) different metal widths with r=40μm.

In order to give the more straightforward explanations of why the miniature 3D inductor has the smaller equivalent capacitance and the higher f_{SR}, the capacitances distribution models are proposed to elucidate this phenomenon. Fig. 6 shows the capacitances distribution model of the n-turn 2-layer stacked inductor. While increasing the turns of the stacked inductor, the more and more metal-to-metal and metal-to-substrate capacitances are generated and parallel connected thus the equivalent capacitances become the larger and larger. Hence, the self-resonance frequency of the stacked inductor decreases while the number of turns increases. In contrast to the stacked inductor, while increasing the turns, the more and more metal-to-metal capacitances are generated and series connected thus the equivalent capacitances become the smaller and smaller, as shown in Fig. 7. So, f_{SR} of the miniature 3D inductor is higher than the stacked inductor with the same turns and layers.



(a) (b)

Fig. 7. Capacitance distribution model (a) stacked (b) proposed.

4. EXPERIMENTAL RESULTS

The proposed miniature 3D inductors had been fabricated in a 0.35-μm standard 1P4M CMOS process. A CMOS VCO had also been fabricated in the same process to verify the functions of the miniature 3D inductors.

4.1 Formulas Validation

Table I shows the measured equivalent capacitance and simulated equivalent capacitance of stacked inductors and proposed 3D inductors to demonstrate the accuracy of equivalent capacitance formulas. The error is less than 5%.

4.2 Compared with the Planar Inductor

Fig. 7 shows one planar inductor and one circuit with two miniature 3D inductors. The sizes of the planar inductor and miniature 3D inductor are 220μm X 220μm and 80μm X 80μm, respectively. In this example, the miniature 3D inductor uses only 16% area to achieve the same inductance with the planar inductor and even better quality factor compares to the planar inductor, as shown in Fig. 8.

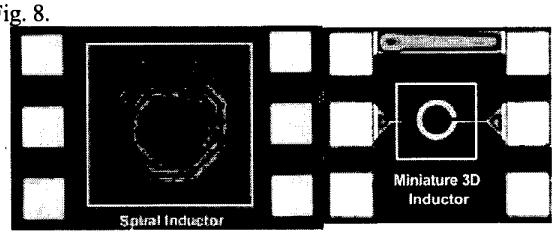


Fig. 6. Die photo of the planar and the miniature 3D inductors with the same inductance.

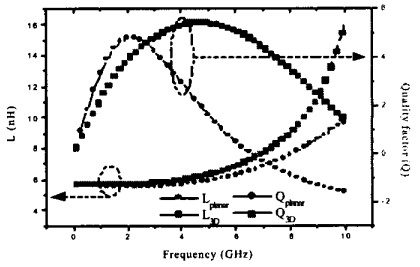


Fig. 8. Measured L and Q of the planar and the miniature 3D inductors.

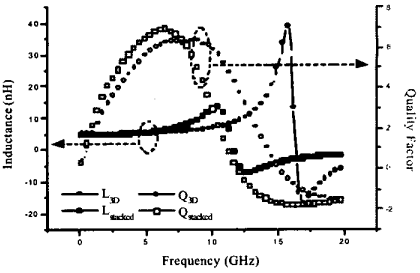


Fig. 9. Measured L and Q of the stacked and the miniature 3D inductors.

4.3 Compared with the Stacked Inductor

In order to compare the self-resonance frequency of the stacked and the miniature 3D inductors, a 2-turn 4-layer stacked inductor has also been fabricated in the same process with 40μm inner diameter, 10μm metal width, 1μm spacing. Fig. 9 displays the inductance and quality factor of the stacked and miniature 3D inductors with the same area. Miniature 3D inductor increases 34% self-resonance frequency with only 8% degradation of the quality factor.

4.4 Application

The die photo of the CMOS LC-Tank VCO, which fabricated in a 0.35-μm 1P4M CMOS process and utilized the miniature 3D inductors, is shown in Fig. 10. This VCO occupies only 450 X 330 μm^2 (not including the pads for testing). With a 3.3V supply voltage, the VCO consumes about 3.43mA. The measured phase noise is −89.1dBc/Hz at 100kHz offset from the 3-GHz carrier

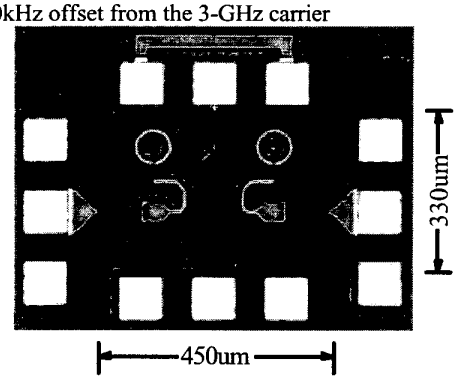


Fig. 10 Die photo of the VCO.

5. CONCLUSIONS

In this paper, a miniature 3D inductor structure is proposed. Compare to the planar inductor, the performances of the miniature 3D inductor are superior to the planar inductor in all aspects, especially saving about 80% area. We also derive the analytical equations and propose the capacitances distribution models to prove the miniature 3D inductor has the higher self-resonance frequency than the stacked inductor, and finally verified by the experimental result. Owing to the advantages of the small area and high self-resonance frequency, the proposed miniature 3D inductor is very suitable for the RF applications. Finally, the proposed structure is not only for CMOS technology but also can be applied to SiGe or Bipolar process.

6. REFERENCES

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TABLE I

The Equivalent Capacitances of Stacked, and Proposed 3D Inductors in 0.35-μm CMOS process (w = 10μm, *spacing* = 1μm, *Employed Metal layers* = M4, M3, M2, M1).

Inductor Configuration	L(nH)	Measured Equivalent Cap (fF).	Simulated Equivalent Cap (fF).	Inner Radius	Turns	Error
Stacked	7.3	54.2	52.4	30	2	3.3%
Stacked	16.7	90.2	86.3	30	3	4.1%
Stacked	31.3	129.4	125.2	50	3	3.3%
Proposed	5.0	24.4	25.2	20	2	3.2%
Proposed	7.5	33.6	35.0	30	2	4.1%
Proposed	9.7	42.9	44.9	40	2	4.6%