an improvement of 13·4 dB in receiver sensitivity. A sensitivity of −36·8 dBm was measured for a 1100 sequence, which agrees very well with the predicted sensitivity of −37·6 dBm.

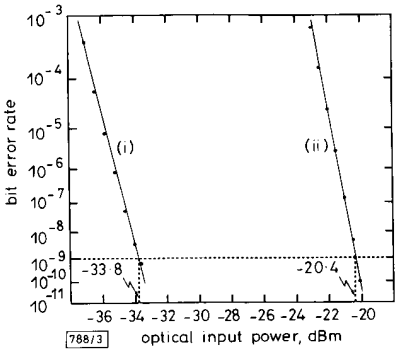

Fig. 3 *10 Gbit/s bit error rate curves*
(i) with optical preamplifier
(ii) without optical preamplifier

The increased penalty (3·0 dB) incurred for a $2^7 - 1$ PRBS as compared to the 1100 result when using an optical preamplifier, is believed to be due to the impact of patterning of the optimal threshold setting in the decision circuit.

Conclusions: A high performance 10 Gbit/s transmission testbed has been developed and a sensitivity of −20·4 dBm has been achieved for a $2^7 - 1$ PRBS. This is the best reported result for a 10 Gbit/s *pin*-FET receiver.

A high gain (27·2 dB), low noise figure (5·6 dB) EDF preamplifier pumped at 1480 nm has been realised. This optical preamplifier has been used to achieve a sensitivity of −33·8 dBm (325 photons/bit) at 10 Gbit/s for a $2^7 - 1$ PRBS, at a wavelength of 1548 nm. This is the highest reported sensitivity at 10 Gbit/s for an EDFA pumped at 1480 nm. The result for a 1100 sequence is −36·8 dBm (163 photon/bit), which agrees very well with predicted performance. This also indicates that there is potential for improvement in performance. By reducing patterning, it is expected that a sensitivity of −35 dBm to −36 dBm could be achieved at 10 Gbit/s using an EDFA pumped at 1480 nm. These results illustrate that erbium-doped fibre amplifiers make 10 Gbit/s transmission viable over cost-effective span lengths.

Acknowledgments: The authors would like to thank the Directors of BNR Europe Limited for permission to publish this Letter.

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10th September 1991

References

1 HENMI, N., *et al.*: 'Rayleigh scattering influence on performance of a 10 Gbit/s optical receiver with an Er doped fibre amplifier'. OFC '90, THC5, p. 155
2 BLAIR, L. T., and NAKANO, H.: 'High sensitivity 10 Gbit/s optical receiver using two cascaded EDFA preamplifiers', Electron. Lett., 1991, **27**, pp. 835–836
3 SAITO, T., *et al.*: 'High receiver sensitivity at 10 Gbit/s using an Er-doped fibre preamplifier pumped with a 0·98 μm laser diode'. OFC'91, PD14, pp. 65–68
4 DESURVIRE, E., and SIMPSON, J. R.: 'Amplification of spontaneous emission in erbium-doped single-mode fibres', *J. Lightwave Technol.*, **LT-7**, pp. 835–845

CRYSTALLINE *p*MOS INVERTER USING AMORPHOUS THIN FILM TRANSISTOR AS ACTIVE LOAD

Indexing terms: Inverters, Semiconductor devices and materials, Transistors

The integration of the amorphous silicon (a-Si : H) thin film transistor on top of a crystalline *p*-type silicon metal–oxide–semiconductor (*p*MOS) transistor to serve as active load has been achieved successfully. The vertical integration of crystalline silicon and amorphous silicon circuits to form the three dimensional structure is a promising technique for future application in high density memory cells and neural network image sensors.

The recent advance in 4 Mbit SRAM[1–3] relies on the stacking of the load element, i.e. thin film transistor (TFT), on top of the metal–oxide–semiconductor (MOS) transistor. The purpose is to reduce the cell area. We present the results on the successful integration of an amorphous silicon TFT (load) on top of the crystalline *p*-channel MOS (*c*-*p*MOS) transistor. Fig. 1*a* and *b* show the circuit diagram and cross-section of the integrated crystalline *p*MOS inverter with amorphous

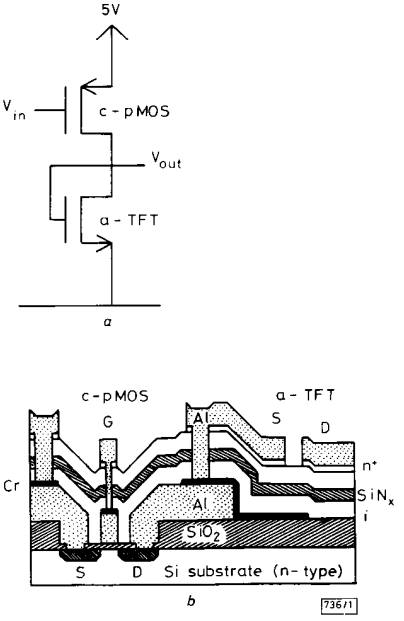

Fig. 1 *Circuit diagram and cross-section of integrated common gate CMOS circuit consisting of crystalline pMOS and amorphous silicon TFT*
a Circuit diagram
b Cross-section

silicon TFT (*a*-TFT) as an active load. The fabrication processes are as follows. The starting silicon wafer is a lightly doped *n*-type substrate. After a standard RCA cleaning process, the 7000 Å field oxide is grown. The first lithographic step is a source and drain patterning, in which the source and drain regions of the MOS field effect transistor are etched using buffered oxide etch. A thin buffer oxide about 300 Å thick is then grown, followed by source and drain implantation with BF_2^+. The second step is to define the active region. The oxide in this region is first stripped. A 400 Å thick gate oxide is then regrown, its quality and uniformity being critical in determining the proper device characteristics. The next step is to open source and drain contact regions. The final step is to pattern Al followed by annealing at 350°C for 10 min and the crystalline *p*MOS is completed. The gate length and width of *c*-*p*MOS are 30 and 300 μm, respectively.

As for the fabrication processes for the upper a-TFT, the first step is the deposition of 2000 Å Cr to serve as etch stop because the etching solution of a-Si : H will also attack the underlying Al.

Afterwards, an a-Si : H i layer, SiN_x, a-Si : H i, and n^+ layers are grown successively. The first i layer is a buffer layer to separate the gate oxide SiO_2 and SiN_x. It is found that if no buffer layer is inserted between these two materials, the underlying c-pMOS will be seriously degraded due to the stress between SiO_2 and SiN_x. SiN_x is the gate insulator of the a-TFT, the second a-Si : H i layer serves as the channel and the n^+ layer is the contact layer. The windows are then opened to contact the underlying Cr. Finally the Al layer is evaporated and patterned and the n^+ a-Si : H layer is then etched away by reactive ion etching (RIE). This completes the entire fabrication processes. The gate length and width of the a-TFT are 25 and 400 μm, respectively.

Fig. 2a shows the common source I–V characteristics of the c-pMOS in this integrated inverter. The gate bias V_G varies

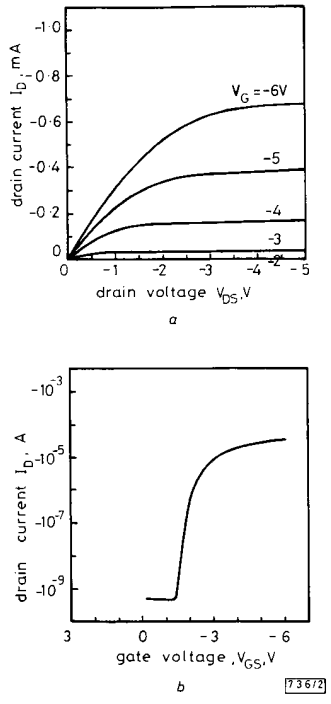

Fig. 2 *Common source I–V characteristics of c-pMOS in this integrated inverter and I–V transfer characteristics of c-pMOS in integrated circuit*

a Common source I–V characteristics
Gate bias V_G varies from 0 to −6 V
b I–V transfer characteristics
Drain voltage V_{DS} is kept at constant −0·1 V

from 0 to −6 V. Fig. 2b displays the transfer I_D against V_{GS} curve with drain voltage V_{DS} = −0·1 V. The threshold voltage is 1·5 V. The hole mobility as calculated from the transconductance is 39 cm^2/V s. Fig. 3 shows the I–V characteristics of an a-TFT load with gate and drain shorted. This I–V characteristic indicates that the equivalent resistance of the active load is not constant and is large at low gate bias. The drain current has not saturated at a drain bias of 5 V. Fig. 4 shows the transfer curve of this inverter. When the input voltage (gate voltage of c-pMOS) is below 3·2 V, the c-pMOS is on while the dynamic resistance of the a-TFT is high, which makes the output voltage V_{out} high; when the input voltage is more than 3·5 V, the c-pMOS is turned off and the output voltage is pulled down to less than 0·5 V. In conclusion, the integration of amorphous Si : H TFT on top of crystalline pMOS to serve as active load has been successfully achieved.

In the fabrication of the a-TFT onto the crystalline pMOS, a new technique of inserting an a-Si : H i layer between SiO_2

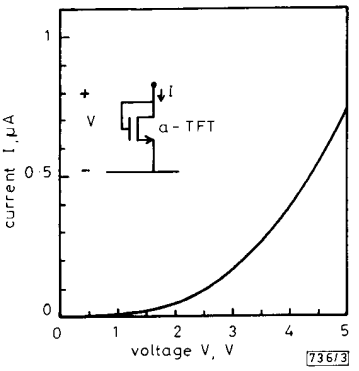

Fig. 3 *I–V characteristics of a-TFT load with drain and gate shorted*

and SiN_x layer successfully solves the stress problem and preserves the usual performance of the crystalline MOSFET. The success of the integration of crystalline silicon device and amorphous silicon device is a key step in future three dimensional memory cell and neural network applications.

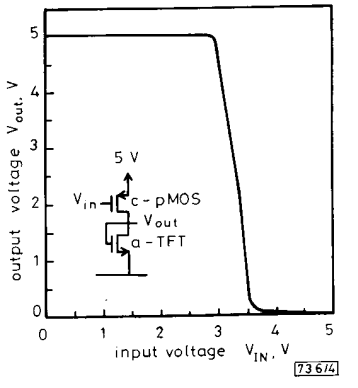

Fig. 4 *Transfer curve of integrated circuit using a-TFT as active load*

Acknowledgment: This work is supported by the National Science Council of the Republic of China under contract No. NSC 80-0417-E002-04.

4th September 1991

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References

1 ADAN, A. O., SUZUKI, K., SHIBAYAMA, H., and MIYAKE, R.: 'A half-micron SRAM cell using a double-gated self-aligned polysilicon PMOS thin film transistor load'. Proc. IEEE 1990 Symp. VLSI Technology, 1990, pp. 19–20

2 UEMOTO, Y., FUJII, E., NAKAMURA, A., and SENDA, K.: 'A high-performance stacked-CMOS SRAM cell by solid phase growth technique'. Proc. IEEE 1990 Symp. on VLSI Technology, 1990, pp. 21–22

3 KINUGAWA, M., KAKUMA, M., YOSHIDA, T., NAKAYAMA, T., MORITA, S., KUBOTA, K., MATSUOKA, F., OYAMATSU, H., OCHII, K., and MACGUCHI, K.: 'TFT (thin film transistor) cell technology for 4 Mbit and more high density SRAMs'. Proc. IEEE 1990 Symp. on VLSI Technology, 1990, pp. 23–24