Low-voltage CMOS four-quadrant multiplier

Shen-Iuan Liu and Chen-Chieh Chang

Indexing terms: Analogue multipliers, CMOS integrated circuits, Multiplying circuits

A new CMOS four-quadrant multiplier that can operate from supply voltages of ±1.5V is presented. This circuit was fabricated in a standard 0.8μm single-poly double-metal CMOS process. Experimental results show that the nonlinearity can be kept <2% across the entire differential input voltage range of ±0.8V. The total harmonic distortion is <2% with the differential input range up to ±0.8V. The measured –3dB bandwidth of this multiplier is ~5MHz. It is expected to be useful in low-voltage analogue signal-processing applications.

Introduction: Battery-powered systems such as implantable biomedical systems, portable communication equipment and hand-held movie cameras [1, 2], etc. require circuits which operate at low supply voltages and have low power consumption. Thus, the demand for analogue circuits that can operate from low supply voltages is very high. Multipliers are a very important building block in many applications, such as adaptive filters, frequency doublers, and modulators. Recently, several low-voltage CMOS/BICMOS four-quadrant multipliers and amplifiers have been presented using the transistors operated in the triode and weak inversion regions [3 – 7]. In this Letter, a new low-voltage CMOS multiplier is presented. Experimental results are also given to verify theoretical analysis.

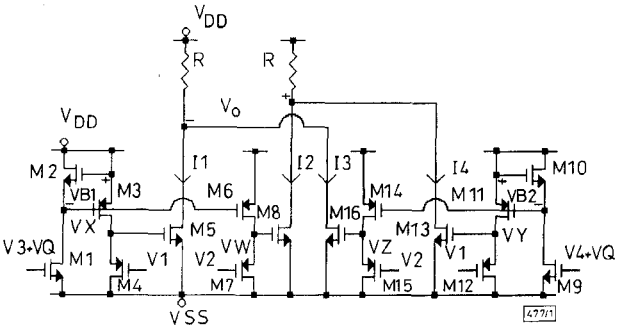

Fig. 1 *Proposed low-voltage CMOS four-quadrant multiplier*

Circuit description: The proposed four-quadrant multiplier is shown in Fig. 1. Assume that all NMOS transistors in Fig. 1 are matched and operate in the saturation region, as do the PMOS transistors. Neglecting the body effect, the gate-to-source voltages of the NMOS transistors M_1 and M_2 will be equal and can be expressed as

$$V_Q + V_3 - V_{SS} = V_{B1} \quad (1)$$

For the matched PMOS transistors M_3 and M_4 (also for M_6 and M_7), a similar relation yields

$$V_{B1} = V_X - V_1 = V_W - V_2 \quad (2)$$

The *n-p* cross-coupling configuration [8] ensures that V_{B1} is constant regardless of the types of transistors. For transistors M_9, M_{10}, M_{11}, M_{12}, M_{14} and M_{15}, the following relation can be obtained:

$$V_Q + V_4 - V_{SS} = V_{B2} = V_Y - V_1 = V_Z - V_2 \quad (3)$$

Assume that NMOS transistors M_5, M_8, M_{13} and M_{16} are matched. Their drain currents can be expressed as

$$I_1 = K(V_X - V_{SS} - V_{Tn})^2 \quad (4)$$

$$I_2 = K(V_W - V_{SS} - V_{Tn})^2 \quad (5)$$

$$I_3 = K(V_Z - V_{SS} - V_{Tn})^2 \quad (6)$$

$$I_4 = K(V_Y - V_{SS} - V_{Tn})^2 \quad (7)$$

From eqns. 1 – 3, the voltages V_X, V_Y, V_Z, and V_W can be expressed in terms of voltages V_1, V_2, V_3, V_4, V_Q and V_{SS}. Substituting them into eqns. 4 – 7 and after some algebraic calculations, the output current I_o of this multiplier can be defined

$$I_o \equiv I_1 + I_3 - I_2 - I_4 = 2K(V_1 - V_2)(V_3 - V_4) \quad (8)$$

Similarly, the output voltage V_o of this multiplier will be

$$V_o = I_o R = 2KR(V_1 - V_2)(V_3 - V_4) \quad (9)$$

For proper operation, the following constraints should be satisfied:

$$V_{SS} - |V_{TP}| < V_1, V_2 < V_{DD} - \max(V_{B1}, V_{B2}) \quad (10)$$

and

$$V_{SS} - V_Q + V_{Tn} < V_3, V_4 < (2V_{DD} + V_{Tn})/2 - V_Q \quad (11)$$

where voltages V_{TP} and V_{Tn} are the threshold voltages of the NMOS and PMOS transistors, respectively.

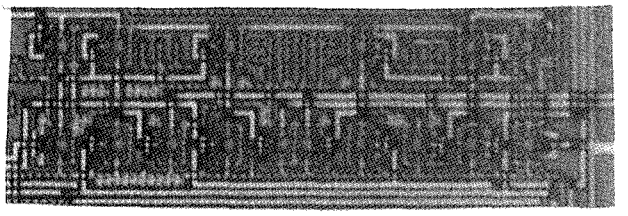

Fig. 2 *Die photograph of proposed multiplier*

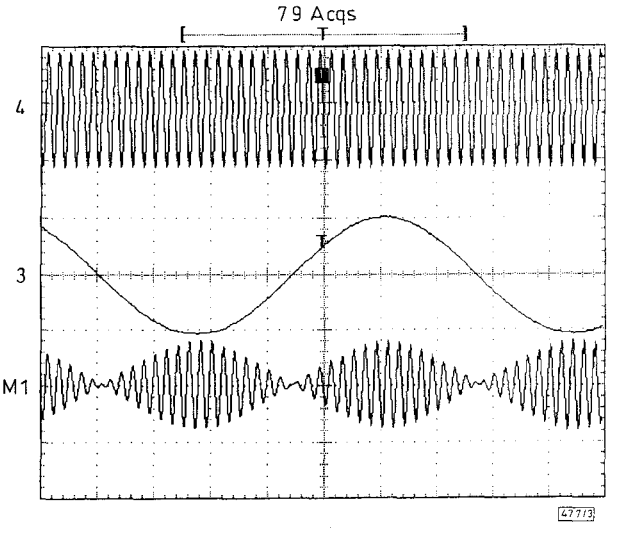

Fig. 3 *Output waveforms*

Uppermost trace (500mV/div) is voltage V_1 (= $-V_2$) with 0.5V, 100kHz sinusoidal signal
Middle trace is voltage V_3 (= $-V_4$) with 0.5V, 3kHz sinusoidal signal
Lowest trace (25mV/div) is output of multiplier
Horizontal scale is 50μs/div

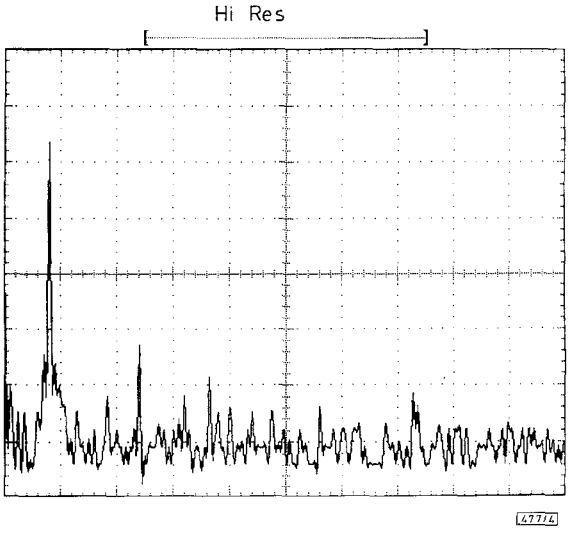

Fig. 4 *Measured spectrum of output waveform where V_1 (= $-V_2$) is a 0.5V, 20kHz sinusoidal signal and V_3 (= $-V_4$) = 0.4V*

Vertical scale: 10dB/div
Horizontal scale: 25kHz/div

Experimental results: The circuit was fabricated in a standard 0.8 μm single-poly double-metal CMOS process. All the aspect ratios (W/L) of the devices in Fig. 1 are equal to 5μ/5μ. The measurement conditions are $R = 22k\Omega$ and the supply voltage is ±1.5V. Fig. 2 shows the die photograph of the proposed multiplier. The linearity of the multiplier is within 2% for $|V_3 (= -V_4)| < 0.8V$. The measured −3dB bandwidth of this multiplier was ~5MHz. To demonstrate its time-domain response, two signals are applied to the proposed multiplier. The voltage $V_1 (= -V_2)$ is a 0.5V, 100kHz sinusoidal signal. The voltage $V_3 (= -V_4)$ is a 0.5V, 3kHz sinusoidal signal. Its output waveform is shown in Fig. 3. The total harmonic distortion of the output voltage was found to be <2% for $|V_1 (= -V_2)| < 0.5V$ and $V_3 = -V_4 = -0.4V$. Fig. 4 shows the measured spectrum of the output voltage with $V_1 (= -V_2)$ being a 0.5V, 20kHz sinusoidal signal and $V_3 (= -V_4) = 0.4V$.

Conclusions: A low-voltage CMOS four-quadrant multiplier is presented. Experimental results show that the nonlinearity can be kept to <2%, across the entire differential input voltage range of ±0.8V. The total harmonic distortion is <2%, with the differential input range up to ±0.8V. This multiplier is expected to be useful in many analogue signal-processing applications.

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Shen-Iuan Liu and Chen-Chieh Chang *(Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan 10664, Republic of China)*

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Performance estimation of Si/SiGe hetero-CMOS circuits

R. Hagelauer, T. Ostermann, U. König, M. Glück and G. Höck

Indexing terms: Silicon, Silicon-germanium, CMOS integrated circuits

Semiquantitative performance extrapolation of Si/SiGe heterostructure *p*- and *n*-channel devices point to transconductances above 1000mS/mm and cutoff frequencies around 200GHz. Circuits such as inverters, logic arrays (e.g. NAND-gates) and flip-flops are simulated with feature sizes down to 0.05μm showing a promising performance potential. Delay times of 2.5 and 0.5ps/stage are obtained for an inverter chain at a power supply voltage of 1 and 2.5V, respectively.

Introduction: The progress of microelectronics is based on the advances of CMOS technology. Over the past 20 years, feature sizes have evolved from 6 to 0.25μm and this trend will continue to at least 0.07μm. With 0.1μm CMOS technology gate delays of 22ps/stage at 1.5V [1] and 11.8ps/stage at 2.5V [2] have been reported. However, CMOS circuit performance seems to be limited by short channel effects (punch-through, bulk doping, ...) for effective channel lengths < 0.25μm. As scaling of silicon becomes more difficult, hetero-FETs (HFETs) or modulation doped FETs (MODFETs) have become of greater interest. Si/SiGe heterostructure technology offers the best opportunity to combine the advantages of heterodevices with the well established Si CMOS technology.

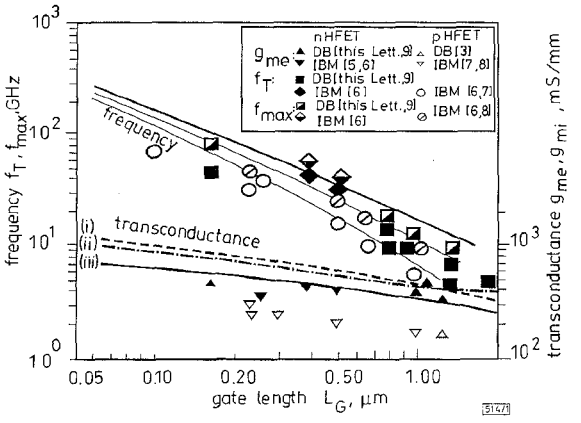

Fig. 1 *Gate length dependence of transconductance and cutoff frequencies for SiGe MODFETs*

Comparison of experimental data and calculations based on velocity saturation charge control model after Das *et al.* [10], which was adapted to SiGe HFETs
gml: (i), (ii), (iii) see text
f_T: ——— $V_{sat}/2\pi L_G$ - see text

Si/SiGe hetero-FET performance: Si/SiGe hetero-FETs consist of an Si or SiGe layer, vertically separated from the MOS or Schottky gate by an SiGe and/or Si layer [3]. The layer sequence can either be undoped or modulation-doped. The 2-D electron or hole gas confined in the channels yield high RT-mobilities, up to 2900cm²/Vs or up to 1800cm²/Vs, respectively, at electron or hole concentrations around 1012cm⁻² [3, 4] and drift velocities close to the saturation. Preliminary devices have already demonstrated promising performances, e.g. transconductances up to 400–500mS/mm for *n*-type HFETs and up to 280mS/mm for *p*-type HFETs as shown in Fig. 1 [3, 5 – 9] Experiments so far have not established a significant gate length dependence. The simulations for *n*-HFETs in Fig. 1, based on the velocity saturation charge control model after Das *et al.* [10] and fitted to the best data at gate lengths at ~1μm, assume the channel to be 12 or 20nm beneath a Schottky gate, a capacitance of 10^{-6}F/cm² (curves (i) and (ii)) or 6 × 10^{-7}F/cm² (curve (iii)), a mobility of 2500 (curve (i) and (ii)) or 3000cm²/Vs (curve (iii)), a drain current constant at 150mA/mm (curve (ii)) or even increasing from 100 to 450mA/mm (curves (i) and (ii)) with decreasing gate lengths L_G. Transconductances of > 1000mS/mm may become possible for *n*-HFETs. For ideal *p*-HFETs, transconductances close to this are expected owing to about the same high mobilities and drift velocities at least when using Ge *p*-type channels. However, that has not been confirmed by experiments with Ge channels due to technological problems related to the thick SiGe buffer layers and mobilities only at ~500cm²/Vs [3, 7]. In Fig. 1 we have also shown cutoff frequencies of *n*- and *p*-HFETs [6 – 8] and new own data for L_G = 0.18 to 2μm. At around 1μm, 14GHz can be obtained and at 0.4μm, ~50GHz for *n*-HFETs. A very high f_{max} of 81GHz was recently found for a 0.18μm T-gate *n*-MODFET [9]. The cutoff frequencies of *p*-HFETs are 30–40% smaller, with a record of f_t = 70GHz at L_G = 0.1μm by IBM in collaboration with universities [7]. The frequencies exhibit a clear gate length dependence close to our simulations (based on [10]) with predictions of > 200GHz. The simulations assume a capacitance of 4 × 10^{-7}F/cm², a channel population of 2 × 10^{12}cm⁻², a saturation velocity of 10^7cm/s, no velocity overshoot and mobilities from 1000 to 3000cm²/Vs. When the gate to channel distance is increased, the transconductance will