```
Q1 0 5 4 BJTP
.ENDS
.MODEL MOSN NMOS(IS=20N KP=26 VTO=5.55V RD=0.5m
  CGSO=160u)
.MODEL BJTP PNP(BF=0.26 TF=1.5U CJC=0.6N RE=1m BR=0.44
  IS=2e-15 NF=2 XTI=6 XTB=5)
```

Table 1: Comparison of different models

	Composite model	Equation model	New model	Device
t_{don}, ns	180	150	150	160
t_r, ns	80	95	95	90
t_{doff}, ns	350	950	950	950
t_f, ns	150	150	150	150
CPU time, s	7.2	108	11	

Results and comparison: A PT-IGBT with a breakdown voltage of 1200V and die size of 12mm square is modelled in PSpice based on three models: the BJT-MOSFET composite model, the equation model and the new model. The output characteristics of the different models are compared in Fig. 2 together with the experimental results. All these models satisfactorily reproduce the static performance of the IGBT. Dynamic performance is tested in a hard-switched circuit with a clamped inductive load. The switching performance parameters and the computational times of the different models are listed in Table 1. The new model simulates the dynamic performance as accurately as the equation model, but its computational time is significantly less. In addition, convergence with the new model is better than with the more complex equation based model.

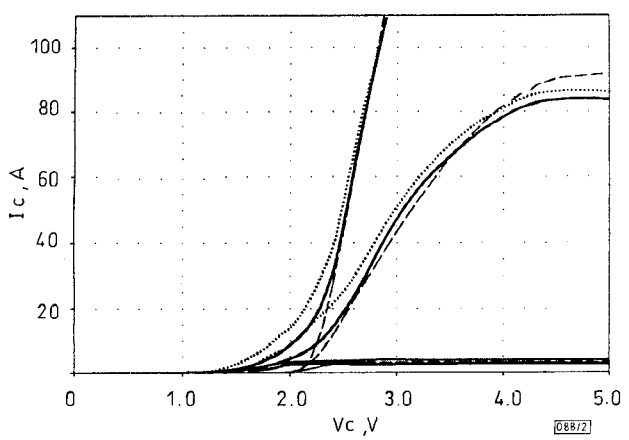

Fig. 2 *Static characteristics comparison*
..... equation model
——— composite model and new model
– – – – experiment

Conclusion: In this Letter, a new IGBT model for PSpice has been proposed and compared with the BJT-MOSFET composite model and the equation based model. The new model possesses the advantages of the two and is efficient, accurate and reliable. The new method for modelling is also applicable to other high-voltage power devices where PSpice usually inaccurately models capacitance high-voltage dependence.

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References

1 BALIGA, B.J.: 'Modern power devices' (Wiley, New York, 987)
2 HEFNER, A.R., and DIEBOLT, D.M.: 'An experimentally verified IGBT model implemented in the Saber circuit simulator', *IEEE Trans. Power Electron.*, 1994, **9**, pp. 532–542
3 MITTER, C.S., HEFNER, A.R., CHEN, D.Y., and LEE, F.C.: 'Insulated gate bipolar transistor (IGBT) using IG-Spice'. IAS'93, 1993, pp. 24–33
4 PROTIWA, F.F., APELDOORN, G., and GROOS, N.: 'New IGBT model for PSpice'. EPE'93, 1993, pp. 226–231
5 SHEN, Z., and CHOW, T.P.: 'Modelling and characterisation of the insulated gate bipolar transistor (IGBT) for SPICE simulator'. ISPSD'93, 1993, pp. 165–170

Higher-order immittance function synthesis using CCIIIs

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Indexing terms: Current conveyors, Current-mode circuits

Two general methods for synthesising higher-order immittance functions using CCIIIs are presented. One of the advantages of these methods is that the proposed circuits require only grounded resistors and grounded capacitors. Moreover, the proposed immittance functions can be applied to realise higher-order filter applications. Simulation results are given to verify theoretical analysis.

Introduction: Several circuits for realising immittance functions using second-generation current conveyors (CCIIs) have been reported [1 – 5]. Recently, a new building block called a third-generation current conveyor (CCIII) [6, 7] has been presented. However, little attention has been paid to realising various immittance functions by using CCIIIs. In this Letter, two general methods are presented for realising higher-order immittance functions using CCIIIs. These methods only require grounded passive components. Moreover, these immittance functions can be applied to realise various higher-order filters. Simulation results are given to verify the theoretical analysis.

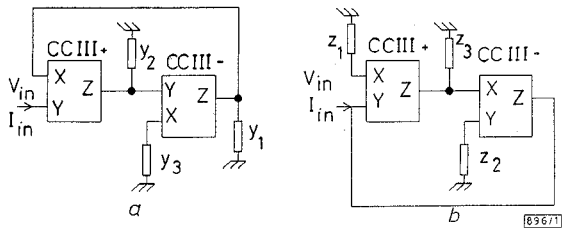

Fig. 1 *Basic admittance and impedance function using two CCIIIs*
a Basic admittance function
b Basic impedance function

Circuit description: The port relations of a CCIII can be characterised by the following matrix:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (1)$$

where the positive and negative signs of the current I_Z denote the non-inverting CCIII and inverting CCIII, respectively. A possible implementation of a CCIII± has been presented recently [7] and, therefore, the circuit complexity of a CCIII can be reduced further. Considering the first basic building circuit in Fig. 1*a*, it consists of a non-inverting CCIII, an inverting one and three grounded admittances. Its driving-point admittance function can be expressed as

$$\frac{I_{in}}{V_{in}} = Y_{in} = Y_1 + \frac{Y_1 Y_3}{Y_2} \quad (2)$$

The second building block is shown in Fig. 1*b*, which consists of a non-inverting CCIII, an inverting one and three grounded impedances. Its driving-point impedance can be given as

$$\frac{V_{in}}{I_{in}} = Z_{in} = Z_1 + \frac{Z_1 Z_3}{Z_2} \quad (3)$$

It has been found that the circuits of Figs. 1*a* and *b* can simulate two kinds of immittance elements in parallel and in series, respectively, by suitably choosing passive elements. Two methods are

proposed to synthesise the higher-order immittance functions by using the basic blocks in Figs. 1*a* and *b*. The higher-order immittance function can be realised by using the circuit, which is similar to Fig. 1*a*, in place of Y_3 in Fig. 1*a* or by using the circuit, which is similar to Fig. 1*b*, in place of Y_2 in Fig. 1*a*. For example, the higher-order immittance circuit is shown in Fig. 2 by using the basic block in Fig. 1*a*. Its immittance function can be given as

$$Y_{in} = Y_1 + \frac{Y_1Y_3}{Y_2} + \frac{Y_1Y_3Y_5}{Y_2Y_4} \quad (4)$$

By connecting similar stages, we can realise the higher-order immittance function which can be expressed by the following equation:

$$Y_{in} = Y_1 + \frac{Y_1Y_3}{Y_2} + \frac{Y_1Y_3Y_5}{Y_2Y_4} + \cdots + \frac{Y_1Y_3 \ldots Y_{2n-1}}{Y_2Y_4 \ldots Y_{2n-2}} \quad (5)$$

Similarly, the higher-order immittance functions can be realised by using the circuit, which is similar to Fig. 1*b*, in place of Z_3 in Fig. 1*b* or by using the circuit, which is similar to Fig. 1*b*, in place of Z_2 in Fig. 1*b*. All the proposed circuits use only grounded resistors and grounded capacitors which are suitable for monolithic integration [8].

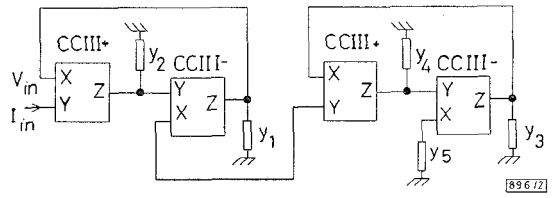

Fig. 2 *Higher-order admittance function using circuit in Fig. 1a*

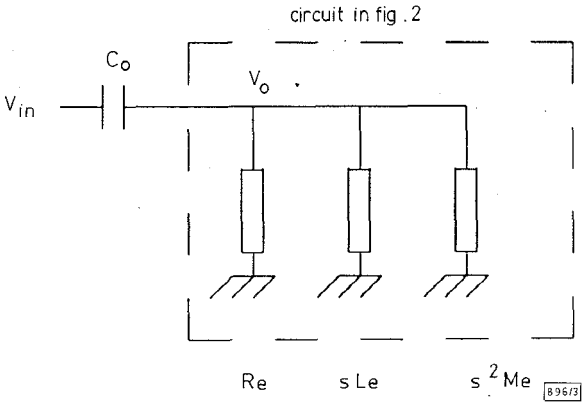

Fig. 3 *Equivalent circuit for third-order highpass filter*

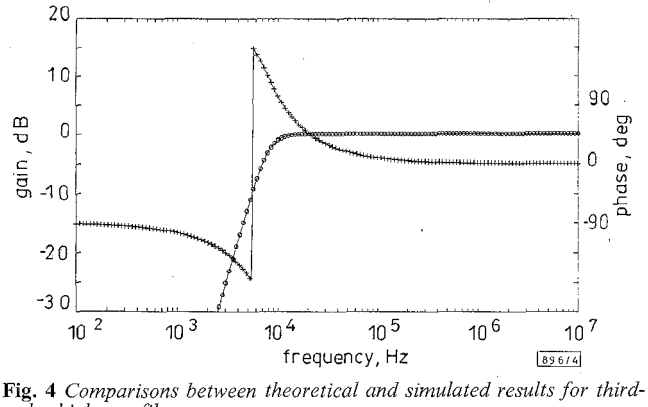

Fig. 4 *Comparisons between theoretical and simulated results for third-order highpass filter*

——— theoretical gain
O simulated gain
——— theoretical phase
\+ simulated phase

Simulation results: To verify theoretical analyses, a proposed immittance function is used to realise a third-order highpass filter. The CCIII is constructed by two CMOS CCIIs [9]. As an example, a third-order highpass filter can be realised by inserting a capacitor C_0 to the immittance function as shown in Fig. 2 with $y_1 = 1/R_1$, $y_2 = sC_2$, $y_3 = 1/R_3$, $y_4 = sC_4$ and $y_5 = 1/R_5$. According to eqn. 4, its driving-point admittance can be

$$Y_{in} = \frac{1}{R_e} + \frac{1}{sL_e} + \frac{1}{s^2M_e} \quad (6)$$

where $R_e = R_1$, $L_e = R_1C_2R_3$ and $M_e = R_1C_2R_3C_4R_5$. Its equivalent circuit is shown in Fig. 3. And its transfer function can be expressed as

$$T(s) = \frac{s^3}{s^3 + s^2\frac{1}{C_0R_e} + s\frac{1}{C_0L_e} + \frac{1}{C_0M_e}} \quad (7)$$

This third-order highpass filter is realised with $R_1 = 10\text{k}\Omega$, $R_3 = 20\text{k}\Omega$, $R_5 = 40\text{k}\Omega$ and $C_0 = C_2 = C_4 = 1\text{nF}$. Fig. 4 shows the simulation results which confirm with results of the theoretical analysis.

Conclusions: In this Letter, the general higher-order immittance functions using CCIIIs have been presented. One of the advantages of this proposed circuit is that it only requires grounded resistors and capacitors. Two methods are also presented to synthesise the higher-order immittance. Moreover, the proposed immittance circuit can be also applied to realise higher-order filter applications and it has been verified by simulations. The proposed circuits are expected to be useful in analogue filtering applications.

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References

1 WILSON, B.: 'Recent developments in current conveyors and current-mode circuits', *IEE Proc. G*, 1990, **137**, (2), pp. 63–77
2 SOLIMAN, A.M.: 'New generalized-immittance converter circuits obtained by using the current conveyor', *Int. J. Electron.*, 1972, **32**, pp. 673–679
3 SENANI, R.: 'Floating ideal FDNR using only two current conveyors', *Electron. Lett.*, 1984, **20**, pp. 205–206
4 HIGASHIMURA, M., and FUKUI, Y.: 'Novel method for realizing higher-order immittance function using current conveyors'. IEEE ISCAS'88, 1988, pp. 2677–2680
5 ISHIDA, M., HIGASHIMURA, M., FUKUI, Y., and EBISUTANI, K.: 'Synthesis of immittance function using current conveyors'. IEEE ISCAS'88, 1988, pp. 2681–2684
6 FABRE, A.: 'Third-generation current conveyor: a new helpful active element', *Electron. Lett.*, 1995, **31**, pp. 338–339
7 PIOVACCARI, A.: 'CMOS integrated third-generation current conveyor', *Electron. Lett.*, 1995, **31**, pp. 1228–1229
8 BHUSAN, M., and NEWCOMB, R.W.: 'Grounding of capacitors in integrated circuits', *Electron. Lett.*, 1967, **3**, pp. 148–149
9 LIU, S.I., TSAO, H.W., and WU, J.: 'CCII-based continuous-time filters with reduced gain-bandwidth sensitivity', *IEE Proc. G*, 1991, **138**, pp. 210–216

Dual-band circularly polarised microstrip antennas with a single feed

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Indexing terms: Microstrip antennas, Antenna feeds, Band-pass filters

The authors present a novel technique for obtaining circularly polarised (CP) dual frequency operation by using two spur-line band-stop filters within the perimeter of a microstrip patch antenna with optimum feed point location and aspect ratio. This circularly polarised dual frequency operation can be obtained without increasing either the size or the thickness of the patch. Furthermore, through several experiments the authors also demonstrate that the location of the feed point establishes and controls a trade-off between axial ratio and impedance bandwidth.