行政院國家科學委員會專題研究計畫 成果報告

適用 32 奈米以下製程之高產能、低成本平行寫入無光罩微影技術初步研究

研究成果報告(精簡版)

計 畫 類 別 ：個別型
計 畫 編 號 ：NSC 95-2218-E-002-045-
執 行 期 間 ：95 年 02 月 01 日至 95 年 10 月 31 日
執 行 單 位 ：國立臺灣大學電機工程學系暨研究所

計 畫 主 持 人：蔡坤諭

計畫參與人員：博士班研究生助理：劉俊宏
碩士班研究生助理：謝艮軒、田沛霖、王豪綜、游孟福

處 理 方 式 ：本計畫可公開查詢

中 華 民 國 96 年 01 月 31 日

Outline

Outline I
Abstract II
中文摘要 III
Research Method and Result ..... - 1 -
1. Electron Beam Solution ..... - 1 -
1.1. Beam Energy ..... - 1 -
1.2. Number of Source ..... - 2 -
1.3. Number of Column ..... - 3 -
1.4. Electron optical system (EOS) ..... - 4 -
1.5. Architecture ..... - 5 -
1.6. Writing Strategy ..... - 5 -
1.7. Data Transmission ..... - 6 -
2. Non-EB Solution ..... - 8 -
2.1. Zone-plate Array Lithography (ZPAL) ..... - 8 -
2.2. Optical Maskless Lithography (OML) ..... - 9 -
2.3. Near-field Lithography ..... - 9 -
2.4. Dip-pen Lithography ..... - 10 -
2.5. Focused Ion Beam Lithography (FIBL) ..... - 10 -
2.6. Nano-imprint Lithography (NIL) ..... - 11 -
2.7. Conclusion ..... - 11 -
3. Review ..... - 12 -
4. Appendices ..... - 13 -
Appendix A The MAPPER System ..... - 13 -
Appendix B Advantest's Multi Column Cell (MCC) System ..... - 14 -
Appendix C Canon's System ..... - 15 -
Appendix D KLA-Tensor's Reflective Electron Beam Lithography (REBL) System - 16 -
Appendix E Multibeam ..... - 17 -
Appendix F Lieca's Projection Maskless Lithography (PML2) ..... - 18 -
Appendix G Data Representation ..... - 19 -
Appendix H FPGA-based Data Buffer Board ..... - 22 -
Appendix I Data Compression ..... - 23 -
Appendix J Zone-plate Array Lithography ..... - 24 -
Appendix K Optical Maskless Lithography (OML) ..... - 26 -
Appendix L Near-field Lithography ..... - 27 -

Appendix M **Dip-pen Lithography** .... - 28 -
Appendix N **Focused Ion Beam Lithography** .... - 29 -
Appendix O **Nano-imprint Lithography** .... - 30 -
5. **Reference** .... - 32 -

Abstract

The rapid progress in microlithography technologies following Moore's law has been kept for half a century. The minimum half-pitch size has been reduced to 65nm and the exposure wavelength to 193nm. The immersion technique will be applied to 193nm scanners in the near future, which can extend optical lithography to 45nm node. According to the International Technology Roadmap for Semiconductors in 2006, the half-pitch size will shrink to 32 nm in 2012. However, there is no promising solution to extend traditional optical projection lithography (OPL) to 32-nm node and beyond.

Maskless lithography (ML2) has gained renewed interests as the cost and challenges of optical lithography masks increase. Major advantages of ML2 over OPL include reduced mask costs, reduced number of mask redesigns, and shorter mask cycle time. The requirements for ML2 are readily defined, but the implementation path is not necessarily obvious so far. In 32-nm node ML2 technologies, the data transmission rate is about several tens tera-bits per second, as is another challenge of ML2. To transfer and management this huge data from storage system to large number of E-beam writing element, we needs to design a dedicated data processing system.

This report is divided into two parts. The first part is to propose an e-beam based massively parallel maskless lithography (MPML2) system for 32-nm node next generation lithography (NGL). The second part we investigate several non e-beam ML2 technologies.

In the first part, we consider the primary parameters, beam energy, number of source, number of column, and electron optical system step by step, and discuss different structures in some tables. After comparing the advantages and the disadvantages of different parameters, we proposed our preliminary architecture, writing strategy, and data transmission system designs.

In the second part, we study six kinds of non e-beam ML2 technologies. They are Zone-plate Array Lithography (ZPAL), Optical Maskless Lithography (OML), Near-field Lithography, Dip-Pen Nanolithography (DPN), Focused Ion Beam Lithography (FIBL), Nano-imprint Lithography (NIL). All of them have capabilities of 32nm resolution patterning. We investigate their performances and then compared

their strength and weakness. At last, we identify the non e-beam ML2 technologies which have the most potential and feasibility to become a 32-nm bellow, NGL solution.

Keywords: lithography, maskless, e-beam, zone-plate, dip-pen, focused ion beam, near-field, nano-imprint

中文摘要

微影技術近半個世紀循著莫爾定律快速的發展，成像半間距已達 65 奈米，其曝光波長為 193 奈米。在運用浸潤式微影技術之後，193 奈米微影技術可用於 45 奈米。根據 2006 年國際半導體技術藍圖(ITRS)的資料，在 2012 年所需要的半間距長會縮小到 32 奈米。現今使用的傳統光學微影技術對於 32 奈米製程尚未有解決方案。

無光罩微影術因能克服尺寸的問題及可大幅減少光罩製成時間和成本而在近年來受到重視，但要將此技術應用到實際半導體生產尚有許多難題需要克服。電子束直接寫入技術即為一種極具潛力的無光罩技術，它的優勢在於高解析度及能深度聚焦。在３２奈米製程的無光罩微影術中，資料傳輸的需求到達每秒數十兆位元，這部分無疑的是其中一項艱難的挑戰，我們需要提出一種專門處理的資料傳輸系統。

這個計劃分成二個部份，第一部分提次世代３２奈米製程大量平行電子束無光罩微影系統的初步架構設計。第二部分研究分析數種非電子束無光罩微影技術。

在第一部分中，我們對主要的結構型態逐項進行分析，包括電子束能量、電子源數目、腔體數目、和電子光學系統。在比較不同規格的優缺點後，我們提出初步的系統架構、寫入策略和資料傳輸系統設計。

在第二部分我們研究六種非電子束無光罩微影技術，包括波帶板陣列微影術、光學無光罩微影術、近場微影術、探針式微影術、離子束微影術和奈米壓印微影術。這些技術都有達到３２奈米製程的能力。我們分析這些技術的優缺點並推斷出其中最有潛力與可行性的非電子束微影技術。

關鍵字：微影、無光罩、電子束、波帶板、探針式微影、離子束微影、近場光微影、奈米壓印

Research Method and Result

1. Electron Beam Solution

In the first part, we propose a micro-technology based MPML2 system to compete with other multiple EB systems. In order to find a proper and achievable schematic of our MPML2 system, we evaluate the advantages and disadvantages of four primary parameters in multiple EB system structure. They are beam energy, number of source, number of column, and electron optical system (EOS) types. These evaluations are made via literature survey and simulation. After evaluations, we propose our MPML2 schematics and the writing strategy and data transmission systems are also proposed.

As Table 1 shows, several promising EB-ML2 systems are summarized with the respects of # f beam, source, column, voltage, and EOS types. (see Appendix A, Appendix B, Appendix C, Appendix D, Appendix E, and Appendix F)

	# of beams	source	column	voltage	EOS
MAPPER	13,000 (DW)	single	single	5 keV	E
ADVANTEST (MCC)	16 / 64 (DW / VSB)	multiple (1 per CC)	single (multiple CC)	50 keV	E & M
Canon	4,096 (DW)	single	single	50 keV	E & M
KLA-Tensor (REBL)	8000*500 (projection)	single	single	50 keV	E & M
Multibeam	10 (DW)	multiple	multiple	50 keV	E
Leica (PML2)	290,000 (projection)	single	single	5->100 keV	E & M

Table 1 Summary of six EB-ML2 technologies

1.1. Beam Energy

Generally, beam energy exceeding 20keV is defined to be high. The advantages and disadvantages of high/low voltage system are summarized in Table 2.

High	Advantages	(1) It has higher resolution, because there are less forward-scattering electrons which broader the spot size. (2) It produces vertical side-wall profile, due to less forward-scattering electrons.
	Disadvantages	(1) It generates more heat on the wafer due to higher electron energy. (2) High energy electrons tend to penetrate through resist layer and hit the layers below. (3) It needs larger lens system to drive large electrostatic or magnetic field for imaging.
Low	Advantages	(1) It limits the penetrating depth of electron beam. (2) It can reduce the proximity effect due to less backscattering electrons.
	Disadvantages	(1) It produces more forward-scattering electrons and result in poorer resolution and side-wall profile. (2) It needs thin resist layers because electrons penetrate less depth.

Table 2 Comparison of high-energy & low-energy systems

Most of EB-ML2 systems in table choose high accelerating voltage beams, so all of them have to drive large voltage or current at the focusing or projecting optical systems. We choose low voltage for our system. One reason is that it's easy to implement tiny EOS in micro fabricating process. The other is to avoid risks of heat and damage of lower layers.

1.2. Number of Source

Source is the device which emits electrons. Single-source and multiple-source systems are discussed in Table 3.

Single	Advantages	(1) It is easy to implement for the scale of source is almost unlimited. (2) It is easy to maintain or replace.
	Disadvantages	(1) It is hard to achieve very high current density and brightness requirement of mass production. (2) Unwanted current loss happens at the beam splitting units.

Multiple	Advantages	(1) It can loose the requirement of current density and brightness by increasing source numbers. (2) It reduce the possible current loss at beam splitting units.
	Disadvantages	(1) It is hard to control beam uniformity of sources. (2) It is hard to maintain and replace the failure units if the source number is quite large.

Table 3 Comparison of single-source & multiple-source systems

Current density and brightness are the most critical challenge in EB-ML2 systems. To achieve high throughput expected, sufficient high current density and brightness are needed. Here we simply evaluate our multi-beam system with 5kV accelerating voltage and 10 wafer/hr throughput in 300mm wafer. Consequently, 196uA of emitting current is needed; this is quite high for available commercial source types. Moreover, we evaluate the source brightness at the conditions of 10,000 beams, 1° converging angle, and 2 nm focusing spot diameter. The calculation results in about $2 \times 10^{8} A/cm^{2}sr$ brightness requirement. Actually, this value should be higher because we must add apertures to limit aberrations and this introduce additional current loss. Amount the source available, this brightness requirement is hard to achieve with the additional consideration of stability and life-time.

We choose multiple sources structure in order to overcome the challenge of brightness. Multiple sources also can reduce the emitter unit size and make it easy to integrate to the micro-column structure via micro-fabricating process.

1.3. Number of Column

Column is the vacuum space in which the EOS operates. Single-column and multiple-column systems are discussed in Table 4.

Single	Advantages	(1) It needs to implement only one set of vacuum system. (2) It can save more space to integrate more beamlets.
	Disadvantages	(1) It is hard to integrate individual control or EO unit for a single beam when the number of beam is quite large. (2) Function of whole system will be affected if there is one failure beam.
Multiple	Advantages	(1) It is easy to maintain and replace when there is a failure beam. (2) It could have various writing strategies if the columns

		are allowed to move individually.
	Disadvantages	(1) It is hard to control column-to-column uniformity. (2) It spends more space. (3) The structure will be more complicated if the columns are allowed to move individually.

Table 4 Comparison of single-column & multiple-column systems

Single-column scheme is preferred, because we expect to achieve sufficient throughput with a huge number of beams. Generally, there is only single pattern to be exposed on a wafer, so we think multiple-column scheme is of no need, and as introduces complexities in structure and writing strategy.

1.4. Electron optical system (EOS)

EOS consists of lens system, blanking system, and deflecting system. There are two type of EOS, one is electrostatic type and the other is magnetic type. The advantages and disadvantages of two lens types are summarized in Table 5.

Electrostatic	Advantages	(1) It spends less space for electrodes implementation. (2) Electrode implementation is simpler than that in coil and polepieces, especially in micro-process. (3) It has faster switching time than magnetic lenses.
	Disadvantages	(1) It suffers worse aberrations. (2) It has weaker focusing and deflecting capabilities. (3) Electrode shape should be carefully designed and manufactured to prevent breakdown when applying high voltage.
Magnetic	Advantages	(1) It has stronger focusing and deflecting capabilities. (2) It has better aberration control.
	Disadvantages	(1) It spends more space to integrate coils and polepieces in the lens system. (2) It is hard to minimize the lens into micro-scale. (3) It generates heat during operating and need cooling systems.

Table 5 Comparison of electrostatic & magnetic EOSs

We select a full-electrostatic EOS for the reason that it is fit for micro-scale process. Due to the dense beamlets configuration of our MPML2 system, the deflecting distance is as small as several microns, thus electrostatic deflector is

sufficient. We also need the deflecting and blanking system to operate in the frequency of several to several tens of MHz, so electrostatic devices are preferable.

1.5. Architecture

After the discussion above, architecture of our MPML2 system can be proposed. As Figure 1 shows, electrons are emitted from micro tips and pass through the micro-lens system. Like common EBL systems, the beam switches on and off by a blanker and scans orthogonally to the motion of stage by the deflector. We propose to add a set of detector and stigmator to check and correct the beam position.

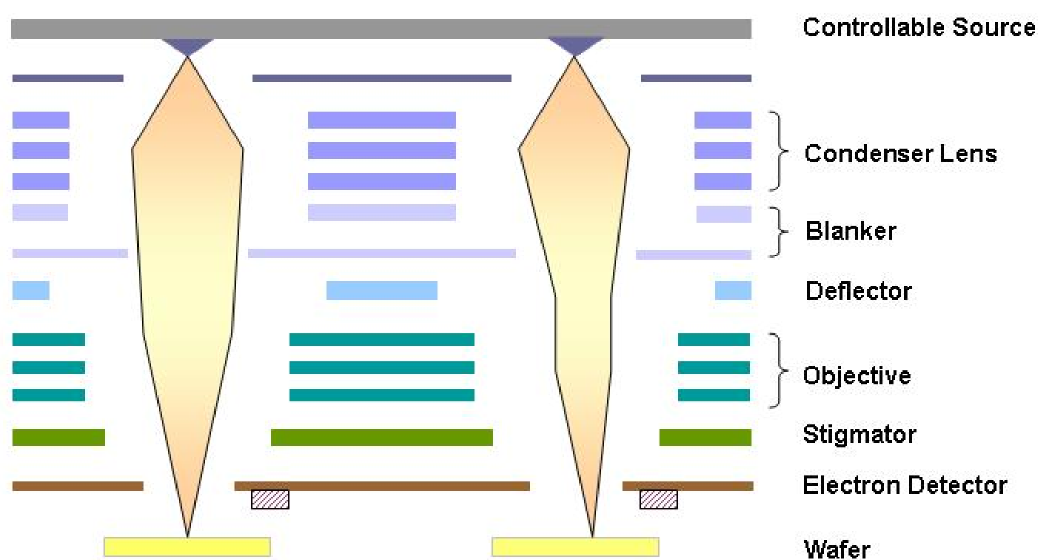

Figure 1 Schematic of MPML2 column

1.6. Writing Strategy

Writing strategies is mainly determined by beam configuration and the field size of single exposure. Electron beams can be mapped into a row or matrix of any shape. In order to limit beam-to-beam interactions, separation of neighboring beams is needed. However, the sufficient separating distance is still left unknown.

We prefer to apply MAPPER's writing strategy to our MPML2 system. As figure 2 shows, the beamlets are mapped into oblique rows. In a single row, beamlets are separate in a fix distance, which is the minimum distance ensuring ignorable interaction. The next neighboring row is placed in the same minimum distance from the former, and a deflecting length shift is introduced to ensure that all the scanning fields are different. The stage travels a raster route and scanning all area of wafer.

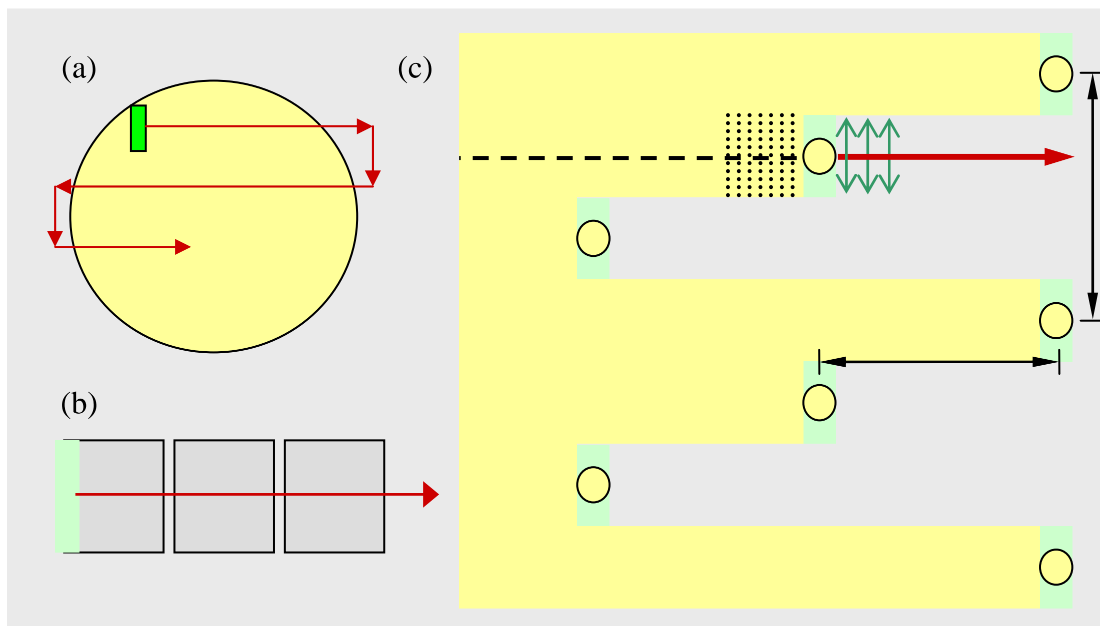

Figure 2 Writing strategy in the point of view of (a) wafer, (b) dies, and (c) beams

1.7. Data Transmission

E-beam based maskless lithography is an extremely potential technology to be the main technique in next-generation lithographic technique. One of the critical problems needs to be solved is data management and transmission. As the semiconductor manufacturer half-pitch is getting smaller, the layout data which define the chip structures and figures is getting larger. In 32-nm half pitch size, the whole layout data in one wafer is arrive at hundred of tera-bits. In today's traditional optical lithography, the throughput is 60 wafers per hour. Therefore the transmission rate is about several ten tera-bits per second (Table 6). To transfer and management this huge data from storage system to large number of E-beam writing element, we needs to integrity design a dedicated data processing system. The data processing system should consider

- Data transmission rate
- Flexibility in processing different data formats
- Flexible Proximity Effect Correction
- Conversion speed [13]

Device specifications		Direct-write specifications	
Minimum feature	32nm	**Pixel size**	16nm

Edge placement	<1nm	**Pixel depth**	6 bits/64 gray
Chip size	10 mm×20 mm	**Chip data (one layer)**	4.68 Tb
Wafer size	300mm	**Wafer data (one layer)**	1680 Tb
Writing time (one layer)	60 s	**Data rate**	28.8 Tb/s

Table 6 Data specifications in pixel type format

It is an important issue to choose the data representation. It affects the data size directly. In this project we consider of hierarchy, vector, pixel, and hybrid format. If the layout figures are all polygon, the data size of vector type data will be ten times smaller than pixel data. However, if consider to electrical beam proximity effect, the data size will increase enormously. Therefore, we propose a new data format: pixel and vector hybrid format. (see (7)Appendix G)

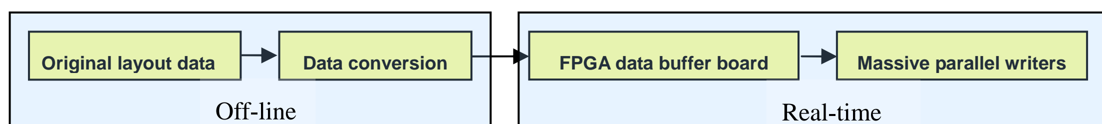

Figure 3 Data path architecture

The basic design of a data processing system capable of delivering tera-pixel data rate necessary to achieve next-generation maskless lithography is shown in Figure 3. This design consists of storage disks, a FPGA based data buffer processor board with memory (Figure 4) (see (7)Appendix H).[14] A heavily interconnected set of two Virtex-II Pro FPGAs makes up the core element of the buffer system. Each FPGA comprises various configurable elements and embedded blocks optimized for high-performance system designs.[15] The original layout data transfer to hybrid including pixel and vector type data. This hybrid data needs to be compressed by lossless compression method (see (7)Appendix I) [16] [17] and stored in the storage disks (RAID system). The action up to above can be done in off-line. Before the writing process begins, a single layer compressed data is transferred from disks to the FPGA based data buffer processor board. As the writers write a stripe across the wafer, compressed data is streamed from the processor board to the writers chip inside a vacuum column in real-time. The compressed data is decompressed by writers chip and control the blanker on or off.

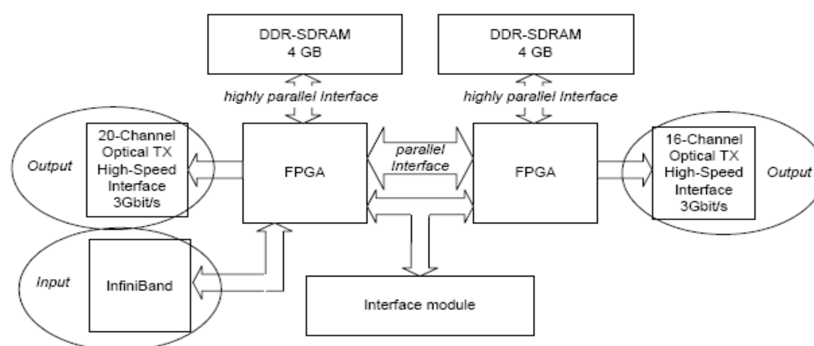

Figure 4 Data buffer architecture for high throughput

To summarize our preliminary data processing system in MPML2, we choose hybrid type data format and store them in RAID system after compress losslessly. The compressed data through FPGA based high speed data management and data transmission buffer board to achieve the enormous transmission rate.

2. Non-EB Solution

In the second part, we evaluate the strength and weakness of six kinds of ML2 systems. They are zone-plate array lithography (ZPAL), optical maskless lithography (OML2), near-field lithography, dip-pen lithography, focused ion beam lithography (FIBL), and nano-imprint lithography (NIL). All of them are under developed for many years, and also has possibilities to become the mainstream technology of wafer production.

2.1. Zone-plate Array Lithography (ZPAL)

ZPAL, developed by Nanostructures Laboratory of MIT, is an optical direct write technology, which utilizes micro-scale zone-plate array and switching mirror array to generate huge numbers of focused beams and expose the whole wafer. The strength and weakness of ZPAL is summarized in Table 7. (see (7)Appendix J)

Strength	➢ With zone-plate technology, ZPAL can be extend to use EUV or x-rays which tend to pass through conventional lenses. ➢ Resolution enhancement techniques which are used in optical lithography can be applied to ZPAL, such as immersion technique.
Weakness	➢ The transmission of zone-plate is merely 40%. ➢ In order to get high throughput and clear pattern, switching

	mirrors should tilt sufficiently fast, and the tilting angles should be controlled precisely. ➢ To achieve 32nm line width, wavelength should be reduce to EUV (13.5nm). Then it will face most of the problems of EUV lithography, such as source life-time, no available resist, multi-coated mirror accuracy, and so on.

Table 7 Strength & Weakness of ZPAL

2.2. Optical Maskless Lithography (OML)

OML, developed by ASML, replaces photomasks by a dynamic pattern generating device called spatial light modulator (SLM) which consists of 1.048M micro-mirrors. With the mirrors tilt or lift, intensities and phases of small patterns can be adjusted, and the whole pattern is imaged to the substrate through high demagnification projection lens. The strength and weakness of OML is summarized in Table 8. (see Appendix K)

Strength	➢ Advances in conventional mask-based optical lithography can be applied to OML, such as resists and RETs.
Weakness	➢ It is hard to control the uniformity of 1.048M mirrors. ➢ To achieve 32nm line-width and below, wavelength should be reduce to EUV (13.5nm). It will face most of the problems of EUV lithography, such as source life-time, no available resist, multi-coated mirror accuracy, and so on.

Table 8 Strength & Weakness of optical maskless lithography

2.3. Near-field Lithography

By approaching the resist surface within the distance of one wavelength, the electromagnetic distribution would be quite different than that under far-field condition. It can be used for optical lithography to surmount diffraction limit. The strength and weakness of near-field lithography is summarized in Table 9. (see Appendix L)

Strength	➢ There is no more diffraction limit, so high resolutions can be obtained by using long wavelength light. ➢ Because the structure of waveguide is simple, it is easy to make a dense beamlets array.

Weakness	➢ For the waveguide is extremely close to the resist, it is hard to control contaminations and damages. ➢ The energy passing through the waveguide is quite low and would reduce the exposure speed of the system. ➢ Depth of focus of near field light is short.

Table 9 Strength & Weakness of near-field lithography

2.4. Dip-pen Lithography

Dip-Pen Nanolithography (DPN) is a scanning probe nanopatterning technique in which an AFM tip is used to deliver molecules to a surface via a solvent meniscus, which naturally forms in the ambient atmosphere. The strength and weakness of dip-pen lithography is summarized in Table 10. (see Appendix M)

Strength	➢ It creates nano-structure in on step without resist. ➢ It is possible to achieve sub-10nm line-width. ➢ A in-situ position detection can be performed during lithographic process, and this ensure the alignment and leveling accuracy.
Weakness	➢ The throughput is quite low compared to other lithographic technologies. ➢ The AFM tip is too close to wafer surface, and this induce the risk of unwanted contaminations and tip breakdown.

Table 10 Strength & Weakness of dip-pen lithography

2.5. Focused Ion Beam Lithography (FIBL)

FIBL is similar to EBL in applications, feature sizes and the fact that it is a serial approach, but uses a beam of ions instead of electrons. A fundamental difference is that ions are charged atomic that can interact physically and chemically with, and settle into, the exposed material, and the particles of which are many orders of magnitude more massive than electrons. The strength and weakness of FIBL is summarized in Table 11. (see Appendix N)

Strength	➢ It can generate high-aspect ratio patterns. ➢ It induces less back-scattering particles than EBL, so it suffers less proximity effect. ➢ It has the possibility of building up structures rather than just

	creating structures destructively.
Weakness	➢ Ion source requirements of low energy spread and high brightness are hard to achieve. ➢ Swelling occurs when developing negative resists and as limits the resolution. ➢ Ions, with thousands times of mass compared to electrons, cause more damage to resist and lower layer structures. ➢ The ions, which lose energies and stays in the substrate, may serve as doping particles and effect the performance of circuits.

Table 11 Strength & Weakness of FIBL

2.6. Nano-imprint Lithography (NIL)

NIL makes a 1:1 pattern transfer from mold to resist. There are three types of resist to use, one can be direct printed, and another should be heated to be soft, and the other should be exposed to cure by UV light after printing. The strength and weakness of NIL is summarized in Table 12. (see Appendix O)

Strength	➢ It performs a fast and low-cost lithographic process. ➢ It has a possibility to print a whole wafer at one time.
Weakness	➢ The 1:1 mold preparation is time consuming and relies on some other high resolution, high throughput ML2 technologies. ➢ The printing uniformity is hard to control, especially in the side region of the mold. ➢ Damage and contamination happen easily in repeated printing process.

Table 12 Strength & Weakness of NIL

2.7. Conclusion

After the discussion above, we conclude that OML and ZPAL are more competitive than all the other technologies. The main reason lies in the abilities of contamination and damage control, as is important for repeated wafer manufacturing process. FIBL is a versatile technology but introduce more possibility for damage

and contamination (ex. doping particles) during the process. In near-field and dip-pen technologies, the gap between resist and writing units are so close that it requires extremely high accuracy of resist thickness control or scan leveling control. Nano-imprint technology uses the contact mold and would suffer more contamination and damage problems.

The potentials of OML and ZPAL for 32nm node manufacturing rely on the extension to EUV. Recently, with large quantity of research and investigations, EUV technologies have many progresses, especially in source and optics. These progresses also benefit OML and ZPAL and help them become more realizable.

3. Review

(1) We finished preliminary studies about architectures, writing strategies, and data preparation techniques of EB and non-EB ML2 systems.

(2) We proposed low-energy, single-column, multiple-source, and full-electrostatic MPML2 system, and the architecture and writing strategy were designed.

(3) Preliminary studies about data transmission process of MPML2 system was done, and we proposed a new concept about hybrid data format.

(4) We proposed a FPGA based data buffer board to management and transmission the enormous data.

(5) We investigated the non-EB ML2 techniques and proposed one is the most potential non-EB technique in next generation lithography (NGL).

(6) To summarize this project, it is conform to our proposal approximately, and achieve our original objective rudimentary.

(7) The results of this preliminary study will be essential for a 3-year (2006-2008) NSC project, “Design of E-beam Based Massively Parallel Maskless Lithography Systems”, which is to develop a MPML2 prototype with high performance, low cost, and high throughput. It will be extremely advantageous for Taiwan’s competence in IC manufacturing.

4. Appendices

Appendix A The MAPPER System

MAPPER Lithography BV is founded in 2001 by scientists in Delft University of Technology. The MAPPER system uses 13,000 beamlets simultaneously writing patterns on wafer at 5keV. A bundle of electrons emitted from one high current source are guided to massive aperture array to generate 13,000 beamlets. Beamlets are switched on and off by electrostatic blanker array, and passing through the deflecting and focusing lens array at the last stage. To form a scanning field of 26× 10mm^2, the beam spots are arranged in a 200×65 array. The deflecting width of an individual beam is 2um. The MAPPER system aims at throughput about 10 300mm wafers per hour in 32nm node and it's still under developed.[1][2][3]

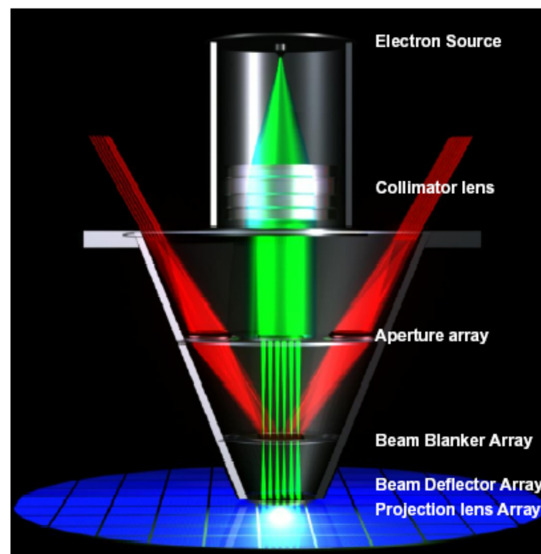

Figure 5 Schematic of MAPPER system[1]

Appendix B　Advantest's Multi Column Cell (MCC) System

Advantest, one of the leaders of semiconductor test equipment, proposed their multiple-column electron beam lithography called MCC systems. CC is a tiny column witch only drives one 50keV high energy beam. Unlike other systems focused on the direct write technique, Advantest designed to apply character projection (CP) to their MCC system. CP technique prepares about 200 types of patterns on the CP aperture masks and images the patterns selected onto the wafer through the demagnification projection lenses and deflectors. The alpha-tool has a 4 ×4 CC array and focuses on 65nm mask production. Advantest plans to combination of CP technology with variable shaped beam (VSB) and forming a new writing strategy of variable character projection (VCP). The throughput and capability of patterning will be extended by applying VCP technologies.[4][5][6]

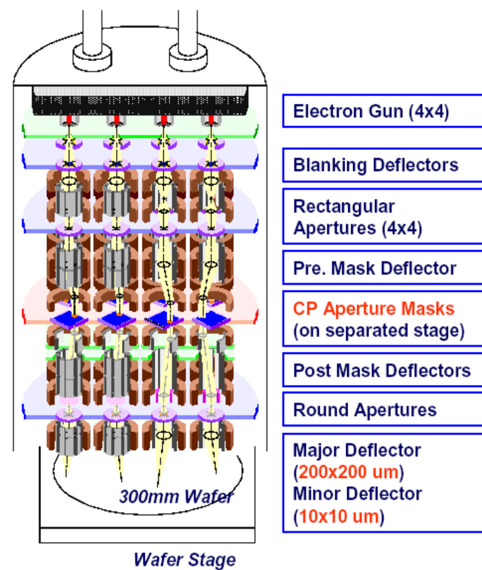

Figure 6　Schematic of MCC system[6]

Appendix C Canon's System

Canon, who is one of the three leaders of lithographic equipment, proposes a 4096 multiple e-beam system which drives at 50keV beam energy. Electrons emitted from one thermionic source are split into 4096 beamlets by an aperture array. Deflectors and blankers are integrated below the apertures. A distinct layer named correction lens array (CLA) is attached, in order to correct field curvature induced from the lens systems. This system can expose a 4×4mm^2 field at one time, each beam has a 4um deflecting width. Canon's system is under development, and the official data of throughput evaluated is 56 200mm wafers per hour, which is unrealistic for mass production.[7]

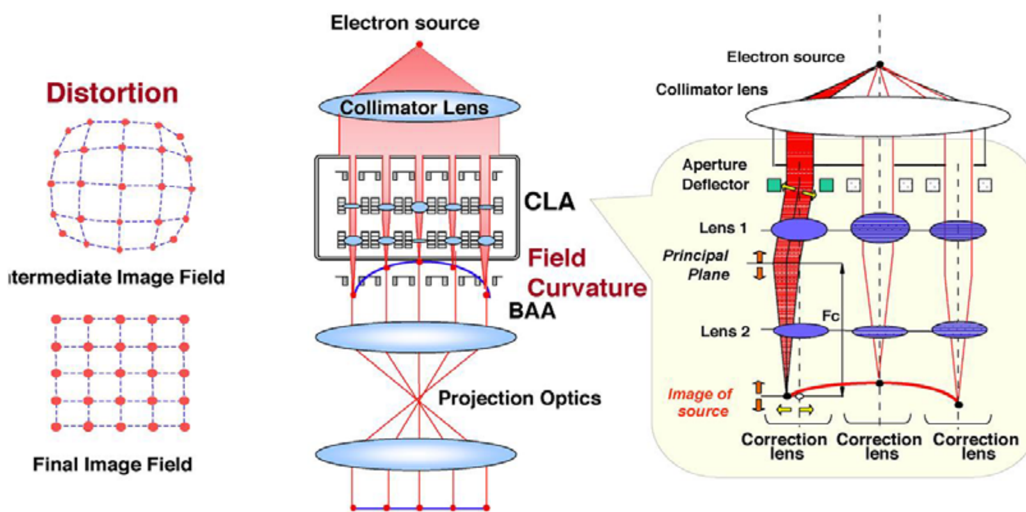

Figure 7 Schematics of Canon's System[7]

Appendix D KLA-Tensor's Reflective Electron Beam Lithography (REBL) System

KLA-Tensor is one of the top semiconductor equipment suppliers. They propose a multiple e-beam system which use digital pattern generator (DPG) to generate the desired pattern. DPG consists of 8,000x500 electron mirrors. A bundle of 50keV electrons passing through the magnetic prism are guided to illuminate the DPG. DSG which consists of array of electrodes can be tuned by changing the driving voltages, and distribution of reflected electrons is modified. Then the modified distribution is demagnified and project to the wafer. Minimum line-width on wafer is about 22.5nm. Throughput of REBL is about 5 300mm wafers per hour. KLA plans to deliver a beta tool in 2007.[8]

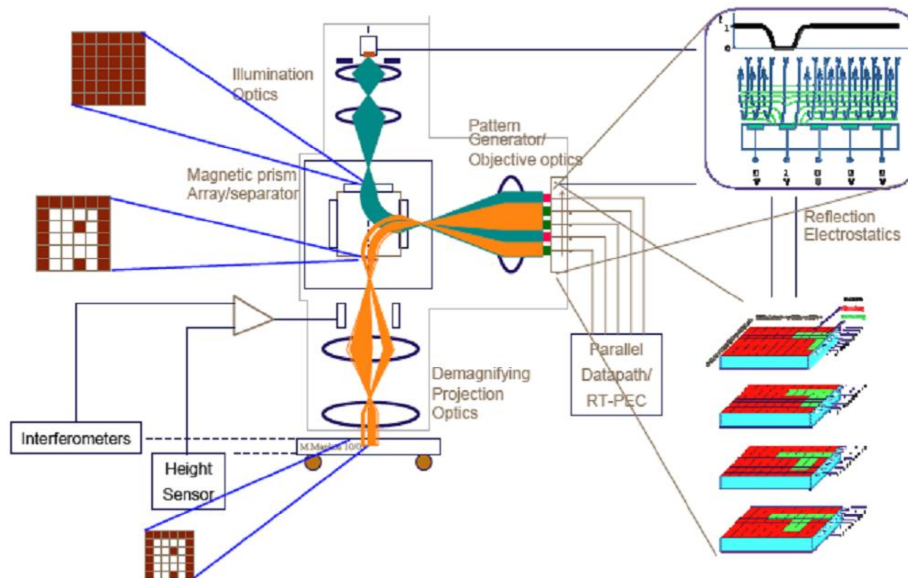

Figure 8 Schematic of REBL System

Appendix E　Multibeam

A new company Multibeam proposes their ML2 solution based on the concept of vector shaped multibeam (VSM). The Multibeam system consist of a monoblock of a 10×1 micro-columns array on 30mm centers. Each micro-column has a thermal field emitter, and scans a stripe of 25×2um^2. Electrons emitted hold 20keV energy and are accelerated to 50keV at the final part of the column. Each beamlet is square-shaped and by adjusting the focusing magnification, a variable size of square beam is obtained. Currently, the official data of throughput evaluated is about 5 300nm wafers per hour at 45nm node.[9][10]

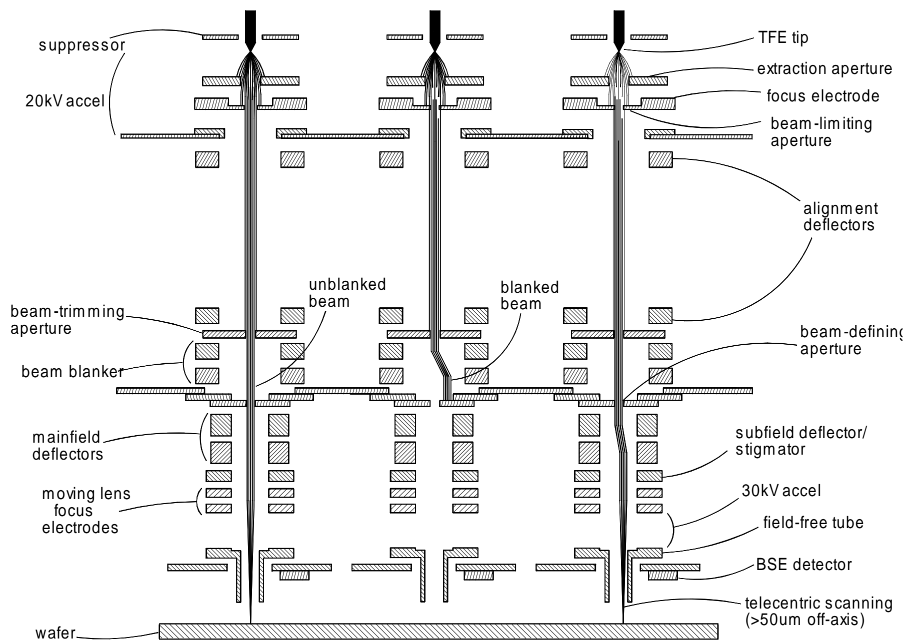

Figure 9 Schematic of Multibeam System[10]

Appendix F Lieca's Projection Maskless Lithography (PML2)

Lieca is one of the leaders of optical equipment supplier and propose a e-beam based projection maskless lithography (PML2) system. In PML2, patterns are formed with a dynamic variable aperture array called aperture plate system (APS). 5keV electrons pass through the APS and the patterns generated are 200x demagnified, and accelerated to project onto the wafer at 100keV energy and 25nm spot size. The throughput evaluated is about 5 300mm wafers per hour at 45nm node, and the beta tool is planned for 2008.[11][12]

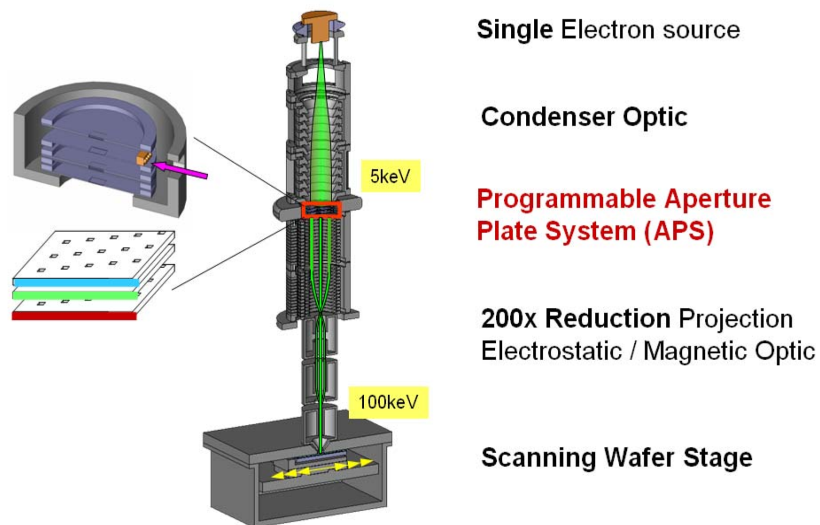

Figure 10 Schematic of PML2[12]

Appendix G Data Representation

The appropriate choice of data representation is an important issue. The data format of original layout data is called Graphic Data System (GDS or GDSII). GDSII Stream format is the standard file format for transferring 2D graphical design data. It contains a hierarchy of structures, each structure containing elements such included polygons, polylines, and structure references. The hierarchy file can transfer to vector type file. And vector type file can further transfer to pixel file. The data size of the hierarchy is smallest, and the pixel file is biggest. However, the e-beam writers need to receive the pixel file. We should consider these three kinds of representations, hierarchical, vector, and pixel, need to define what kind of data type we choose to use.

1. Pixel type format

Pixel type is most widely used in mask-writer. We roughly calculate the data size in pixel type format.

Device specifications		Direct-write specifications	
Minimum feature	32nm	Pixel size	16nm
Edge placement	<1nm	Pixel depth	6 bits/64 gray
Chip size	10 mm×20 mm	Chip data (one layer)	4.68 Tb
Wafer size	300mm	Wafer data (one layer)	1680 Tb
Writing time (one layer)	60 s	Data rate	28.8 Tb/s

Table 13 Direct-write specifications

Table 13 presents relevant specifications for devices with a 32nm minimum feature size. To meet these requirements, the corresponding specifications for a direct-write pixel-based lithography system are shown on the right side of Table 13. The minimum feature size of 32 nm requires the size of 16 nm pixels. Sub-nanometer edge placement can be achieved using 6-bit gray pixels.

A 10 mm ×20mm chip can represents $\frac{10mm}{16nm} \times \frac{20mm}{16nm} \times \frac{6bits}{pixel} \simeq 4.68Tb$ of data per chip. A 300mm wafer containing 350 copies of the chip, results in 1365 Tb of data per layer wafer. Therefore, to expose one layer of an entire wafer in one minute requires a throughput of $4.68Tb \times 350 / 60\,seconds \simeq 28.8Tb/s$. In this data format, the compression and decompression element is necessary. Pixel data needs to compress to decrease the data size. As the compressed data transfer to the writers, compressed data needs to decompress by decoder chip.

2. Vector type format

Fig. 11 data representation for vector and pixel

Vector type of data representation is a more efficient way to pixel type. For a simple graph as Figure 11, it only needs three polygons to describe, instead of a lot of pixels. We calculate the data size of vector type data is about ten times smaller than pixel data for a 32 nm half-pitch ordinary layout file.

In vector type format, we need a data transfer chips in the writers to transfer data from vector format to pixel format. If the polygon of layout data contains more pixels, the efficiency of vector type data is much better. However, the proximity effect is a big problem for vector type data. As the half pitch gets smaller, the proximity effect will get serious. In this saturation, we need use some correction method to redefine the layout data. The figure of layout will be change and the edge of figure will be distortion. The effect will make the size of vector type format get larger.

3. Hybrid data format

We can combine the advantage of vector type and Pixel type to create a new approach. We can use vector type to describe simple polygon part of layout data, and use pixel type to describe the other part (Figure 12). For a polygon, it needs four parameter to define, the position X, Y, width and length (W, L), if W and L are smaller than some given value, it means that is not efficient to describe graph in vector type, then we can use pixel type to present the rest graph. Here we use 57 bits to describe a polygon, if one polygon is containing less than 57/5 = 12 pixels, vector type is not efficient. So if W*L is smaller than 12, vector type is not efficient

anymore. For the graph of layout data after proximity correction, it becomes more complex than the original layout data. In this situation, Hybrid approaches may be a good solution. However, in hybrid format, we also need a data transfer chips in the writers to transfer data from hybrid format to pixel format. The implementation of the hybrid data format needs to be further considered.

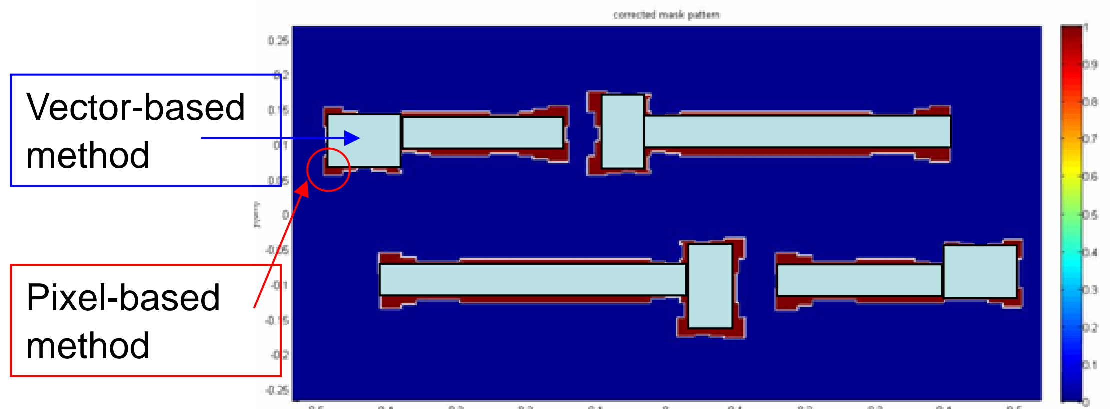

Figure 12　Diagram for hybrid data format

Appendix H FPGA-based Data Buffer Board

The field programmable gate array (FPGA) based data buffer for management and data rate is used in design for high speed lithography system. The processing and transfer of the enormous data volumes required to parallel switch the individual apertures on the programmable blanker, thus defining the chip patterns. It is a challenge to sets high demands on the data processing and the whole data path requiring data rates in the gigabit/s and even terabit/s range. The requirements for the data buffer including storage capacity, throughput, incorporation of data re-arrangements and transmission coding, error detection, and appropriate interface solutions. The figure of data buffer architecture for high throughput and data buffer hardware is in Figure 13 and Figure 14.

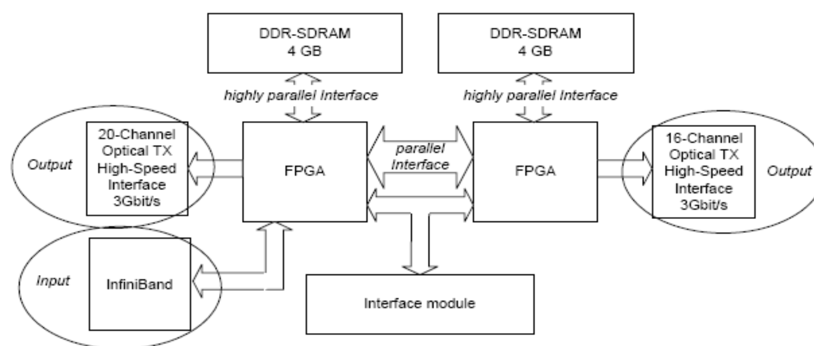

Figure 13 Data buffer architecture for high throughput[14]

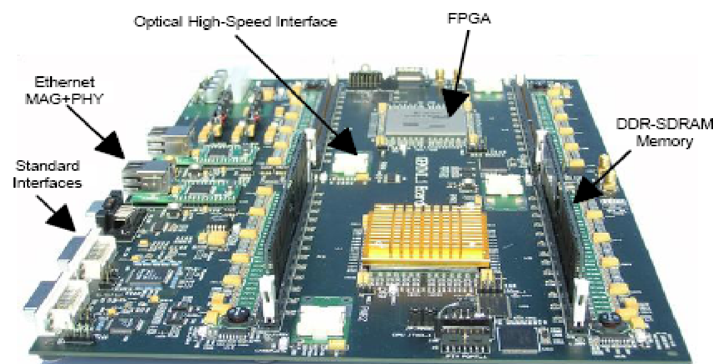

Figure 14 Data buffer hardware (16-layer PCB)[14]

Appendix I Data Compression

Data compression is an effective method for saving storage space and transmission bandwidth. The compression scheme must be lossless for the layout figure can't be changed. The compression algorithm has to adapt to the changes in the data structure to make the compression ratio as big as possible. Meanwhile, the implementation of the compression and decompression must be minimizing memory and power. The trade-off between processing complexity and real-time ability hardware implementation need to be further research. Recently a novel lossless compress technique called Context-Copy-Combinatorial-Code (C4). The C4 is designed dedicated for pixel format layout data. Although it can't use in hybrid format data, but its algorithm is worth to investigate for our further research in data format chosen.

Appendix J Zone-plate Array Lithography

1. Introduction to Zone-Plate-Array Lithography

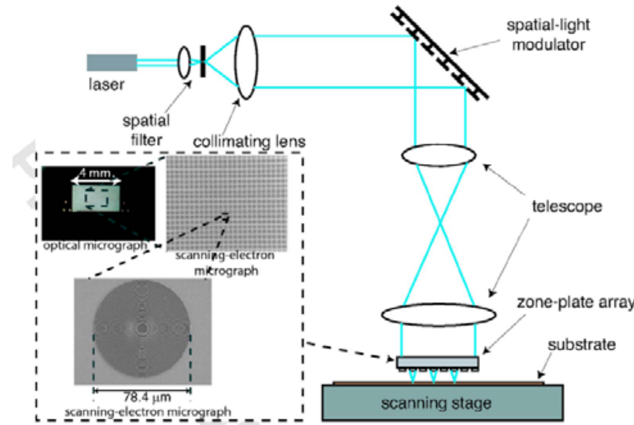

Figure 15 Schematic of ZPAL system[18]

In Zone-plate-Array Lithography system, a zone-plate array is used to create an array of tightly focused spots on the photoresist-coated surface of a substrate. By modulating the light intensity incident on each zone plate by means of an upstream spatial light modulator (SLM) while scanning the substrate, one can write patterns of arbitrary geometry in a dot matrix fashion.[18][19]

An array of Fresnel zone plates focuses incident radiation into an array of spots on a substrate. The spot size is approximately equal to the outer zone width of the zone plate. By means of micromechanics, incident light is split into multiple beamlets and can be switched on and off. The beamlet turn on is reflected to the zone plate and simultaneously scanning the substrate in a raster route.[20]

The throughput of ZPAL system can be evaluated by the following equation:

$$T_{total} \propto \frac{WaferDiameter^2}{\left(OZW^2\right)\left(\#\ ofZonePlates\right)},$$

where T_{total} is the time in seconds and the OZW is the outer zone width. The throughput in terms of wafers per hour is simply $\frac{Wafers}{Hour} = \frac{3600}{T_{total}}$, and decreasing the minimum feature size (i.e. OZW) by a factor of 2 decreases the throughput by a factor of 4. If the number of Zone Plates is increased, the throughout of wafer becomes very large.

Currently, ZPAL utilizes 193nm wavelength light, and achieve a minimum feature size of . To achieve the resolution of 32nm or below, light wavelength should be reduced below 193nm, even below 157nm. Here we evaluate the

capability of ZPAL with EUV source. We calculate the resolution from the resolution equation: $W_{min} = k_1 \times \frac{\lambda}{NA}$, with 0.8 k_1 and 0.7 NA, and 13.5nm wavelength. About 15nm resolution is obtained.

2. SLM

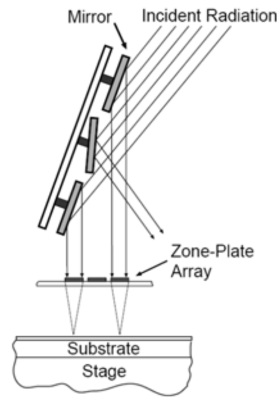

Figure 16 Manufacturing process of zone-plate

As figure shows, SLM consists of micro-mirror array in the path of the radiation. With accurate alignment and tilting angle adjustment, each mirror will be responsible for the illumination of an individual zone plate.

3. Fabrication of UV Zone Plates

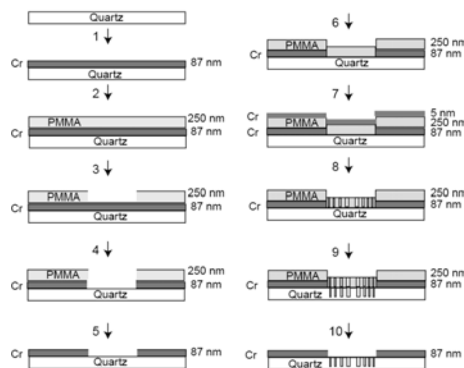

Figure 17 Manufacturing process of zone-plate

The main steps of the process are the following:

1. Defining the areas in which the zone plates are going to be placed.
2. Surrounding these areas with a Cr layer of the thickness calculated in the last section.
3. E-beam writes the actual zones inside the clear circles.
   Reactive ion etch the wafer to provide the desired π phase shift.[21]

Appendix K Optical Maskless Lithography (OML)

ASML is one of the three leaders of lithographic equipment suppliers, and they proposed their optical ML2 solutions -- OML. OML system is different from conventional optical lithographic scanner in the mask stage. OML technology replaces the mask by a spatial light modulator (SLM), which consists of 512x2048 adjustable micro-mirrors. Each micro-mirror can be tilt or lift to introduce intensity loss or phase shift of the incident light. Hence, desired patterns can be generated by the SLM, and then demagnified and imaged onto the wafer. Currently, OML aimed at 65nm and 45nm node and utilize 193nm wavelength DUV. Throughput evaluated is about 5 300mm per hour.[22][23][24]

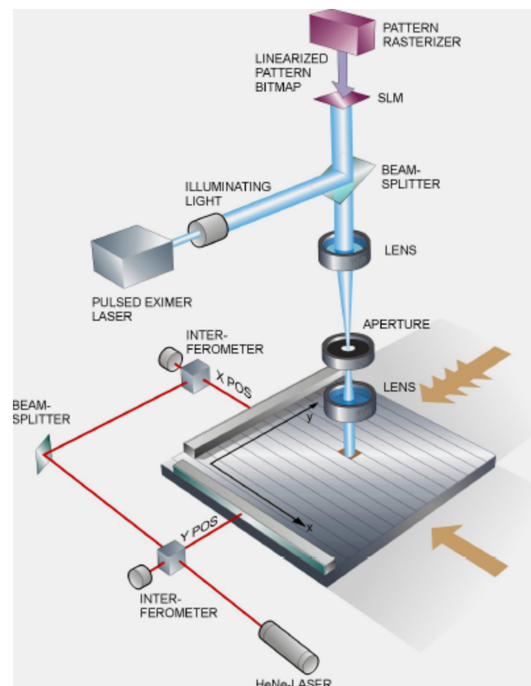

Figure 18 Schematic of OML system[22]

Appendix L Near-field Lithography

Under the near-field conditions, the local electromagnetic fields that exist around dielectric and metallic nanostructures can be used to circumvent the diffraction limit. Near-field lithography utilize some material and / or structure as a waveguide and place the waveguide extremely near to the resist, even contact with it, to write high resolution patterns.

A new approach that can potentially produce sub-wavelength structures uses broad beam illumination of standard resist with visible light. This method is based on the plasmon resonance occurring in nanoscale metallic structures. When a metal nanoparticle is placed in an optical field, it exhibits a collective electron motion known as the surface plasmon oscillation. This can result in strongly enhanced electrical fields near the particle when the excitation occurs at the resonance frequency.[25]

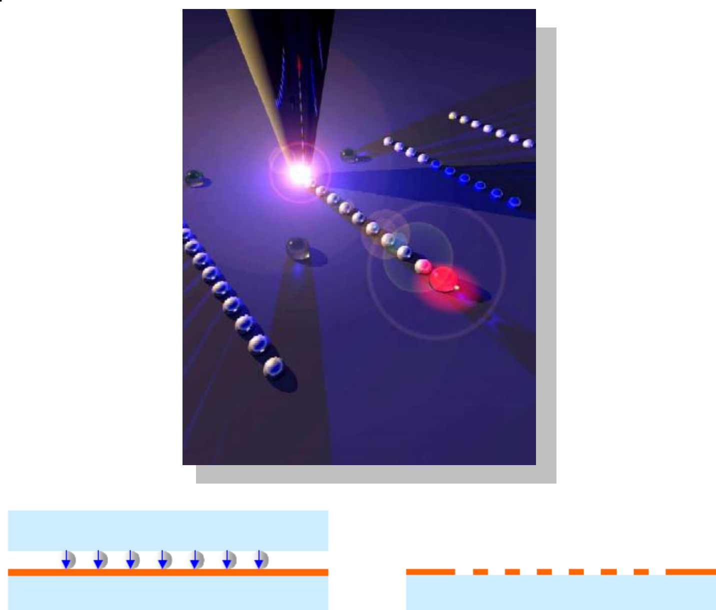

Figure 19 Near-Field Lithography[26]

As Figure 19 shown, illumination of metal nanoparticles at plasmon resonance produces a strongly enhanced dipole field near the particle. This enhanced field can be used to locally expose a thin layer of resist. In order to obtain intensity enhancement directly below the particle, the incoming light should be polarized approximately normal to the resist layer (p-polarization), implying the need for glancing incidence exposure. We have shown that the local field enhancement occurring around metal nanoparticles when they are excited at the surface plasmon resonance frequency can be used to print nanoscale features in thin resist layers. Feature sizes below $\lambda/10$ can be generated using visible illumination and standard g-line photoresist.[26]

Appendix M Dip-pen Lithography

Dip-Pen Nanolithography (DPN) is a scanning probe nanopatterning technique in which an AFM tip is used to deliver molecules to a surface via a solvent meniscus, which naturally forms in the ambient atmosphere.

As the AFM tip approaches the substrate, a water meniscus forms between them. The molecules transport and anchor themselves to the substrate via chemisorptions or electrostatic interactions. When alkanethiols are patterned on a gold substrate, a monolayer is formed in which the thiol headgroups form relatively strong bonds to the gold and the alkane chains extend roughly perpendicular to surface (Figure 20).

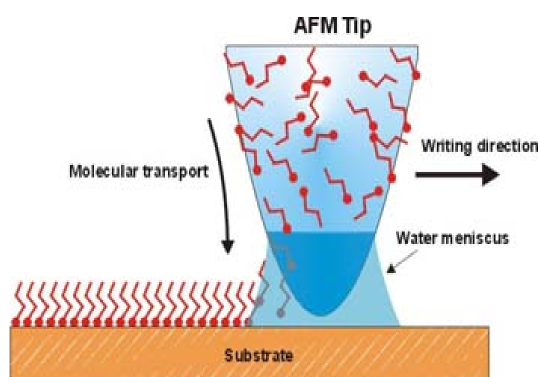

Figure 20 Dip-Pen Nanolithography[27]

Creating nanostructures using DPN is a single step process which does not require the use of resists. Using a conventional atomic force microscope (AFM) it is possible to achieve ultra-high resolution features with linewidths as small as 10-15 nm with ~ 5 nm spatial resolution. For nanotechnological applications, it is not only important to pattern molecules in high resolution, but also to functionalize surfaces with patterns of two or more components.

One of the most important attributes of DPN is that, because the same device is used to image and write a pattern, patterns of multiple molecular inks can be formed or aligned on the same substrate. With the aid of software created in-house (which has been commercialized through NanoInk), we have devised a nanolithographic tool which is ink-general and allows for simple registration of inks. Also, the contamination which could result from typical lithographic techniques (such as photolithography), is avoided.[27]

Appendix N Focused Ion Beam Lithography

IBL is similar to EBL in applications, feature sizes and the fact that it is a serial approach, but uses a beam of ions instead of electrons (Figure21). A fundamental difference is that ions are charged atomic that can interact physically and chemically with, and settle into, the exposed material ,and the particles of which are many orders of magnitude more massive than electrons. This addition of material offers the possibility of building up structures rather than just creating structures destructively.[28]

Ion Beam Lithography using MeV protons is a technique which is able to produce 3D microstructures in positive resists such as PMMA as well as in negative resists such as SU-8. An advantage of IBL is that no mask is needed to produce structures with high aspect ratios and sub-micrometer detail in the lateral direction. There are two basic features of the IBL setup: First is the implementation of a faster scanning system spherically designed for high resolution IBL. Second, the smallest feature size attainable is determined by the lateral dose distribution of the ion beam, which varies with depth in the resist.[29]

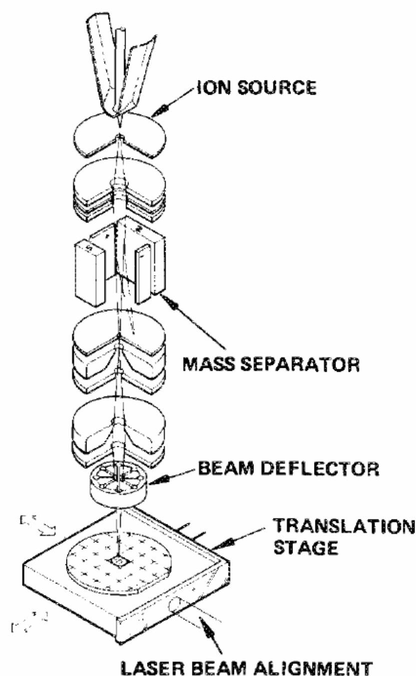

Figure 21 Schematic of focused ion beam lithography[30]

Appendix O Nano-imprint Lithography

Nanoimprint is an emerging lithographic technology that promises high-throughput patterning of nanostructures. Based on the mechanical embossing principle, nanoimprint technique can achieve pattern resolutions beyond the limitations set by the light diffractions or beam scatterings in other conventional techniques. There are three major ways to achieve the process:

1. Nano-Imprint Lithography

Imprint lithography has two steps: imprint and pattern transfer. In the imprint, a mold with nanostructures on its surface is pressed into a thin resist cast on a substrate. The resist, a thermal plastic, is deformed readily by the mold when heated above its glass transition temperature (due to a low viscosity). After the resist is cooled below its glass transition temperature, the mold is removed (Figure 22). In the pattern transfer, an anisotropic etching process, such as reactive ion etching, is used to remove the residual resist in the compressed area, transferring the thickness contrast pattern created in the imprint into the entire resist.[31]

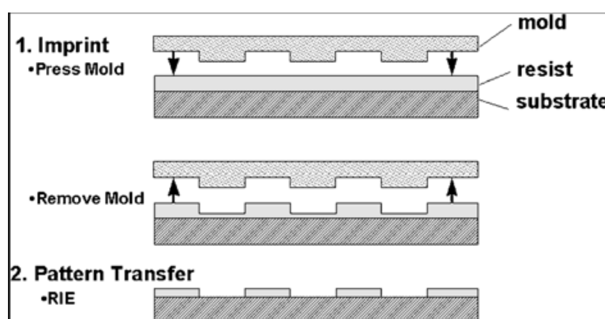

Figure 22 Nano-Imprint Lithography [31]

2. Step and Flash Imprinting Lithography

An organic thermoset planarizing/transfer layer was coated on a silicon wafer and then cured. A thin layer of a silicon-containing thermoplastic was spin coated on the transfer layer. An etched polysilicon on silicon template was brought into contact with the coated substrate. This "sandwich" structure was then placed in a press and heated to 150 °C under pressure for 15 minutes (Figure 23). An advantage to this process is that one needs only to generate low aspect ratio features. These features can then be transferred through the transfer layer via an anisotropic O2 RIE etching process analogous to that used in bilayer lithography to generate high aspect ratio, high-resolution images.[32]

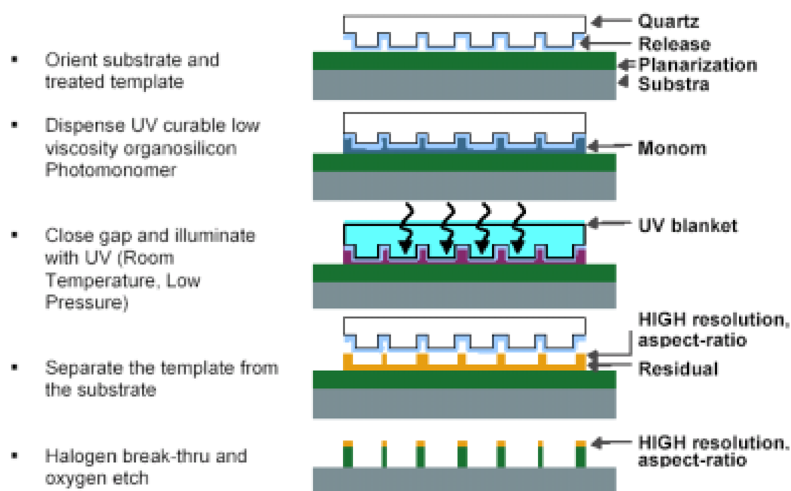

Figure 23 Step and Flash Imprinting Lithography[32]

3. Laser Assisted Direct Imprint

In 'laser-assisted direct imprint' (LADI)—a single excimer laser pulse melts a thin surface layer of silicon, and a mould is embossed into the resulting liquid layer(Figure 24). A variety of structures with resolution better than 10 nm have been imprinted into silicon using LADI, and the embossing time is less than 250 ns. The high resolution and speed of LADI, which we attribute to molten silicon's low viscosity (one-third that of water), could open up a variety of applications and be extended to other materials and processing techniques. [33]

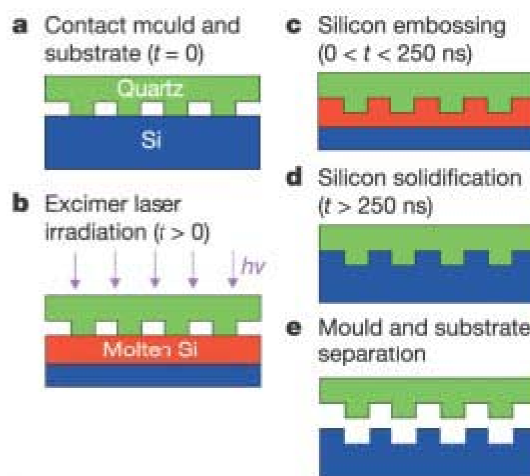

Figure 24 Laser-assisted direct imprint[33]

5. Reference

[1] SEMATECH Maskless Workshop, Jan. 2005. Available at http://www.sematech.org/resources/litho/meetings/emerging/20050117/

[2] B.J. Kampherbeek, *"MAPPER Technology Developments,"* Maskless Workshop, January 17-19 2005

[3] Moonen, D., L.H.A. Leunissen, P.W.H. de Jager, P. Kruit, A.J. Bleeker, K.D. v.d. Mast, *"Design of an Electron Projection System with Slider Lenses and Multiple Beams,"* in Proceedings of SPIE 2002, 5-7 march 2002.

[4] T. Haraguchi, T. Sakazaki, S. Hamaguchi, and H. Yasuda, *"Development of electromagnetic lenses for multielectron beam lithography system,"* Journal of Vacuum Sciences and Technology B 20 (6), Nov/ Dec, 2002

[5] Yasuda Hiroshi, "*A proposal for an MCC (Multi-Column Cell with Lotus Root lens) system to be used as a mask making e-beam tool,"* Proceedings of the SPIE, Volume 5567, pp. 911-921, 2004.

[6] A. Yamada, *ADVANTEST Technology Developments*, Maskless Workshop, January 17-19 2005

[7] Phillip Ware, "Removing The Mask," oe magazine pp. 26-27, march 2002.

[8] Marian Mankos, Harald F. Hess, David L. Adler, and Kirk J. Bertsche, *"Maskless reflection electron beam projection lithography,"* US Patent Issued on March 22, 2005

[9] N. William Parker, *A high throughput NGL electron beam direct-write lithography system*, Proceedings of SPIE, Volume 3997, pp. 713-720, 2000

[10] T.S. Ravi, *MultiBeam Systems Technology Developments*, Maskless Workshop, January 17-19 2005

[11] Christoph Brandstätter, *Projection maskless lithography*, Proceedings of the SPIE, Volume 5374, pp. 601-609, 2004.

[12] C. Brandstätter, *Leica Technology Developments*, Maskless Workshop, January 17-19 2005.

[13] Juergen Gramss, Hans Eichhorn, Melchior Lempke, Renate Jaritz, Volker Neick, Dirk Beyer, Bertram Buerger, Ulrich Baetz, Klaus Kunze, and Nikola Belic, *"Data prep: the bottleneck of future applications?"***,** Proc. SPIE 6281, 2006

[14] Sven-Hendrik Voss and Maati Talmi ,*"FPGA based high-speed system solutions for innovative maskless lithography systems"***,** Proc. SPIE 6283, 2006

[15] Sven-Hendrik Voss a,*, Maati Talmi a, Juergen Saniter a, Juergen Eindorf a, Alexander Reisig a, Joachim Heinitz b, Ernst Haugeneder, *"High-speed data storage and processing for projection mask-less lithography systems"*, Microelectronic Engineering 83 (2006)

[16] Vito Dai and Avideh Zakhor ,*"Lossless layout compression for maskless lithography systems",* Proc. SPIE 3997, 2000

[17] Hsin-I Liu, Vito Dai, Avideh Zakhor, and Borivoje Nikolic, *"Reduced complexity compression algorithms for direct-write maskless lithography systems"***,** Proc. SPIE 6151, 2006

[18] Rajesh Menon, Dario Gil, and Henry I. Smith., "*Experimental characterization of focusing by high-numerical-aperture zone plates*" Journal of the Optical Society of America A, vol. 23, Issue 3, pp. 567-571, 2006.

[19] *Maskless Parallel Patterning with Zone-Plate-Array Lithography* by Dario Gil, Master's thesis, Massachusetts Institute of Technology, Department of Electrical Engineering and Computer Science, June 2000.

[20] Rajesh Menon, Amil Patel, David Chao, Michael Walsh, and H. I. Smith, *"Zone-Plate-Array Lithography (ZPAL): Optical Maskless Lithography for Cost-Effective Patterning,"* Proceedings of the SPIE, Volume 5751, pp. 330-339, 2005

[21] Dario Gil, *"Maskless Parallel Patterning with Zone-Plate-Array Lithography,"* June 2000.

[22] Timothy O'Neil, Arno Bleeker, and Kars Troost, *"Optical Maskless Lithography (OML) Project Status,"* Maskless Workshop, January 17-19 2005.

[23] Tor Sandstrom, Arno Bleeker, Jason D. Hintersteiner, Kars Troost, Jorge Freyer, and Karel van der Mast, *"OML: optical maskless lithography for economic design prototyping and small-volume production,"* Proceedings of SPIE -- Volume 5377, pp. 777-787, May 2004.

[24] Hans Martinsson, et al., *"Current status of optical maskless lithography,"* Journal of Microlithography, Microfabrication, and Microsystems, Volume 4, Issue 1, pp. 11003, 2005.

[25] Pieter G. Kik, Stefan A. Maier, and Harry A. Atwater, "*Plasmon Printing-A New Approach to Near-Field Lithography*" Mat. Res. Soc. Symp. Proc. 705, Y3.6, 2002.

[26] Homepage: NanoPhotonics Characterization Lab. of University Central Florida — at http://kik.creol.ucf.edu/index.htm

[27] Piner,R. D.; Zhu, J.; Xu, F.; Hong, S.; Mirkin, C. A. *"Dip Pen Nanolithography,"* Science, 1999, 283, 661-663.

[28] Paul Holister, Cristina Román Vas, Tim Harper, *"Lithography Technology White Paper,"* Cintífica, LTD., October 2003

[29] J.A. van Kan, J.L. Sanchez, B. Xu, T. Osipowicz, F. Watt, *"Micromachining using focused high energy ion beams: Deep Ion,"* Nucl. Instr. and Meth. in Phys. Res. B 148 (1999) 1085-1089

[30] John Melngailis, *"Focused ion beam technology and applications,"* Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures, March 1987, Volume 5, Issue 2, pp. 469-495

[31] Stephen Y. Chou, Peter R. Krauss, Wei Zhang, Lingjie Guo, and Lei Zhuang, *"Sub-10 nm imprint lithography and applications,"* J. Vac. Sci. Technol. B 15.6., Nov/Dec 1997

[32] M. Colburn, S. Johnson, M. Stewart, S. Damle, T. Bailey, B. Choi, M. Wedlake, T. Michaelson, S.V. Sreenivasan, J. Ekerdt, and C. G. Willson, *"Step and Flash Imprint Lithography:A New Approach to High-Resolution Patterning,"* Proc. SPIE, 1999

[33] Stephen Y. Chou, Chris Keimel and Jian Gu, *"Ultrafast and direct imprint of nanostructures in silicon,"* 20 JUNE 2002, NATURE VOL 417