行政院國家科學委員會專題研究計畫 期中進度報告

具區塊記憶特性之隨機碼(2/3)
期中進度報告(精簡版)

計 畫 類 別 ：個別型
計 畫 編 號 ：NSC 95-2221-E-002-181-
執 行 期 間 ：95 年 08 月 01 日至 96 年 07 月 31 日
執 行 單 位 ：國立臺灣大學電機工程學系暨研究所

計 畫 主 持 人：林茂昭

報 告 附 件 ：出席國際會議研究心得報告及發表論文

處 理 方 式 ：期中報告不提供公開查詢

中 華 民 國 96 年 05 月 17 日

行政院國家科學委員會專題研究計畫
期中報告
具區塊記憶特性之隨機碼 (2/3)
Random Coding with InterBlock Memory

計畫編號：NSC 95-2221-E-002-181
執行期間：95 年 8 月 01 日至 96 年 10 月 31 日
主持人：林茂昭 國立臺灣大學電機工程學系

一、中文摘要

在本年度計劃中，我們研究具區塊間記憶之渦輪碼編碼調變系統，其編碼架構為在傳統渦輪碼後串接一個多工器(multiplexer)、延遲處理器(delay processor)及訊號點對應器(signal mapper)。在本研究中，我們考慮相鄰區塊間之不同記憶程度，並為改善在單個的碼句(codeword)內反覆的解碼方法(IDSC)會導致大錯誤係數的問題，我們提出一種在相鄰碼句間訊息傳遞之重覆性解碼演算法(IDAC)，可以提昇系統的可靠度。

研究成果顯示，在同樣的解碼複雜度、錯誤率和解碼的延遲長度的考量下，我們所設計的具區塊間記憶之渦輪碼編碼調變，在使用 IDAC 來解碼下，不管是短碼或是長碼均優於傳統的渦輪碼編碼調變系統。
關鍵詞：隨機碼、渦輪碼、編碼調變、重覆性解碼。

英文摘要

In this project, we investigate the performance of turbo coded modulation with interblock memory for which the encoding is implemented by serially concatenating a multiplexer, a multilevel delay processor, and a signal mapper to a conventional turbo encoder.

In this research, we consider the conditions of various degrees of interblock memory. We propose iterative decoding between adjacent codewords (IDAC), which provides error performance much better than the iterative decoding within a single codeword (IDSC). Simulation results show that with IDAC, turbo coded modulation with interblock memory is superior to the conventional turbo trellis coded modulation for either short or long code length considering the associated complexity, error rates, and decoding delay.
Keywords: Random coding, Turbo Code, coded modulation, Iterative Decoding.

二 、計畫的緣由、文獻探討與目的(Goals)

In the last decade, random-like codes such as binary turbo codes [1], low density parity check (LDPC) codes [2], turbo trellis coded modulation (TTCM) [3], and bit interleaved coded modulation (BICM) [4] have pushed the error performances of channel coding close to the Shannon limit for very long codes. However, there is still some room for improvement if the code lengths and coding complexity are taken into consideration.

Each of the turbo code, the LDPC code, or BICM is a block code for which the dependency of code bits (or symbols) is confined within one block. We believe that adding dependency to code bits (symbols) of different blocks of a random coding design can enhance the coding performance. In this 3-year proposal, we will investigate the rich field of random coding with interblock memory.

In the first project year, the performance of binary turbo coding with interblock memory was investigated. In this year, we study turbo coded modulation with interblock memory. In the third year, we will design turbo BLAST with interblock memory, where turbo BLAST is a randomly coded MIMO system.

三、研究方法(Methods)

In the first project year, we investigate the performance of binary turbo coding with interblock memory for which the encoding is implemented by serially concatenating a multiplexer, a multilevel delay processor, and a

binary signal mapper to a conventional turbo encoder. The scheme of binary turbo coding with interblock memory can also be used to construct coded modulation if the binary signal mapper is replaced by the signal mapper for a modulation constellation.

A. Encoding

Fig. 1 shows the encoding structure of turbo coded modulation with interblock memory, *T*, where *C* is the conventional binary turbo code [1]. The output of *C* is split into multiple streams, and then each stream undergoes a different delay. These streams are linearly combined to form *T*. The code *C* is constructed from a rate-1/3 binary turbo code which consists of a *K*-bit interleaver and rate-1/2 constituent codes RSC1 and RSC2. An arbitrary code rate $R > 1/3$ for *C* can be obtained by uniformly puncturing the parity bits of RSC1 and RSC2.

Denote the *t*-th code word of a rate-1/3 turbo code word as $[\bar{u}(t), \bar{p}_1(t), \bar{p}_2(t)]$, where $\bar{u}(t)$ is the message part and $\bar{p}_1(t)$ and $\bar{p}_2(t)$ are parity parts from RSC1 and RSC2, respectively.

Let $\bar{u}(t) = [u(t,0), u(t,1), \cdots, u(t,K-1)]$ and $\bar{p}_j(t) = [p_j(t,0), p_j(t,1), \cdots, p_j(t,K-1)]$, where $u(t,k)$ and $p_j(t,k)$, j = 1,2, k = 0,1,…,*K*-1, are binary bits. A code word at time *t*, $\bar{a}(t)$, of rate-2/3 binary turbo code *C*, $\bar{a}(t) = [\bar{u}(t), \bar{p}(t)]$, where $\bar{p}(t) = [p_1(t,0), p_2(t,1), p_1(t,4), p_2(t,5), \cdots, p_1(t,K-2), p_2(t,K-1)]$, can be obtained by uniformly puncturing one fourth of parity bits of both $\bar{p}_1(t)$ and $\bar{p}_2(t)$.

The turbo coded sequence $\vec{a} = \{\cdots, \bar{a}(t), \bar{a}(t+1), \cdots\}$ is sequentially processed by the multiplexer and the delay processor to produce the associated output sequences $\vec{v} = \{\cdots, \bar{v}(t), \bar{v}(t+1), \cdots\}$ and $\vec{s} = \{\cdots, \bar{s}(t), \bar{s}(t+1), \cdots\}$, respectively, where $\bar{v}(t) = [\hat{v}(t,0), \hat{v}(t,1), \cdots, \hat{v}(t,\lambda-1)]$, $\bar{s}(t) = [\hat{s}(t,0), \hat{s}(t,1), \cdots, \hat{s}(t,\lambda-1)]$, and each of $\hat{v}(t,k) = [v_1(t,k), \cdots, v_m(t,k)]$ and $\hat{s}(t,k) = [s_1(t,k), \cdots, s_m(t,k)]$ is a binary *m*-tuple. Note that $m\lambda = K/R$. The sequence $\vec{s}$ is then processed by a memoryless signal mapper to produce the output sequence $\vec{z} = \{\cdots, \bar{z}(t), \bar{z}(t+1), \cdots\}$, where $\bar{z}(t) = [\hat{z}(t,0), \hat{z}(t,1), \cdots, \hat{z}(t,\lambda-1)]$ and $\hat{z}(t,k) = \omega(\hat{s}(t,k)) \in \Omega$. Ω is a signal constellation consisting of 2^m signal points. The resultant code *T* takes $\vec{z}$ as its code sequence.

For concise presentation, the indexes *t* and *k* are omitted in the remainder of this paragraph. For a constellation with 2^m points, we consider a q-level partition, $q \le m$. Let $0 = i_0 < i_1 < \cdots < i_{q-1} < i_q = m$, where i_j is an integer. Write $\hat{s} = [\theta_1, \cdots, \theta_q]$, where $\theta_j = [s_{i_{j-1}+1}, s_{i_{j-1}+2}, \cdots, s_{i_j}]$. With this, we can have a q-level partition chain $\Omega = \Omega_0 / \Omega_1 / \Omega_2 / \cdots / \Omega_q$, where Ω_{j-1} is partitioned into $2^{i_j - i_{j-1}}$ cosets of Ω_j and θ_j represents one of the $2^{i_j - i_{j-1}}$ cosets [9-10]. Since Ω is a signal constellation, the distance measure $\Delta(\hat{z}, \hat{z}')$ is the squared Euclidean distance between $\hat{z}$ and $\hat{z}'$. Let $\omega(\hat{s})$ and $\omega(\hat{s}')$ denote two signal points which are in the same coset of Ω_{j-1}, but in distinct cosets of Ω_j labelled by $\theta_j = \alpha$ and $\theta_j = \beta$, respectively. We define $\Delta_j(\alpha, \beta)$ to be the least one of all the possible $\Delta(\omega(\hat{s}), \omega(\hat{s}'))$, and $n_j(\alpha, \beta)$ to be the average number of signal points $\omega(\hat{s}')$ satisfying $\Delta(\omega(\hat{s}), \omega(\hat{s}')) = \Delta_j(\alpha, \beta)$.

Furthermore, let $\omega(\hat{s}), \omega(\hat{s}') \in \Omega_{j-1}$ and $s_{i_{j-1}+k} \ne s'_{i_{j-1}+k}$. We define $\delta_j^{i_{j-1}+k}$, $k = 1, \cdots, i_j - i_{j-1}$, to be the least one of all the possible $\Delta(\omega(\hat{s}), \omega(\hat{s}'))$, and $\eta_j^{i_{j-1}+k}$ to be the average number of signal points $\omega(\hat{s}')$ satisfying $\Delta(\omega(\hat{s}), \omega(\hat{s}')) = \delta_j^{i_{j-1}+k}$. Note that if $q = m$, then $\delta_j^j = \Delta_j(1,0) = \Delta_j$ and $\eta_j^j = n_j(1,0) = n_j$ for $j = 1, \cdots, m$. The necessity of introducing the m-level parameters, i.e., η_i^j and δ_i^j for all possible i and j, in addition to the q-level parameters $\{\Delta_1(\cdot,\cdot), \cdots, \Delta_q(\cdot,\cdot)\}$ and $\{n_1(\cdot,\cdot), \cdots, n_q(\cdot,\cdot)\}$ is

that even though we use a q-level partition structure in the encoding, the bit-by-bit decoding used in the turbo decoding views the coding as an m-level structure.

Example 1 : Let m = 3, q = 3 and $\{i_1, i_2, i_3\} = \{1,2,3\}$. Consider an 8PSK signal constellation Ω with Ungerboeck's labelling [9]. It can be checked that $\{\Delta_1(1,0) = 0.586, \Delta_2(1,0) = 2, \Delta_3(1,0) = 4\}$, $\{n_1(1,0) = 2, n_2(1,0) = 2, n_3(1,0) = 1\}$, $\{\delta_1^1 = 0.586, \delta_2^2 = 2, \delta_3^3 = 4\}$ and $\{\eta_1^1 = 2, \eta_2^2 = 2, \eta_3^3 = 1\}$.

Example 2 : Let m = 3, q = 2 and $\{i_1, i_2\} = \{1,3\}$, Consider an 8PSK signal constellation Ω with mixed labelling [6]. It can be checked that $\{\Delta_1(1,0) = 0.586, \Delta_2(00,10) = 2, \Delta_2(00,01) = 2, \Delta_2(00,11) = 4\}$, $\{n_1(1,0) = 2, n_2(00,10) = 1, n_2(00,01) = 1, n_2(00,11) = 1\}$, $\{\delta_1^1 = 0.586, \delta_2^2 = 2, \delta_2^3 = 2\}$ and $\{\eta_1^1 = 2, \eta_2^2 = 1, \eta_2^3 = 1\}$.

With such a q-level partition, we can use a general q-level delay processor instead of the m-level delay processor to construct coded modulation. Write $\hat{v}(t,k) = [\gamma_1(t,k), \cdots, \gamma_q(t,k)]$, where $\gamma_j(t,k) = [v_{i_{j-1}+1}(t,k), v_{i_{j-1}+2}(t,k), \cdots, v_{i_j}(t,k)]$. The relationship between $\gamma_j(t,k)$ and $\theta_j(t,k)$ is $\theta_j(t,k) = \gamma_j(t-(q-j),k)$ for $1 \le j \le q$, $k = 0,1,2,\cdots,\lambda-1$ and $m\lambda = K/R$.

We can use either IDSC or IDAC to decode T in the case of coded modulation. Note that, for either IDSC or IDAC, the extrinsic value for each labelling bit is calculated in bit level rather than in symbol level in the MAP demapper since the bit-by-bit decoding is used in the turbo decoding of *C*.

B. Two specific constructions

We now consider the design of TCM with rate of 2 bits per 8PSK symbol. Let *C* be a rate-2/3 conventional binary turbo code with an interleaver size of K message bits. Let $\bar{a}(t) = [\bar{u}(t), \bar{p}(t)]$ be the *t*-th codeword of *C*, where $\bar{p}(t) = [p_1(t,0), p_2(t,1), p_1(t,4), p_2(t,5), \cdots, p_1(t,K-2), p_2(t,K-1)]$.

Construction A: We use the parameters of *m*, Ω, *q*, $\{i_1, i_2\}$ and the signal labelling as given in Example 2. The relation between inputs and outputs of the multiplexer is described by $v_1(t,k) = u(t,2k)$ and $v_2(t,k) = u(t,2k+1)$. In addition, $v_3(t,k) = p_1(t,2k)$ for even k and $v_3(t,k) = p_2(t,2k-1)$ for odd *k*. Let $\lambda = K/2$. The relation between inputs and outputs of the delay processor is described by $s_1(t,k) = v_1(t-1,k)$, $s_2(t,k) = v_2(t,k)$ and $s_3(t,k) = v_3(t,k)$, $k = 0,1,\cdots,\lambda-1$. The relation among $\vec{s}$, $\vec{v}$ and $\vec{a}$ is given in Fig. 2. The resultant code *T* is a TCM with rate 2 bits per 8PSK symbol.

We may consider a modified version of Construction A which is denoted as Construction A' by employing Ungerboeck's labelling instead of mixed labelling and a three-level delay processor, i.e., $m = q = 3$ and $\lambda = K/2$, which yields $\{\Delta_1(1,0) = 0.586, \Delta_2(1,0) = 2, \Delta_3(1,0) = 4\}$ and $\{\eta_1^1 = 2, \eta_2^2 = 2, \eta_3^3 = 1\}$. Although the asymptotic performance is quite good, $\{\eta_1^1 = 2, \eta_2^2 = 2, \eta_3^3 = 1\}$ implies a dense distance spectrum and hence causes poor error performance by using IDSC for the SNR of interested to us. In addition, the decoding delay will be increased. Although we can use IDAC to decode Construction A' for reducing the increased error coefficients, we must respectively apply IDSC to $\bar{a}(t)$, $\bar{a}(t+1)$, and $\bar{a}(t+2)$ to sufficiently reduce the increased error coefficients and hence the decoding complexity is significantly increased. Moreover, the decoding delay is further increased.

Suppose that we switch the positions of $u(t,2k)$ and $p_1(t,2k)$, and switch the positions of $u(t,2(k+1))$ and $p_2(t,2k+1)$, where *k* is an even integer. Then, the message for which $u(t,2k)$ and $u(t,2(k+1))$ are zero for all the even *k* will greatly reduce the code distance. A compromise given in the following construction can obtain less code distance but thinner distance spectrum as compared to Construction A.

Construction B: This construction is the same as Construction A except that we switch the

positions of $u(t,2(k+1))$ and $p_2(t,2k+1)$, where k is an even integer.

In T, the code bits of C are split into the streams with different delays before being fed into the signal mapper. This design allows streams with different delays to have different levels of protection. Hence, T provides some kind of irregularity for the code bits of C. Furthermore, we can provide a variety of irregularity by considering the construction T_C which employs various degrees of interblock memory. T_C is obtained by passing only a fraction, P_{IB}, of the code bits of C through the delay processor, while the input of the signal mapper is the combination of the output of the delay processor and the remaining bits of C. By varying the fraction, P_{IB}, we can have T_C with various irregularity and error performance.

we can consider coded modulation constructed from various degrees of combination of Construction A (or Construction B) and the TTCM in [3]. The TTCM in [3] is constructed by appending to the encoder of a binary turbo code C a multiplexer, an interleaver, and a signal mapper. The labelling used in the signal mapper of the TTCM in [3] is the Gray labelling. For Construction A or B with P_{IB}=1, the decoding delay is 2K message bits, i.e., K 8PSK symbols, if IDSC is used. If IDAC is used, the decoding delay becomes 3K message bits. In general, for Construction A or B with $P_{IB} = \varepsilon$, the decoding delay is $2K\varepsilon$ + (1-ε)K message bits if IDSC is used. If IDAC is used, the decoding delay becomes $3K\varepsilon$ + (1-ε)2K message bits. For the TTCM in [3], the decoding delay is K message bits.

C. Distance properties

With the general q-level delay processor and the signal mapper, we can check the distance properties of the resultant code T in a manner similar to that used in [8]. Let $\vec{v} = \{\cdots, \bar{v}(-1), \bar{v}(0), \cdots\}$ be a weight-d binary sequence that is the multiplexed version of a turbo coded sequence $\vec{a}$ from C. Let $\vec{z}$ and $\vec{z}_0$ be the output sequences associated with $\vec{v}$ and $\vec{0}$, respectively, where $\vec{0}$ is the all zero sequence. Assume $\bar{v}(t) = \bar{0}$ for t < 0 and $\bar{v}(0) \neq \bar{0}$, where $\bar{0}$ is the all zero codeword consisting of λ binary m-tuples. The pairwise distance measure $\Delta(\vec{z}, \vec{z}_0)$ between sequences $\vec{z}$ and $\vec{z}_0$ is lower bounded by $\Delta_{LB}(\vec{v},\vec{0}) = \sum_{j=1}^{q}\sum_{k=0}^{\lambda-1}\Delta_j(\gamma_j(0,k),\hat{0}_j)$, where $\hat{0}_j$ denotes the all zero $(i_j - i_{j-1})$-tuple.

D. Iterative decoding within a single codeword (IDSC)

We illustrate IDSC for Construction A. Extension to other constructions is straightforward. Fig. 2 shows the relation among sequences $\vec{s}$, $\vec{v}$ and $\vec{a}$ for Construction A, where $\vec{a}$, $\vec{v}$ and $\vec{s}$ are the output sequences of the encoder of C, the multiplexer, and the delay processor, respectively. Let $\bar{z}(t)$ be the transmitted word and $\bar{y}(t)$ be the received word. For j=1,2,3, write
$\bar{v}_j(t) = [v_j(t,0), v_j(t,1), \cdots, v_j(t,\lambda-1)]$.

Now consider the decoding of $\bar{a}(t)$. The decoder of IDSC consists of a MAP (maximum a posteriori probability) demapper and a turbo decoder of C. Suppose the extrinsic L-values (or log-likelihood ratios) $L_{D,e}(\bar{a}(t-1)) = L_{D,p}(\bar{a}(t-1)) - L_{D,c}(\bar{a}(t-1))$ of bits in $\bar{a}(t-1)$ have been obtained from the decoding of $\bar{a}(t-1)$, where $L_{D,p}(\bar{a}(t-1))$ and $L_{D,c}(\bar{a}(t-1))$ are the associated *a posteriori* and channel values.

Step 1 The demapper computes the *a posteriori* L-values $L_{M,p}(\bar{v}_2(t))$ of bits in $\bar{v}_2(t)$ and $L_{M,p}(\bar{v}_3(t))$ of bits in $\bar{v}_3(t)$, based on the received word $\bar{y}(t)$ and the *a priori* L-values $L_{M,a}(\bar{v}_1(t-1)) = 0$ which can be obtained from $L_{D,e}(\bar{a}(t-1))$. Similarly, the demapper computes $L_{M,p}(\bar{v}_1(t))$ based on $\bar{y}(t+1)$ and $L_{M,a}(\bar{v}_2(t+1)) = L_{M,a}(\bar{v}_3(t+1)) = 0$. In

the calculation of $L_{M,p}(\bar{v}(t))$, the values $L_{M,a}(\bar{v}(t))$ are zero and hence the values $L_{M,p}(\bar{v}(t))$ equal the extrinsic values $L_{M,e}(\bar{v}(t))$.

Step 2 The turbo decoder of C uses $L_{M,p}(\bar{v}(t))$ as channel value $L_{D,c}(\bar{a}(t))$ for bits in $\bar{a}(t)$ to recover bits of $\bar{a}(t)$ and obtain values $L_{D,e}(\bar{a}(t))$ which are stored for the calculation of $L_{M,p}(\bar{v}_2(t+1))$ and $L_{M,p}(\bar{v}_3(t+1))$.

Throughout this paper, the Max-Log-MAP algorithm with correction factors [11-12] is employed and N_I denotes the number of iterations for the decoding of C.

In C, this weight-d binary sequence, $\vec{v}$, contributes to only "one" neighbor in counting $N(d)$, where $N(d)$ is the multiplicity of codewords of weight d. For T with IDSC, this weight-d binary sequence, $\vec{v}$, may contribute more than one in counting $N(\Delta_{LB}(\vec{v},\vec{0}))$. Specifically, the code sequence, $\vec{v}$, contributes to

$$n(\vec{v},\vec{0}) = \prod_{j=1}^{q}\prod_{k=1}^{i_j - i_{j-1}}\prod_{\ell=1}^{\lambda-1}[\eta_j^{i_{j-1}+k}]^{v_{i_{j-1}+k(0,\ell)}} \quad (1)$$

neighbors in counting $N(\Delta_{LB}(\vec{v},\vec{0}))$.

E. Iterative decoding between adjacent codewords (IDAC)

For T, IDSC results in large error coefficients as indicated in equation (1). The error coefficients can be reduced and hence the performance can be improved by iteratively decoding between two adjacent turbo code words, $\bar{a}(t)$ and $\bar{a}(t+1)$. This decoding is referred to as iterative decoding between adjacent codewords (IDAC). We illustrate the decoding of $\bar{a}(t)$ for Construction A. Extension to other constructions is straightforward. Suppose that $L_{D,e}(\bar{a}(t-1))$ has been obtained.

Step 1 Based on $L_{D,e}(\bar{a}(t)) = 0$ (equivalently $L_{M,a}(\bar{v}(t)) = 0$), we use IDSC to decode $\bar{a}(t+1)$ and obtain $L_{D,e}(\bar{a}(t+1))$. In the demapper, the calculation of $L_{M,p}(\bar{v}(t+1))$ is based on $L_{M,a}(\bar{v}(t)) = 0$.

Step 2 Based on $L_{D,e}(\bar{a}(t+1))$ obtained in Step 1, $L_{D,e}(\bar{a}(t-1))$ and $L_{M,a}(\bar{v}(t)) = 0$, the demapper calculates $L_{M,p}(\bar{v}(t))$. The decoder of C then use $L_{M,p}(\bar{v}(t))$ as $L_{D,c}(\bar{a}(t))$ to decode $\bar{a}(t)$ and obtain $L_{D,e}(\bar{a}(t))$.

Step 3 Based on $L_{D,e}(\bar{a}(t))$ obtained in Step 2, we use IDSC to re-decode $\bar{a}(t+1)$ and update $L_{D,e}(\bar{a}(t+1))$.

Step 4 Based on updated $L_{D,e}(\bar{a}(t+1))$ obtained in Step 3, $L_{D,e}(\bar{a}(t-1))$, and $L_{M,a}(\bar{v}(t)) = 0$, the demapper calculates of $L_{M,p}(\bar{v}(t))$. The decoder of C uses updated $L_{M,p}(\bar{v}(t))$ as new channel values $L_{D,c}(\bar{a}(t))$ to decode $\bar{a}(t)$ and obtain $L_{D,e}(\bar{a}(t))$.

Step 5 After repeating Steps 3 and 4 for $N_{IDAC}-1$ times, we can recover $\bar{a}(t)$ and obtain $L_{D,e}(\bar{a}(t))$.

In the above, N_I iterations are used for each turbo decoding of C.

四、研究成果(Results)

We now consider the error performance of Constructions A and B. In the following, BER simulation and analysis of EXIT charts in AWGN channels are given. The constituent codes used in these examples are 4-state and 16-state codes with generator matrices given by $(1, 5/7)_8$ and $(1, 37/21)_8$, respectively.

A. BER results for short-to-moderate code lengths

The simulation of 4-state Constructions A and B with P_{IB} = 1 (or P_{IB} = 4/8) and K = 2048 by using either IDSC or IDAC is performed. The simulation of 4-state TTCM constructed

from [3] is also performed for comparison. The simulation results are given in Fig. 3. From Fig. 3, we can see that the error performance of Construction A or B is better than that of TTCM [3] at moderate-to-high SNR not only for the same interleaver size but also for the same decoding delay. In particular, the 4-state Construction A with K = 2048, P_{IB} =4/8 can achieve a BER of 10^{-5} at E_b/N_o of 4.3 dB and 4.0 dB, respectively if IDSC and IDAC are respectively used, while for the 4-state TTCM [3] with K = 4096, the associated BER is around 2×10^{-5} at E_b/N_o=4.7 dB. The 4-state Construction A with K = 2048, P_{IB} =4/8 can achieve a BER of 10^{-4} at E_b/N_o of 4.05 dB and 3.85dB respectively if IDSC and IDAC are respectively used, while for the 4-state TTCM [3] with K = 4096, to achieve BER = 10^{-4}, E_b/N_o=4.3 dB is needed.

We also observe that the error performance at high SNR of Construction A or B can be improved by increasing P_{IB}. Construction A or B can achieve much better error performance with higher decoding complexity by using IDAC as compared to using IDSC. In addition, Construction A is suitable for low BER (or high SNR) conditions while Construction B is suitable for moderate BER (or moderate SNR) conditions.

B. BER results for long code lengths

We perform BER simulation for Construction B with large K to see whether the proposed TTCM can achieve the near-capacity performance. The simulation results are given in Fig. 4. We also perform the analysis of EXIT charts [7] to obtain the pinch-off SNR limits. The results of BER in the error floor region and pinch-off limits are also given in Table I. Also included in Table I are the simulation results of the TTCM constructed from [3]. We see that, Construction B with K = 262144 can achieve a BER of 3.18×10^{-8} at E_b/N_o = 3.14 dB which is slightly better than the threshold (pinch-off SNR) of 3.15 dB for the irregular LDPC-CM given in [5]. In addition, the pinch-off limits of 4-state and 16-state Construction B using IDAC are 3.10 dB and 3.05 dB, which are only 0.20 and 0.15 dB from the constraint capacity (2.9 dB),respectively.

五、結論與討論(Concluding Remarks)

In this research, the performance of turbo coded modulation with interblock memory is investigated. Coded modulation, T_C, can be constructed based on various degrees of interblock memory and decoded by using either IDSC or IDAC. Simulation shows that for short-to-long code lengths, the error performance of turbo coded modulation with interblock memory, in general, is better than that of the conventional TTCM[3], for moderate-to-high SNR. The simulation results are confirmed by the analysis of EXIT charts. We expect that there is advantage in introducing interblock memory to other random-like codes such as (irregular) LDPC codes, (irregular) RA codes, random coded MIMO, etc...

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六、圖表（Figures and Tables）

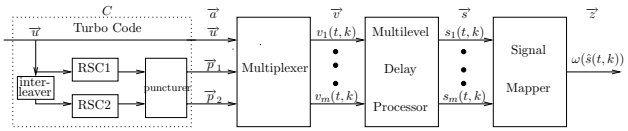

Fig. 1: Encoding structure of binary turbo coding with interblock memory

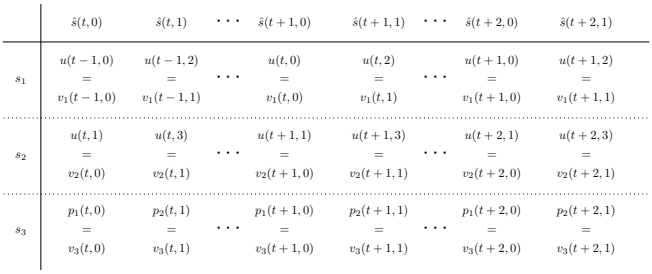

Fig.2: Relation among sequences $\vec{s}$, $\vec{v}$ and $\vec{a}$ for Construction A

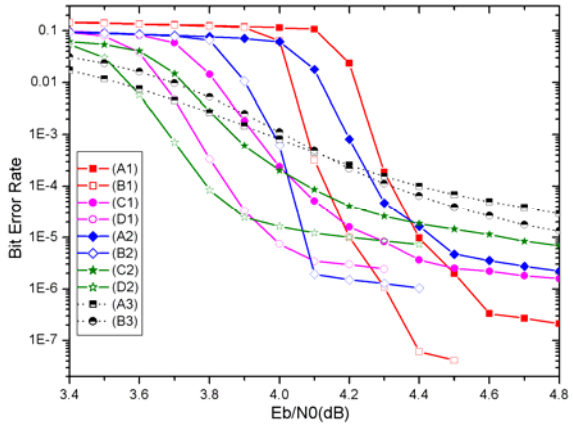

Fig.3: Simulation for 4-state Construction A (Constr. A), Construction B (Constr. B), and TTCM [3] with N_I=10.

(A1) Constr. A, IDSC, P_{IB}=1, K=2048.
(B1) Constr. A, IDAC, P_{IB}=1, N_{IDAC}=3, K=2048.
(C1) Constr. A, IDSC, P_{IB}=4/8, K=2048.
(D1) Constr. A, IDAC, P_{IB}=4/8, N_{IDAC} =3, K=2048.
(A2) Constr. B, IDSC, P_{IB}=1, K=2048.
(B2) Constr. B, IDAC, P_{IB}=1, N_{IDAC}=3, K=2048.
(C2) Constr. B, IDSC, P_{IB}=4/8, K=2048.
(D2) Constr. B, IDAC, P_{IB}=4/8, N_{IDAC}=3, K=2048.
(A3) 4-state TTCM[3], K=2048.
(B3) 4-state TTCM[3], K=4096.

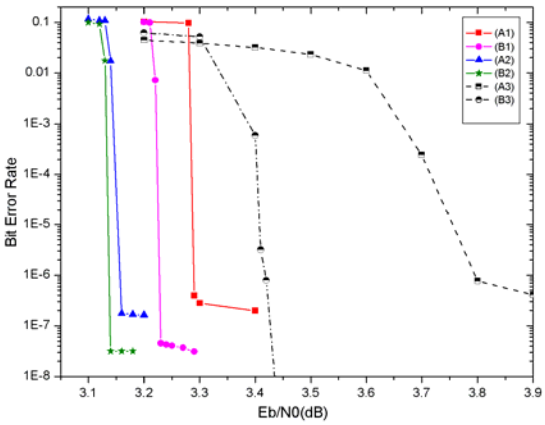

Fig.4: Simulation for Construction B (Constr. B) with P_{IB}=8/8 and TTCM[3]. All results are based on N_I=18.

(A1) 4-state Constr. B, IDSC, K=262144.
(B1) 4-state Constr. B, IDAC, N_{IDAC} =3, K=262144
(A2)16-state Constr. B, IDSC, K=262144.
(B2)16-state Constr. B, IDAC, NIDAC =3, K=262144
(A3):4-state TTCM[3], K=262144.
(B3):4-state TTCM[3], K=524288.

TABLE I
Results of pinch-off limits and BER in the error-floor regions for construction B and TTCM [3]. The BER simulation is based on N_I=18, and K=262144 and K=524288 for construction B and TTCM[3], Respectively.

	Construction B (4-state)			Construction B (16-state)		
	Pinch-off	Error Floor Performance		Pinch-off	Error Floor Performance	
	Limits(dB)	Eb/No(dB)	BER	Limits(dB)	Eb/No(dB)	BER
IDSC	3.27	3.30	2.81×10^{-7}	3.12	3.16	1.77×10^{-7}
IDAC	3.10	3.23	4.53×10^{-8}	3.05	3.14	3.18×10^{-8}
	TTCM[3] (4-state)			TTCM[3] (16-state)		
	Pinch-off	Error Floor Performance		Pinch-off	Error Floor Performance	
	Limits(dB)	Eb/No(dB)	BER	Limits(dB)	Eb/No(dB)	BER
	3.55	3.8	7.72×10^{-7}	3.25	3.40	2.43×10^{-6}

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我參加過多次 ISITA 並且在 2004 ISITA 及 2006 ISITA.都擔任學術議程委員，覺得這一次 ISITA 投稿數及參與會議人數都沒有以往熱烈估計。原因是近年有許多 IEEE 通訊領域的學術會議都接受消息理論領域之論文發表。這些論文可記錄於 IEEE Xplore 資料庫，方便他人於網路檢索。因此許多研究人員都樂於投稿於這些學術會議。目前發表於 ISITA 之論文則缺乏類似的資料庫支援網路檢索。我與 Fujiwara 教授談及此論點，Fujiwara 教授提及 ISITA 建立資料庫所面臨的一些問題，也會設法來解決處理。此外我來首爾之前受 IEEE Information Theory Society Taipei Chapter 的 Chapter Chair 韓永祥教授之託，來探詢在台灣舉辦 ISITA 之可能性。Fujiwara 教授告知 2008 ISITA 已經確定將於 New Zealand Auckland 舉行。因為台灣極可能舉辦 2010 IEEE VTC，所以我就沒有再探詢在台灣舉辦 2010 ISITA 之可能性。於大會進行中得知南韓又將舉辦 2009 IEEE ISIT 心中頗有一些失落感。

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我個人發表的論文為”Improved Decoding for Trellis Coded Modulation with a Convolutional Processor,”內容是針對以往設計之一種具大自由距離之籬柵式編碼調變設計改善錯誤率之解碼方式。先前之簡化解碼方式造成了大數量的錯誤係數

(近距離的路徑數目)，因此在低訊雜比的狀況下解碼錯誤率並不理想。在此論文中我們以乘積式籬柵(product trellis)來進行解碼，可以降低錯誤係數，也因而得以降低錯誤率。我在會議中遇到美國夏威夷大學的 Marc Fossorrier 教授，他對於此研究很感興趣，也建議一些可以進一步改善錯誤率之方向。此外，他也提到今年一位前往美國夏威夷大學接受他指導的攻讀博士學位的學生王仲立。Fossorrier 教授覺得王仲立資質很好，基礎紮實。這位王仲立同學先前曾在我指導之下獲得台大電信所碩士學位。

我參加過多次 ISITA 並且在 2004 ISITA 及 2006 ISITA.都擔任學術議程委員，覺得這一次 ISITA 投稿數及參與會議人數都沒有以往熱烈估計。原因是近年有許多 IEEE 通訊領域的學術會議都接受消息理論領域之論文發表。這些論文可記錄於 IEEE Xplore 資料庫，方便他人於網路檢索。因此許多研究人員都樂於投稿於這些學術會議。目前發表於 ISITA 之論文則缺乏類似的資料庫支援網路檢索。我與 Fujiwara 教授談及此論點，Fujiwara 教授提及 ISITA 建立資料庫所面臨的一些問題，也會設法來解決處理。此外我來首爾之前受 IEEE Information Theory Society Taipei Chapter 的 Chapter Chair 韓永祥教授之託，來探詢在台灣舉辦 ISITA 之可能性。Fujiwara 教授告知 2008 ISITA 已經確定將於 New Zealand Auckland 舉行。因為台灣極可能舉辦 2010 IEEE VTC，所以我就沒有再探詢在台灣舉辦 2010 ISITA 之可能性。於大會進行中得知南韓又將舉辦 2009 IEEE ISIT 心中頗有一些失落感。