A Dual-Loop Automatic Gain Control for Infrared Communication System

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ABSTRACT

This paper presents a dual-loop Automatic Gain Control (AGC) employed in 10Mbps infrared communication system. The AGC is composed of an exponential-type variable-gain amplifier, a shaping filter, a gain/buffer stage, a non-coherent envelope detector, and a pair of integrators that provide dual loop bandwidths. The switch and two integrators are realized by a proposed switched integrator technique. The fast acquisition is accomplished by a 500 KHz loop bandwidth at the initial acquisition state and followed by a 50 KHz loop bandwidth at the steady state. The AGC is implemented in $0.6\mu m$ SPTM CMOS technology. According to the post-layout simulation, it achieves an acquisition time of $5\mu s$ and provides a constant output of $1V_{pp}$ at a 50Ω load for 20dB input signal amplitude range. The dual-loop AGC consumes 88 mW power from a single 3.3-V supply and occupies $1.8 \times 1.8\ mm^2$ area.

1. INTRODUCTION

The booming wireless digital transmission technology stimulates demand for high speed portable information terminals. These terminals are strictly limited to power consumption, size, and weight. Infrared radiation medium conforms with these requirements for high speed, short range, light of sight (LOS), point-to-point cordless data transfer. It possesses not only the advantages of low cost, high speed infrared emitters and detectors but also the availability of spectral region that is wide and unregulated. The Infrared Data Association (IrDA) has established standards for short-range, half duplex LOS links operating at bit rates up to 4 Mb/s. Through prudent use of the technologies employed in currently available systems, it is possible to enhance the performance of wireless infrared transmission significantly. This design is based on the 10 Mb/s diffuse links infrared transmission system with 4-PPM modulation.

The critical issue to build an infrared link at this data rate is to develop a high performance receiver. In general, the receiver consists of an optical detector, analog front-end, an A/D converter, a matched filter, timing recovery circuits, and demodulation circuits. For most infrared link applications, the optical signals over the $780 - 950nm$ wavelength band are detected by silicon photodiodes and transformed to electric signals. The signal will be further processed by the analog front-end (AFE) circuit before digitization. The main function of the AFE is the automatic gain control (AGC) that keeps the signal within the dynamic range so as to fully load the fixed scale of the A/D converter and to provide the detection circuits in further synchronization process with signals of amplitude within the predefined level. To enhance the data transmission rate, the AGC needs to converge fast while averting from noise disturbance. The rest of this paper is to discuss a dual-loop AGC architecture that resorts its wide loop bandwidth to obtain a fast acquisition and turns to narrow loop bandwidth for less jitter performance at the steady state. Section II describes the proposed AGC architecture and circuit design followed by simulation results in Section III. Finally, conclusions are drawn in Section IV.

2. AGC ARCHITECTURE AND CIRCUIT

The AGC signal processor applied in the receiver of 10-Mb/s IR diffuse link demands fast convergence. The transmission system uses 4-PPM modulation and full slot scheme with slot rate of 20 MHz. The transmitted data package contains 2,098 bits including 70 preamble sequence bits, 256 training PN code bits, and 1,772 data bits. Accordingly, the analog front-end must achieve its steady state in $5\mu s$, i.e., 25 symbol periods of the preamble signal. To speed up the acquisition process of the conventional feedback-type AGC system and less sensitive to environmental and process variations, a dual-bandwidth AGC VLSI architecture is proposed as shown in Fig.1. The architecture and circuit designs are described in the following.

2.1 Architecture

The proposed AGC comprises a forward path and a feedback path that automatically regulate the loop bandwidth. The forward path includes a variable gain amplifier (VGA), a shaping filter, and a gain/buffer, whereas the feedback path contains an envelop detector, a switch, and two integrators. These two integrators with different unity-gain frequencies provide two different corresponding loop bandwidth coefficients for the AGC. In the beginning of the loop acquisition when the AGC output magnitude error is large, the wider integrator A dominates the loop response for fast convergence. When the output signal gradually approaches the reference value V_{ref}, the small unity-gain frequency in-

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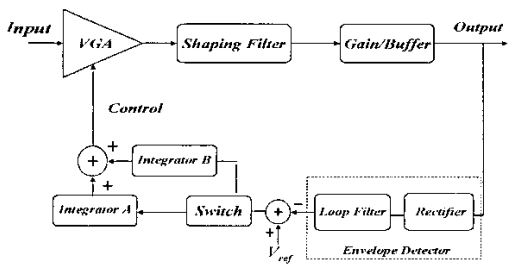


Figure 1: Block diagram of the dual loop AGC.

tegrator B operates instead. With this narrow AGC loop-bandwidth, a better noise immunity and a less jitter AGC control signal will be achieved in the steady state.

In order to analyze the loop behavior, an s-domain approximation linear model of the proposed dual bandwidth AGC is shown in Fig.2. K_f denotes the lumped gain of the

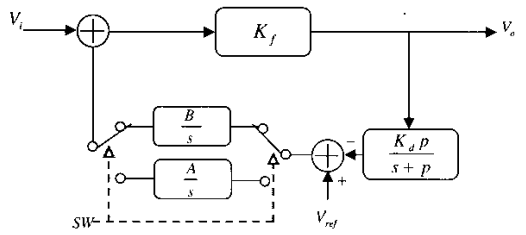


Figure 2: The analytic model of dual loop AGC.

forward path and $\frac{K_d P}{s+P}$ characterizes the loop filter. The transfer function of the output signal V_o with respect to the reference voltage V_{ref} can be derived as:

$$\begin{aligned} H(s) &= \frac{V_o}{V_{ref}} = \frac{K_f Q(s+p)}{s^2 + ps + K_f K_d PQ} \\ &= \frac{K_f Q(s+p)}{s^2 + 2\zeta\omega_n s + \omega_n^2} \end{aligned} \quad (1)$$

where $Q = A$ or B depending on whether integrator A or integrator B is turned on. It can be derived that the natural frequency ω_n is $\sqrt{K_f K_d pQ}$ and the damping factor ζ is $\frac{p}{2\sqrt{K_f K_d PQ}}$. Based on system simulation, the system requires $\omega_n = 500kHz$ for the wide loop bandwidth and $\omega_n = 50kHz$ for the narrow one. Setting the pole of the loop filter being $p = 2\pi \times 1MHz$, it may be determined that the unity gain frequencies of integrator-A is 600kHz and that of integrator-B is 75kHz.

2.2 Variable Gain Amplifier

Conventional CMOS variable gain amplifier (VGA) circuits regulate their gains by adjusting the degeneration resistance or load resistance, which results in a linear control characteristic. However, a VGA with exponential gain-control function is required for its wide control range and constant loop gain which results in invariant settling time [1]. Due to the intrinsic lack of logarithmic characteristics of CMOS device in strong inversion, a pseudo-exponential transfer function, $\sqrt{\frac{1+x}{1-x}}$, is used to approximate the exponential control curve. This approximation is based on the square-law relationship of MOSFET device. It can be derived that the approximation error is less than 1dB for x up to ± 0.7.

Fig.3 shows the circuit diagram of CMOS VGA with the pseudo-exponential gain characteristic with respect to V_C. The gain cell comprises a differential pair, a controllable current bias and two diode-connected transistor loads. The bias current, $2I_b + 2I_x$ is mirrored from the bias-and-control stage. The same amount of current is mirrored to transistors $M9^+$ and $M9^-$ of current source stage by transistors $M7$ and $M8$. With the fixed bias voltage, V_{bias2}, the tail current of the current source stage provided by M_{11} remains at $4I_b$. This forces the currents through M_{10}^+ and M_{10}^- to be $2I_b$ and the additional $2I_x$ from the drain of M_9^+ and M_9^- to flow through MN^+ and MN^- of the gain stage. Consistent with KCL theorem applied on the drain of MN^+ and MN^-, currents through the diode-connected load MP^+ and MP^- are $I_b - I_x$.

The signal gain is the ratio of the input transconductance and the load transconductance, which can be derived as

$$\begin{aligned} Gain &= \frac{V_{out}}{V_{in}} = \frac{g_{mn}}{g_{mp}} \\ &= \frac{\sqrt{2\mu_n C_{OX}(\frac{W}{L})_N}}{\sqrt{2\mu_p C_{OX}(\frac{W}{L})_P}} \sqrt{\frac{I_b + I_x}{I_b - I_x}} \\ &= K\sqrt{\frac{1+x}{1-x}} \end{aligned} \quad (2)$$

where $K = \frac{\sqrt{2\mu_n C_{OX}(\frac{W}{L})_N}}{\sqrt{2\mu_p C_{OX}(\frac{W}{L})_P}}$ and $x = \frac{I_x}{I_b}$. The control current $I_c = 2I_b + 2I_x$ has a linear relationship with the control voltage V_c as

$$2I_x = \frac{1}{2} g_m \times V_c \frac{(\frac{W}{L})_3}{(\frac{W}{L})_2} \quad (3)$$

By cascading two gain stages, the VGA provides voltage gain from -7dB to 13dB with 100 MHz bandwidth with 1-pF loading and 20 dB dynamic range with respect to -47dB THD.

2.3 4th Order Bessel Bandpass Filter

The 4-PPM 10Mb/s input signal is affected by interference under 50kHz caused by infrared emissions from fluorescent lights. A shaping filter must be designed to filter out the optical interference and higher order harmonics. In order to have better interference rejection for frequency below 50 kHz and linear phase response for PPM signals, a 4th-order Bessel band-pass filter with 5.5 MHz center frequency and 10 MHz bandwidth is designed. The filter consists of a 2nd-order high-pass filter cascaded by a 2nd-order low-pass filter. Using signal flow graph method, the fully differential 2nd-order high-pass and the 2nd-order low-pass filters are realized by OTA-C circuits as shown in Fig.4 and Fig.5 respectively.

2.4 Gain/Buffer

To amplify the signal from $100mV_{pp}$ to $1V_{pp}$, a broadband amplifier with 100 MHz bandwidth and 20 dB gain is designed as shown in Fig.6 [2]. It is composed of a transcon-

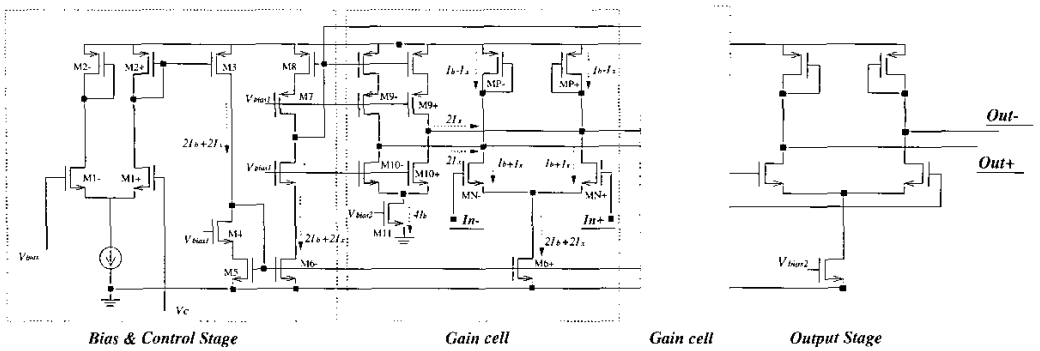


Figure 3: Exponential-type VGA

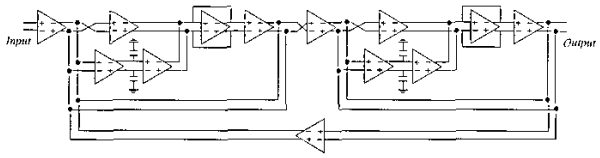


Figure 4: 2nd-order Bessel high pass filter

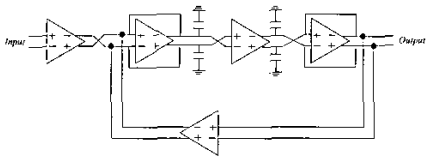


Figure 5: 2nd-order Bessel low pass filter

ductance stage, a current amplification stage, and a transimpedance stage. The input voltage signal is firstly converted to current by a source coupled pair and then amplified by two current mirrors, M2-M3 and M4-M5. Finally, the signal is converted back to voltage by the transimpedance stage composed of M7 and M8. The voltage gain of this block can be described as

$$A_{gb} = G_{m1} \times A_{i1} \times A_{i2} \times R_z \tag{4}$$

The current gains, A_{i1} and A_{i2}, are achieved by the device ratios of current mirrors M2, M3 and M4, M5. With shunt-shunt feedback connection [2], R_Z is the transimpedance

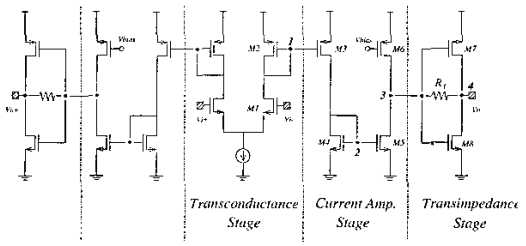


Figure 6: Gain/buffer circuit

value as

$$R_z = \frac{A}{1 + A\beta} = R_t \frac{g_m R_t}{1 + g_m R_t} \tag{5}$$

where g_m is the sum of M7 and M8 transconductance values and R_t is realized by a PMOS transistor biased at triode region. The circuit yields wide bandwidth for its low impedance at each node of the transconductance stage and current amplification stage. The impedances at node 3 and node 4 are reduced by a factor of $(1 + A\beta)$, which shifts the poles at node 3 and 4 to higher frequencies.

2.5 Feedback path

The feedback path consists of a magnitude detector, a loop filter, and switch circuit that provide the integration function of two different unity gain frequencies. The adopted non-coherent envelope detection comprises a rectifier followed by a loop filter as shown in Fig.7. The rectifier is an alternating voltage follower configuration [4] that extracts the output signal from the common source node. The 1st-order loop filter is realized by a simple RC constant configuration with a pole $\frac{g_m}{C}$ at 1 MHz.

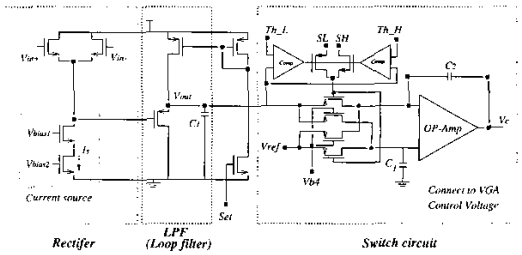


Figure 7: Feedback path of AGC

The voltage difference between the output signal envelope $V_{o,det}$ and the reference signal V_{ref} is retrieved and integrated by an OP-based integrator. To linearize the MOS resistors in the integrator, the double-MOSFET method [3] is adopted. The switch and two integrators are realized by a proposed switched integrator technique. It firstly compares the output magnitude with threshold voltages $V_{th,L}$ and $V_{th,H}$ and then applies one of the two bias voltages to the MOS-resistors so as to assign the unity gain frequency parameter of the integrator.

The designed op-amp is a two-stage configuration with 68 MHz unity-gain frequency. The switched integrator changes the unity gain frequency 600 kHz and 75 kHz respectively according to the outputs of the comparators. This mechanism is used to yield a large unity gain frequency at the initial acquisition state and a small unity gain frequency at the steady-state for the dual-loop AGC.

3. POST LAYOUT SIMULATION RESULTS

Fig.8 shows the chip layout of the proposed dual-loop AGC which consists of VGA, BPF, gain/buffer, rectifier, loop filter and switch circuit. The AGC is realized in a $0.6\mu m$ SPTM CMOS technology with $1,800 \times 1,800\mu m^2$ chip area. Fig.9 shows the dual-loop switching behavior. As the input signal magnitude changes abruptly, the comparator will change the MOSFET resistor biasing voltage and induce the commutation of the two feedback loops. The constant output magnitude can be demonstrated in Fig.10 with input signal strength from $40mV_{pp}$ to $400mV_{pp}$. The AGC has an acquisition time less than $5\mu s$. The overall chip performance is summarized in Table1.

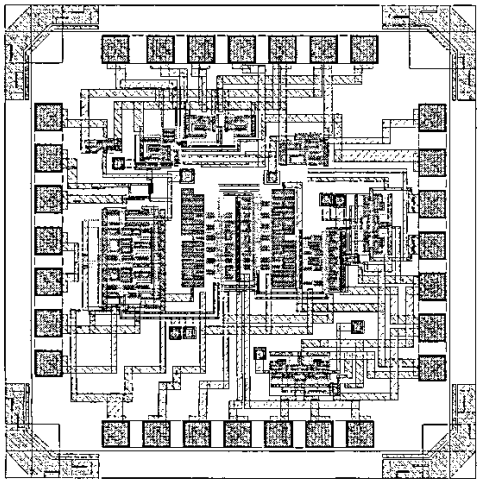


Figure 8: chip layout of dual loop AGC.

Power supply	3.3V
Technology	TSMC $0.6\mu m$ SPTM CMOS
VGA dynamic range	$> 20dB(40mV_{pp} \sim 400mV_{pp})$
VGA output	$180mV_{pp}$
VGA bandwidth	100MHz @ 0.1-pF loading
Constant AGC output	$1V_{pp}$
SNR	52dB @ 10-pF loading
THD	$-33dB@10MHz, 200mV_{pp}$
Wide loop bandwidth	500kHz
Narrow loop bandwidth	50kHz
Power consumption	80mW

Table 1: Performance summary of the post-layout simulation results

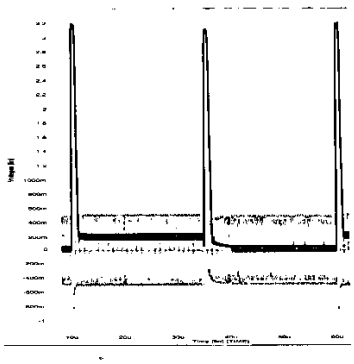
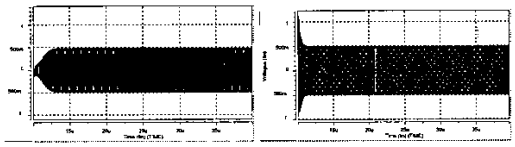


Figure 9: The switching behavior of the two feedback loops.



(a) $40mV_{pp}$ input (b) $400mV_{pp}$ input

Figure 10: Constant $1V_{pp}$ magnitude output with respect to different input signal strength.

4. CONCLUSION

A dual-loop AGC architecture has been proposed for the high speed 10Mbps infrared communication analog front-end circuit. With 500kHz wide loop bandwidth at the initial acquisition state and 50kHz narrow loop bandwidth at the steady state, the AGC achieves $5\mu s$ fast convergence time and maintains noise immunity. It provides $1V_{pp}$ magnitude for 20dB input strength range and consumes 88mW power including the driving buffer.

5. ADDITIONAL AUTHORS

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