Compact Current Model for Mesa-Isolated Fully-Depleted Ultrathin SOI NMOS Devices Considering Sidewall-Related Narrow Channel Effects

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Abstract

This paper presents the sidewall-related narrow channel effects on the current conduction in mesa-isolated fully-depleted ultra-thin SOI NMOS devices. As verified by the 3D simulation results, the closed-form analytical model predicts that in the subthreshold region the channel current near the sidewall dominates due to narrow channel effects.

Summary

For deep-submicron SOI CMOS devices, small geometry effects are gradually receiving substantial attention due to the progress of the processing technology [1]. Compact threshold voltage models considering short-channel effect or narrow-channel effect based on 2D analysis have been reported [2][3]. However, for studying the latter effect on the current conduction of a small-geometry MOS device, 3D device simulation is required [4]. In this paper, an analytical sidewall-related narrow-channel effect current conduction model for mesa-isolated fully-depleted ultrathin SOI NMOS devices is described. Fig.1 shows the mesa-isolated ultrathin SOI NMOS device under study. Fig.2 shows the 3D electron density contours in the thin-film of the ultrathin SOI NMOS devices with different channel widths based on the 3D simulation results. As shown in the figure, the distribution of the electron density is not uniform in the y-direction at the thin-film surface. At the location near the sidewall the electron density is higher— the sidewall induced electrons are important. With a narrower channel, the sidewall induced electrons are more important in affecting the current conduction. In the analytical current conduction model presented in this paper, the non-uniformity in the electron density profile due to the influence of the sidewall oxide is considered. In order to the simplify the analysis, the y-direction of the channel is divided into two portions: (1) the center portion ($I_{D,center}$) and (2) the sidewall portion ($I_{D,edge}$). In the center portion, the electron profile is assumed to be uniform. In the sidewall portion, the electron density is higher than that in the center portion. Based on Ref.[3], the threshold voltages of the center portion ($V_{TH,center}$) and the sidewall portion ($V_{TH,center}$) are derived as shown in Fig.3. Fig.4 shows the drain current versus the gate voltage of the ultrathin SOI NMOS device based on the analytical model and the 3D simulation results. As shown in the figure, from the $I_{D,edge}$ and $I_{D,center}$ curves, the threshold voltage of the sidewall portion is smaller than that of the center portion. Therefore, in the subthreshold region, the drain current of the sidewall portion ($I_{D,edge}$) dominates. At a large V_G in the strong inversion region, the dominance of the center portion drain current ($I_{D,center}$) can be identified. From this figure, the drain currents in both the center and the sidewall portions should be considered simultaneously, especially in the moderate inversion region when the gate voltage is near the threshold voltage. Fig.5 shows the drain current versus the gate voltage of the ultrathin SOI NMOS devices with different channel widths based on the analytical model and the 3D simulation results. As shown in the figure, when the channel width is scaled down, the sidewall effect is more important. Figs.6 show the drain current versus the gate voltage of the ultrathin SOI NMOS devices with channel widths of $2.4\mu m$ and $0.3\mu m$ and (a) different gate and sidewall oxide thicknesses, (b) different thin-film thicknesses, (c) different thin-film doping densities based on the analytical model and the 3D simulation results. As shown in Fig.6(a), when the front oxide (t_{ox1}) and the sidewall oxide (t_{sw}) become thicker, the subthreshold region with its drain current less sensitive to the channel width becomes larger. This implies that when the thickness of the front oxide (t_{ox1}) increases, the threshold voltages of both the center and the sidewall portions ($V_{TH,center}$, $V_{TH,edge}$) increase. However, the increase in the threshold voltage of the center portion ($V_{TH,center}$) is larger. Therefore, the difference between $V_{TH,center}$ and $V_{TH,edge}$ becomes wider. As shown in Figs.6(b)&(c), when the thickness of the thin-film (t_{si}) becomes thinner or the doping density of the thin-film (N_{si}) becomes lighter, their subthreshold curves are sensitive to the channel width. This implies that at a thinner thin-film or at a more lightly doped thin-film, the threshold voltages of both the center and the sidewall portions ($V_{TH,center}$, $V_{TH,edge}$) become smaller. In addition, the magnitude of the shrinkage of the threshold voltage of the center portion ($V_{TH,center}$) is larger, therefore, the difference between $V_{TH,center}$ and $V_{TH,edge}$ shrinks. Under this situation, the total subthreshold current is not dominated by the edge portion ($I_{D,edge}$).

References

[1]C.Teng, et.al., *SOI Conf.Tech.Dig.*, p.26,95. [2]J.G.Fossum, et.al., *IEEE TED*, p.866,88. [3]J.B.Kuo, et.al., *Sol.St.Elec.*, p.1321,96. [4]J.P.Krusius, et.al., *IEEE TED*, p.1274,96.

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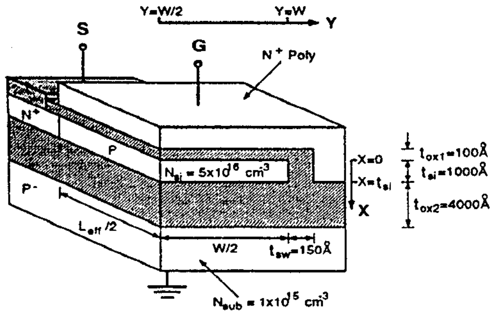


Figure 1: Cross section of the mesa-isolated ultrathin narrow-channel SOI NMOS device under study.

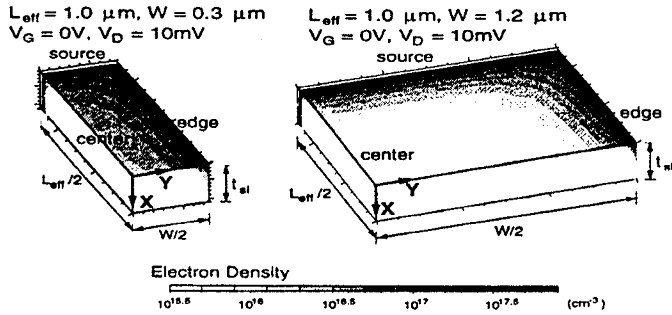


Figure 2: The 3D electron density contours of the ultrathin SOI NMOS devices with channel widths of $0.3\mu m$ and $1.2\mu m$, biased at $V_G = 0V$ and $V_D = 10mV$ based on the 3D simulation results.

$$
\begin{aligned}
V_{TH,center} &= V_{FB} + \phi_G - \phi_{si}, \qquad (1)\\
\phi_G &= \frac{-\phi_{si}(1+\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}}) - \phi_{s3}\frac{C_{si}}{C_{ox1}}(1-\alpha') + \frac{qN_a t_{si}^2}{2\epsilon_{si}}\frac{C_{si}}{C_{ox1}}(1+2\frac{C_{si}}{C_{ox2}})(1-2\alpha)}{1+\alpha'\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}}},\\
\alpha &= ((1-\frac{C_{si}}{C_{sw}}\frac{t_{si}}{l_0})e^{-W/2l_0} + (1+\frac{C_{si}}{C_{sw}}\frac{t_{si}}{l_0})e^{W/2l_0})^{-1},\\
\alpha' &= \alpha \cdot \frac{t_{si}^2}{l_0^2}\frac{(\gamma+\frac{C_{si}}{C_{ox1}})(1+2\frac{C_{si}}{C_{ox2}})}{1+\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}}},\\
l_0 &= t_{si}\sqrt{\frac{(\gamma-\gamma^2)+(1-\gamma^2)\frac{C_{si}}{C_{ox1}}+(2\gamma-\gamma^2)\frac{C_{si}}{C_{ox2}}+2\frac{C_{si}}{C_{ox1}}\frac{C_{si}}{C_{ox2}}}{2(1+\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}})}}.
\end{aligned}
$$

$$
\begin{aligned}
V_{TH,edge} &= V_{FB} + \phi'_G - \phi_{si}, \qquad (2)\\
\phi'_G &= \frac{-\phi_{si}(1+\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}}) - \phi_{s3}\frac{C_{si}}{C_{ox1}}(1-\beta') + \frac{qN_a t_{si}^2}{2\epsilon_{si}}\frac{C_{si}}{C_{ox1}}(1+2\frac{C_{si}}{C_{ox2}})(1-2\beta)}{1+\beta'\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}}},\\
\beta &= \alpha \cdot cosh(\frac{W}{2l_0}), \qquad \beta' = \alpha' \cdot cosh(\frac{W}{2l_0}).
\end{aligned}
$$

Figure 3: The analytical model.

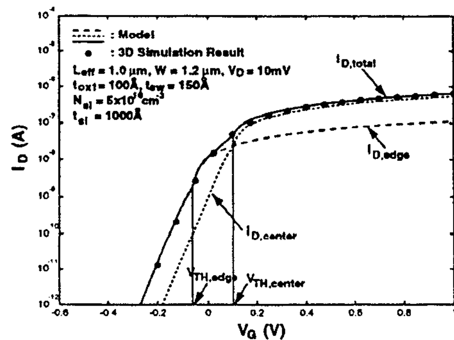


Figure 4: The drain current versus the gate voltage of the ultrathin SOI NMOS device with a channel length of $1\mu m$ and a channel width of $1.2\mu m$ based on the analytical model and the 3D simulation results.

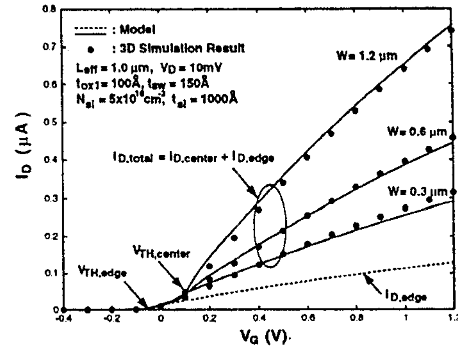
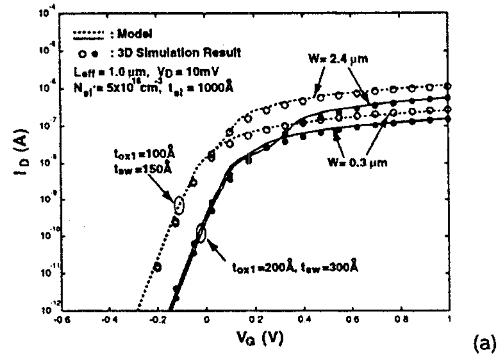
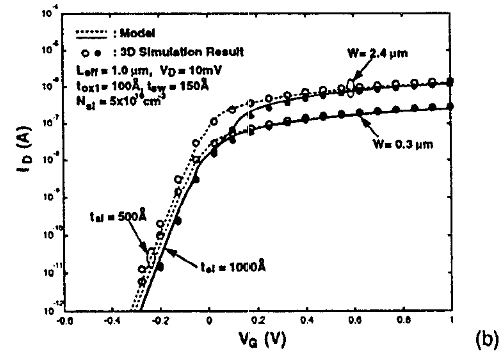


Figure 5: The drain current versus the gate voltage of the ultrathin SOI NMOS devices with a channel length of $1\mu m$ and channel widths of $1.2\mu m$, $0.6\mu m$ and $0.3\mu m$, biased at $V_D = 10mV$, based on the analytical model and the 3D simulation results.





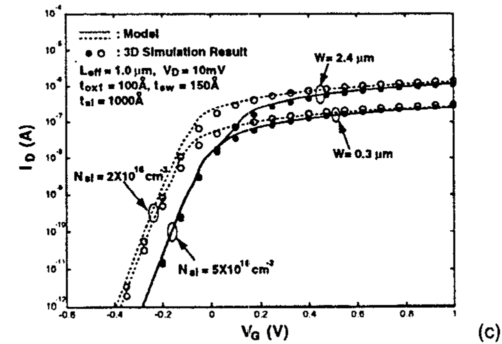


Figure 6: The drain current versus the gate voltage of the ultrathin SOI NMOS devices (a) with different gate oxide thicknesses and sidewall oxide thicknesses, (b) with different thin-film thicknesses, (c) with different thin-film doping densities based on the analytical model and the 3D simulation results.