A 1.7~3.125Gbps Clock and Data Recovery Circuit Using a Gated Frequency Detector

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Abstract

A fully integrated clock and data recovery (CDR) circuit with the proposed gated frequency detector (GFD) is presented. It has been realized in a standard 0.25-um CMOS technology. The proposed voltage-controlled oscillator (VCO) can achieve wide operation range and small K_{VCO} by employing the analog/digital dual loop architecture. It can relax the constraint on choosing the loop parameter to reduce the size of the on-chip capacitor. The proposed GFD will make the frequency lock time fixed and can avoid the harmonic locking problem for wide data rate operations. All measured BERs are less than 10^{-12} with the data rate from 1.7Gbps to 3.125Gbps.

1. Introduction

The requirements for faster information exchanging have led to the demand for high speed data communications. Various researches focus on high speed transceivers, especially the clock and data recovery (CDR) circuits [1-2]. For a conventional charge-pump CDR with the loop filter of R_P in series of C_P, the natural frequency, ω_n, and the damping ratio, ζ, of the closed loop transfer function can be represented as [3]

$$\omega_n = \sqrt{\frac{I_P D_T K_{VCO}}{2\pi C_P}}, \quad (1)$$

$$\zeta = \frac{R_P}{2}\sqrt{\frac{I_P D_T C_P K_{VCO}}{2\pi}}. \quad (2)$$

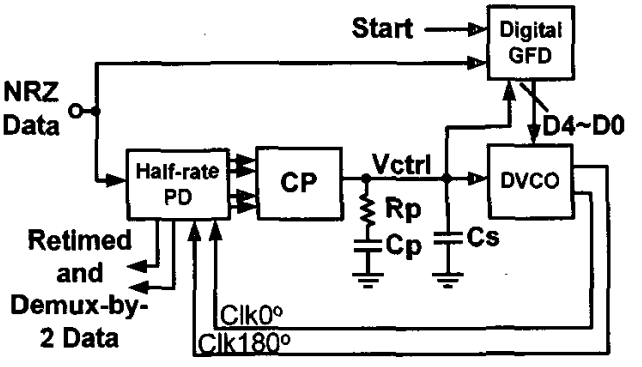


Fig. 1 Half-rate CDR architecture.

where I_P is charge pump current, D_T is input data transition density and K_{VCO} is VCO gain. Usually, the tuning range of a VCO should be large enough to overcome the process, voltage and temperature variations, i.e., K_{VCO} will be large. A large C_P might be needed to reduce loop bandwidth for jitter suppression. To let the natural frequency and damping ratio remain constant, if K_{VCO} is reduced by a factor of k, C_P can be reduced by the same factor. It can reduce the die area. In order to reduce the K_{VCO}, a wide tuning range VCO with analog/digital dual-controlled mechanisms is proposed.

In recent years, the concept of intellectual property (IP) has grown rapidly. To be a reusable IP, CDRs must have wide operation range for different data-rate applications. Intuitively, one can increase the tuning range of the voltage-controlled oscillator (VCO) to enlarge the possible operation range. In wide data-rate applications, CDRs have to extract embedded clock information from the preamble data. A wide range frequency detector will be

required. Harmonic locking issue will make CDR circuits difficult to differentiate the situations between slow data rate and consecutive data. Although digital quadricorrelators [4, 5] can be used in frequency acquisition, it will take hundreds of preamble data until the frequency lock is achieved. Moreover, when the initial frequency difference is large, harmonic locking would happen for digital quadricorrelators. To avoid this predicament, a digital gated frequency detector (GFD) is presented to acquire random data without harmonic locking issue.

2. Circuit Description

The proposed fully integrated CDR circuit is shown in Fig. 1. It consists of a digital GFD, an analog/digital dual-controlled VCO (DVCO) and a linear half-rate phase detector (PD) [1]. To receive the data, the signal, *Start*, is set to low to clear the GFD. The proposed GFD consists of two gated oscillators (GOs), a voltage-controlled delay line (VCDL), a phase comparator (PC), a 5-bit successive approximation register-controlled (SAR)

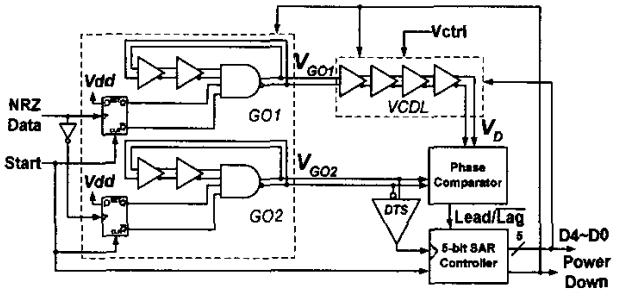


Fig. 2 The proposed GFD.

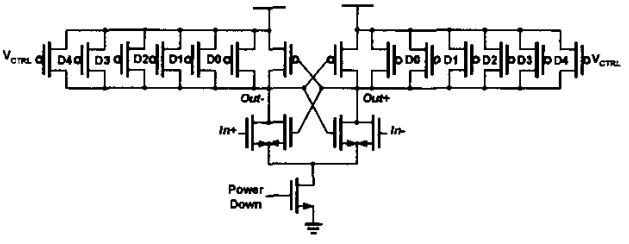


Fig. 3 Delay cell of VCO and VCDL.

[6] controller and a differential to single-ended (DTS) buffer, as shown in Fig. 2. The delay cells in the VCDL, as shown in Fig. 3, are identical to those in the VCO. The only difference between them is that the signal, *PowerDown*, of the delay cells in the VCO is connected to power supply while that in the VCDL is controlled by the 5-bit SAR controller.

In order to operate correctly, the preamble signal is needed as shown in Fig. 4. Suppose that the first two data are "10", i.e., logic one followed with a logic zero and the remaining preamble signal can be random data or periodic data of 1010.... The two GOs would be triggered by the first rising and falling edges of the preamble signal, respectively. Assume these two GOs are identical and they will oscillate at the same frequency and keep a constant phase difference. Since the time difference between the first rising and falling edges of the preamble is equal to a bit time, the phase difference between V_{GO1} and V_{GO2} would be the same. The signal V_D is generated by the VCDL from the signal V_{GO1}. The PC will compare the phase relation between the signals V_D and V_{GO2}. V_{GO2} through the DTS buffer triggers the 5-bit SAR controller to adjust the VCDL. If V_D is aligned with V_{GO2}, the delay time, T_D, of the VCDL would be close to a bit time. In other words, if these delay cells are connected as a ring oscillator, it will oscillate close to half data rate. After the 5-bit binary searching is finished, the controller will turn off the GOs and the VCDL to reduce the power consumption.

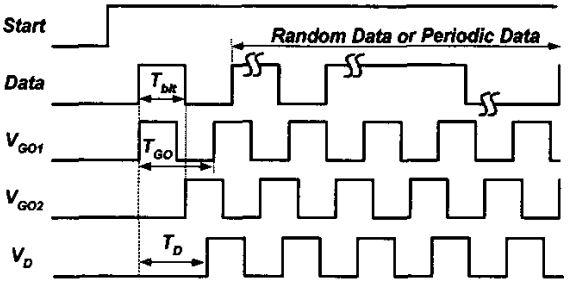


Fig. 4 Timing diagram of digital GFD.

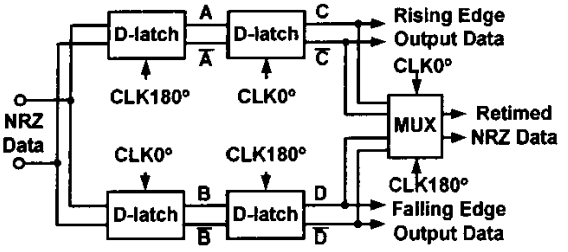


Fig. 5 Phase detector with MUX in [1].

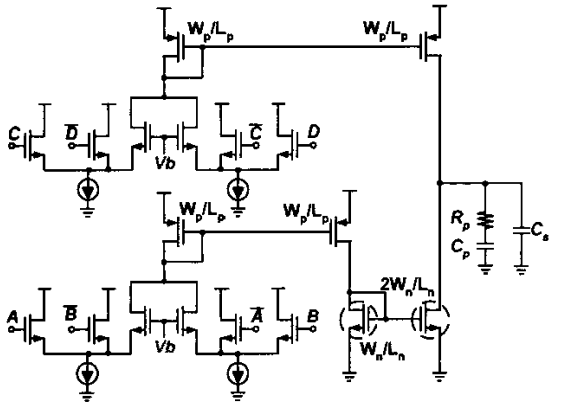


Fig. 6 Current mode XOR gates [1] with modified charge pump.

A linear half-rate PD [1] is employed in this work as shown in Fig. 5. Conventional static and dynamic logics cannot perform phase detection for such a high speed. To extract high speed phase information, all logic components in Fig. 5 are implemented in current mode logic (CML) [7]. The current mode XOR gates [1] with the modified charge pump are implemented as shown in Fig. 6 to achieve high speed operation. The symmetry configuration could reduce the loading mismatch of phase detector.

3. Experimental Results

The proposed CDR has been fabricated in a standard 0.25-μm CMOS technology. All the passive elements are integrated with active elements. Fig. 7 shows the die photograph. This CDR consumes 200mW from a single 2.5V supply at the data rate of 3.125Gbps and occupies a chip area of $1.5 \times 1.8\text{mm}^2$. Fig. 8 illustrates the measured transient response for the GFD at the data rate of 2.5Gbps. The operating frequency of the digital GFD is 500MHz. The signal, *PowerDown*, of the GFD will switch from logic one to logic zero and thus turn off the GOs and the VCDL after 5 cycles of the GO.

Figs. 9(a) and 9(b) illustrate the retimed data and clock when the CDR locks to 1.7Gbps and 3.125Gbps NRZ data with a PRBS of 2^7-1, respectively. The measured rms and peak-to-peak jitters from 1.7Gbps to 3.125Gbps are below 7.4 ps and 62.2 ps, respectively. The measured jitter transfer functions for all data rates are almost the same because the K_{VCO} is nearly constant. The bit-error-rate (BER) testing time was set to be 20 minutes and no error occurred.

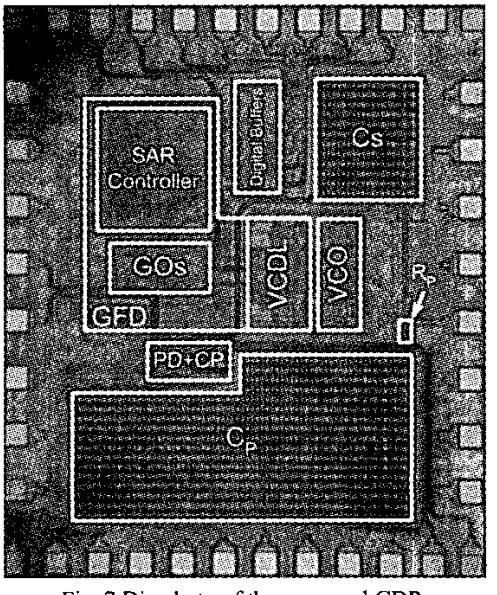


Fig. 7 Die photo of the proposed CDR.

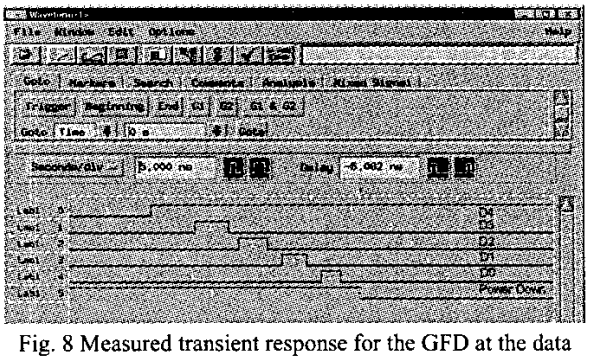
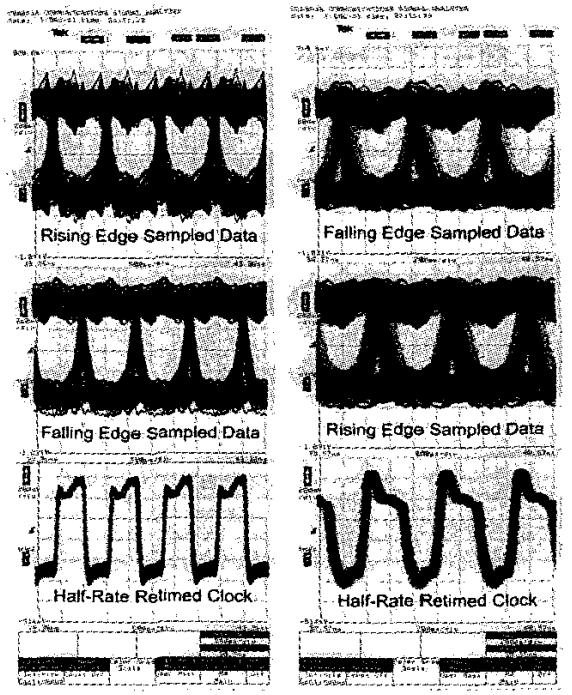


Fig. 8 Measured transient response for the GFD at the data rate of 2.5Gbps.



(a) (b)

Fig. 9 Retimed data and clock at the data rate of (a) 1.7Gbps (b) 3.125Gbps.

The measured BERs are all smaller than 10^{-12}. Table 1 gives the performance summary of this work.

4. Conclusions

A 1.7~3.125Gbps CDR circuit is realized in a 0.25-μm standard CMOS technology. The DVCO incorporating with the proposed wide range GFD can achieve both small K_{VCO} and wide operation range without harmonic locking issue. This dual loop architecture can relax the loop parameter and further reduces the area of on-chip capacitor. The GFD has a fixed lock time which is independent of data pattern. All the measured BERs are less than 10^{-12} at the data rate from 1.7Gbps to 3.125Gbps.

5. Acknowledgement

The authors would like to thank Chip Implementation Center (CIC) of National Science Council, Taiwan, for fabricating this chip.

Table 1 Performance Summary

Technology	Standard 0.25um 1P5M CMOS	
Power Supply	Single 2.5V	
Chip Area	1.5 mm x 1.8 mm	
Power Consumption	VCO	43mW~87mW
	PD + CP	15mW
	Digital Buffers	57mW~98mW
	GFD	125mW
	Total (GFD Off)	115mW@1.7Gbps
		157mW@2.5Gbps
		200mW@3.125Gbps
RMS Jitter	7.4ps @1.7Gbps	
	7.5ps @2.5Gbps	
	6.7ps @3.125Gbps	
Peak-Peak Jitter	62.2ps @1.7Gbps	
	61ps @2.5Gbps	
	60ps @3.125Gbps	

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