A 2-V CMOS 455KHz FM/FSK Demodulator using Feedforward Offset Cancellation Limiting Amplifier

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Abstract

This paper presents a low-voltage low-power IF 455KHz signal processor that contains a three-stage limiting amplifier and an FM/FSK demodulator. The limiting amplifier uses an on-chip feedforward offset cancellation circuit. The FM/FSK demodulator employs a quadrature detector that is composed of an on-chip phase detector and an external tank phase shifter. The demodulation constant is 20mV/KHz with maximum ±10KHz frequency deviation. The IF signal processor that consumes 2.3mW from a single 2-V power supply demonstrates a high sensitivity of -72dBm. It occupies an active area of 0.2mm^2 using 0.6μm digital CMOS technology.

Introduction

Fig. 1 shows the architecture of the CMOS IF 455KHz signal processor that can be applied to superheterodyne communication system such as pager. It contains two functions, namely, magnitude control and FM/FSK demodulation.

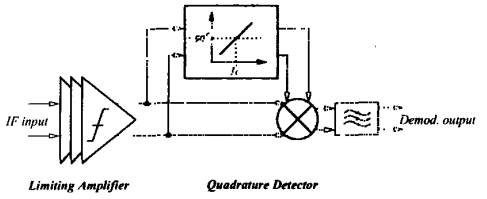

Figure 1: Architecture of IF 455KHz signal processor.

Limiting amplifier is selected as a magnitude control rather than AGC (Automatic Gain Control) because limiting amplifier handles larger dynamic range. However, DC offset is a major concern since it may be so large that reduces the sensitivity, and degrades the recovered data BER. Unlike conventional external passive approach, a feedforward offset cancellation technique is employed on chip at each gain stage of the amplifier, which exhibits instantaneous response and high level integration [1].

FSK (Frequency Shifting Keying) can be treated as a discrete FM signal. In general, FSK frequencies are usually equally spaced and centered at a nominal carrier frequency. A pager requires an FM/FSK demodulator with high frequency discrimination since the signal bandwidth of the FSK or 4-FSK is rather narrow. The FM/FSK demodulator employed is a quadrature detector [2], which is composed of an external tank phase shifting network and an integrated phase detector to achieve high discrimination function under low voltage operation.

The rest of this paper is organized as follows: Circuit designs of the proposed CMOS limiting amplifier and quadrature detector are described in Section II. In Section III experimental results are demonstrated. Finally, conclusions are drawn in Section IV.

Circuit Designs

Limiting Amplifier

Limiting amplifier is basically an amplifier chain that enlarges different magnitudes of input signal into saturation. This amplifier chain has to provide a small signal gain of 70dB, at least, in pager application in order to cover the required input dynamic range. At the same time, it has to yield a high pass function to alleviate the DC offset due to mismatch. The designed upper bandwidth is ten times of the IF 455KHz to reduce the AM-PM conversion effect [3], while the lower band is at 10KHz that causes little influence on data band near

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455KHz [4].

The proposed limiting amplifier as shown in Fig. 2 contains three stages of gain cell. The first two cells are identical and the third one comes with an auxiliary output driver. Feedforward offset cancellation technique instead of conventional negative feedback method is applied in this architecture [5].

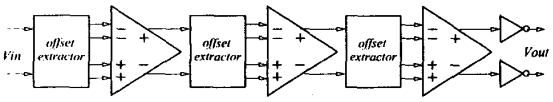


Figure 2: Block diagram of the limiting amplifier using feedforward offset cancellation at each gain cell.

The core of the amplifier, as shown in Fig. 3, is composed of two cross-connected source-coupled pairs with two differential input pairs M_1-M_4. This source-coupled pairs are all connected to the preceding stage. Besides, an R-C network is inserted at input of each pair, which is the offset extraction circuit. When input frequency is beyond the R-C cutoff frequency, this circuit structure can be equivalent to a conventional source-coupled pair. On the other hand, when the input frequency is below the R-C cutoff frequency, the offset voltage associated with the common mode voltage generated from the previous stage will store at the capacitor. Thus, the two source-coupled pairs have different input common mode voltages. Due to cross-connected mechanism, the amplifier will cancel the offset voltage presented at the input, while the offset generated in the current stage will be cancelled at the following stage. This technique gives instantaneous response since the offset extractor circuit of each stage only needs to extract the offset voltage generated by the preceding stage. Smaller value of capacitors and resistors at each gain cell can therefore be implemented on chip.

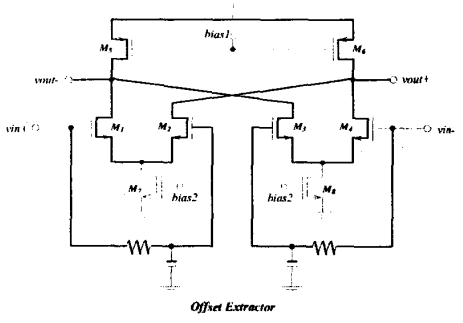


Figure 3: Gain cell of the limiting amplifier.

The large time constant RC network of the offset extractor is realized by a triode-biased PMOS resistor and an off-type PMOS gate-to-bulk capacitor in standard digital CMOS technology. The gate-to-bulk capacitance used is 2.3pF when PMOS ($320\mu m/10\mu m$) is at off region. The -3dB corner frequency is 10KHz of the formed high pass function. The designed offset cancellation range is $\pm$ 230mV, which is sufficient enough to cover the CMOS process variation that causes offset.

On the other hand, the high frequency roll-off of the gain stage is determined by the output impedance of the source-coupled pair and the associated parasitic capacitance, as shown in Equ. 1.

$$f_{-3dB} = \frac{1}{2\pi(r_{o1}//r_{o5}//r_{o3}) \cdot (C_{gd5} + C_{gd1} + C_{gd3})} \quad (1)$$

Considering the trade-off among the bandwidth, gain and power consumption, three-stage structure is selected. The identical first two stages provide 28dB differential voltage gain with 4.6MHz bandwidth. Two auxiliary output drivers, as shown in Fig. 2, are added at the last stage.

Quadrature Detector

The block diagram of the quadrature detector for FM/FSK demodulation is shown in Fig. 1. In this structure, a Phase Shifting Network (PSN) shifts the phase of incoming FM signal by an amount that is proportional to its instantaneous frequency. A Phase Detector (PD) is then used to detect the phase difference between the original FM signal and its phase shifted signal. Finally, a low-pass filter is used to remove high frequency noise and extract the demodulated output. This method converts deviation of the frequency into shifting of the phase. Equ. 2 is the phase response of the phase shift network, where f_c is the carrier frequency and K is a proportional constant. Therefore, appropriate value of the phase-shift can improve the frequency discrimination in demodulation.

$$\phi(f) = -\frac{\pi}{2} + 2\pi K(f - f_c) \quad (2)$$

Fig. 4 shows the proposed quadrature detector circuit. Differential circuit structure is employed. External tank circuits with Q of 20 and on-chip quadrature capacitors C_{q1} and C_{q2} are composed as phase shifting networks that provide a linear phase shift at the IF signal band. Gilbert-type phase detector is integrated for detecting the phase difference between the limiting amplifier output and the phase-shift network output waveforms. The upper two PMOS devices $M_1 - M_2$ driven by the limiting

amplifier output and lower four PMOS devices $M_3 - M_6$ connected to phase-shift networks outputs work as commutating switches. No tail current source is used in the phase detector because of low supply 2-V operation. A first-order external low pass filter at the phase detector output removes high frequency harmonics. Higher order low pass function may be required for different applications. The demodulated signal amplitude at filter output is proportional to the frequency deviation of the modulating signal.

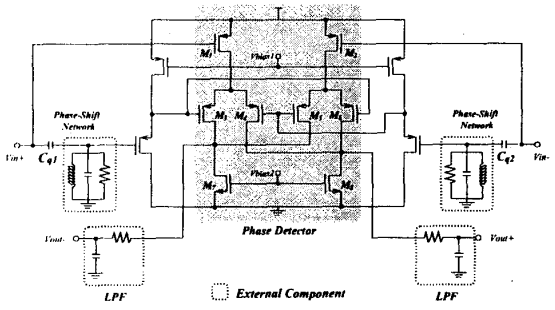


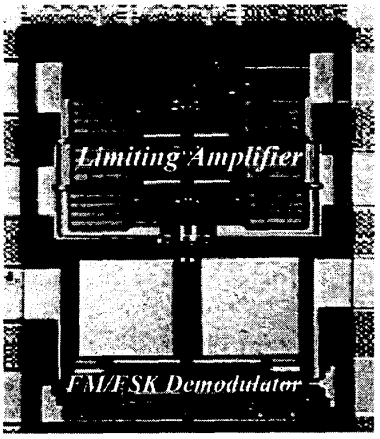
Figure 4: Circuit diagram of the quadrature detector.

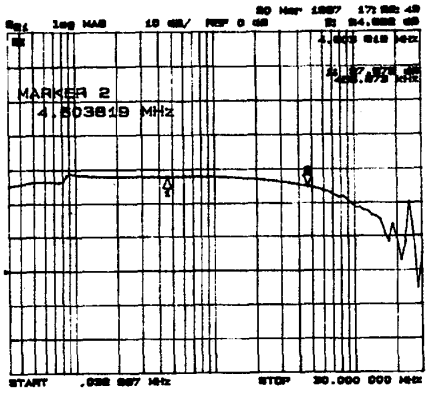
Experimental Results

Fig. 5 is the die photo of the IF 455KHz signal processor using 0.6μm single-poly double-metal digital CMOS technology. The active area is 0.2mm^2. Total circuits consume 1.15mA from a single 2-V power supply. The minimum supply voltage can be down to 1.8-V while the circuits still perform well. Fig. 6 shows the small signal frequency response of the limiting amplifier gain stage. Each stage provides a gain of 28dB with a bandwidth of 4.6MHz . The minimum detectable signal level, as shown in Fig. 7, is -72dBm when input impedance matches to 50Ω.

The measured demodulation constant of the quadrature detector, as shown in Fig. 8, is 20mV/KHz for IF 455KHz. The FM deviation range can be wider than 20KHz. Fig. 9 shows the demodulated baseband output with 200mV$_{pp}$ swing when 3.2KHz data rate, ±5KHz frequency deviation FM signal is applied. The demodulated signal for a 4-FSK (±1.6KHz, ±4.8KHz) input data is shown in Fig. 10. The four levels are all well separated by more than 70mV though whole measurements shown in this paper are single ended.

Table 1 is the summary of measured performance of the limiting amplifier and quadrature detector.





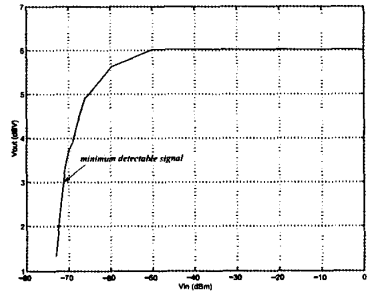


Figure 7: Measured sensitivity of the limiting amplifier.

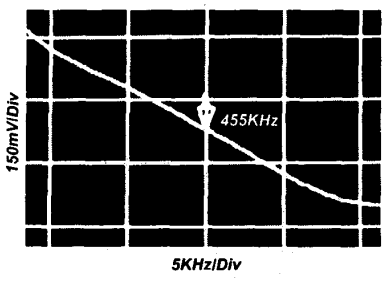


Figure 8: Measured FM demodulator output voltage versus input frequency deviation.

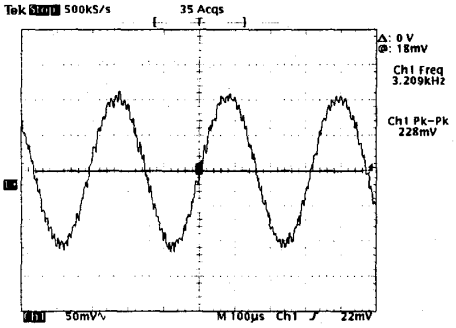


Figure 9: The demodulated 3.2KHz data rate FM output signal with frequency deviation of ±5KHz.

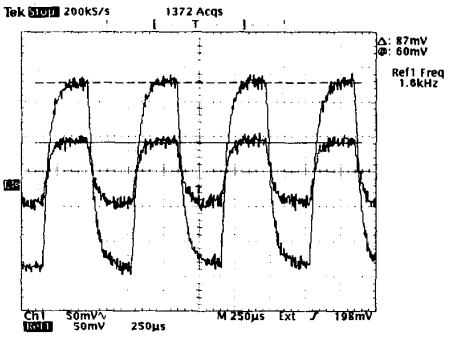


Figure 10: The demodulated 3.2Kbps 4-FSK output levels with frequency deviations of ±1.6KHz and ±4.8KHz.

Conclusions

A 2-V low-voltage low-power IF 455KHz signal processor that contains a limiting amplifier and an FM/FSK demodulator is presented. The limiting amplifier that employs feedforward offset cancellation technique at each of the three gain stages consumes less than 0.5mA. This limiting amplifier achieves a sensitivity of -72dBm. Passive offset-extraction network of each gain cell is integrated on the same chip. The quadrature detector that is composed of an external tank phase shifting network and an on-chip phase detector is adopted in FM/FSK demodulator. The demodulator processes a high demodulation constant of 20 mV/KHz and draws a current less than 0.7mA.

Technology	0.6μm CMOS
Limiting Amplifier	
single stage gain	28 dB
single stage bandwidth	4.6 MHz
sensitivity	-72 dBm@50Ω
Quadrature Detector	
demodulation constant	20 mV/KHz
max. freq. deviation	± 10KHz
Output LSB for 4-FSK signal	70 mV
Supply Voltage	2-V
Power Consumption	2.3mW

Table 1: Measured performances of the CMOS limiting amplifier and quadrature detector.

References

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