A 1.2V, 18mW, 10Gb/s SiGe Transimpedance Amplifier

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Abstract

To the authors' knowledge, the first 1.2V, 18mW, 10Gb/s SiGe transimpedance amplifier (TIA) is presented here. It has been realized in a 0.35μm SiGe process and its area is 0.45mm² with pads. Employing inductive series and shunt peaking techniques, the proposed TIA can achieve a transimpedance gain of 61.6dBΩ and the bandwidth of 7.4GHz, while dissipating only 18mW with 1.2V supply. With an equivalent photodiode capacitance of 0.15pF, this TIA shows the input referred noise current density of 22pA/ √Hz.

I. Introduction

The growing popularity of multimedia applications demands high data rate wired telecommunication systems. Many existing wired systems require 10Gb/s analog front-ends, such as OC192 for telecommunications and 10Gb/s Ethernet for data communications. The key requirements for designing a high-speed front-end are: 1) to integrate both the high-speed analog front-end and digital back-end and 2) low voltage and low power. Traditionally, analog RF front-end utilized high f_T transistors of GaAs. However, GaAs RF circuits could not be integrated with succeeding CMOS digital processors. With the past decade, there is a significant effort to implement the multi-gigabits optical front-ends [1]-[5] in BiCMOS and CMOS technologies. It can provide the advantages of high integration and low cost.

Conventional bandwidth-enhancement techniques, such as the regulated cascode topology [2] [3] and the negative feedback configuration [1], will suffer the limitation of the supply voltage. When the deep submicron technology advances further, the low supply voltage is indispensable. In this paper, a low-voltage and low power transimpedance amplifier (TIA) utilizes the inductive series and shunt peaking techniques to improve the overall bandwidth. To save the power dissipations, this proposed TIA can provide a high transimpedance gain without a power-hungry buffer because it uses the same gain stage to match a 50-ohm resistive load directly. A 1.2 V, 18mW, 10Gb/s SiGe transimpedance amplifier is implemented in a 0.35μm SiGe 3p3m process. Compared to the current high-speed TIAs [1]-[6], the proposed one can achieve the lowest supply voltage and lowest power consumption.

II. Circuit design

A. Low-voltage amplifier

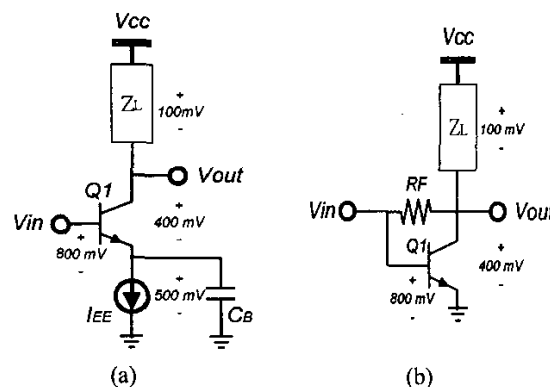To develop low-voltage analog and digital circuits is

Fig. 1 Common emitter amplifier (a) conventional topology (b) proposed low-voltage one.

of great interest. In [7], it is described that bipolar circuits have the innate DC headroom problem. For the bipolar transistors with a constant current density, the base-emitter voltage (V_{BE}) does not decrease with the scale-down technology and it has a turn-on voltage of 800mV. Besides, a minimum collector-emitter voltage (V_{CE}) around 400mV can protect high-speed bipolar transistors against heavy saturation. Under a supply voltage of 1.2V, the classical cascode amplifier using bipolar devices is forbidden. Fig. 1 illustrates two common emitter amplifiers. The evaluation of their minimum supply voltage for a low supply voltage of 1.2V and high-speed operation are considered. In the conventional topology of Fig. 1(a), it uses a bypass capacitor C_B and a tail current source I_{EE} that may occupy 500mV headroom in experience. Obviously, the sum of V_{BE} in Q1 and the voltage across the tail current source will exceed the supply voltage. Fig. 1(b) represents a shunt-shunt feedback amplifier with R_F, which can have a dc self bias and provide input matching. When the voltage swings across Z_L maintain as small as 100mV, it is sufficient to make the amplifier operated in the supply voltage below 1V operation.

Furthermore, the voltage gain for two common emitter amplifiers in Figs. 1(a) and (b) can be calculated. For the conventional common emitter amplifier in Fig. 1(a) with the bypass capacitor, C_B, the small-signal voltage gain can be

$$A = \frac{v_{out}}{v_{in}} = -g_m Z_L, \qquad (1)$$

where g_m is the transconductance. Since $g_m = I_C/V_T$, eq. (1) can be sequentially simplified as follows:
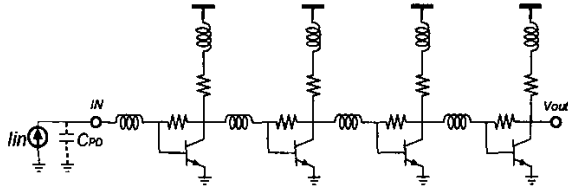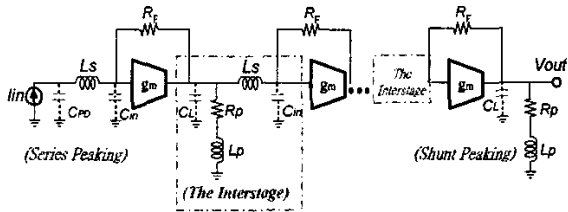
Fig. 2 The proposed TIA

Fig. 3 The small-signal model for the proposed TIA

$$\left| \frac{v_{out}}{v_{in}} \right| = \frac{Ic \cdot Z_L}{V_T} \quad (2)$$

where $V_T = kT/q$. In eq. (2), the sufficient voltage across Z_L can increase the gain and it is especially important for low-voltage amplifiers. Supposed that the impedance of Z_L is much smaller than R_F, the low-voltage topology in Fig. 1(b) can reach a similar voltage gain as Fig. 1(a). By means of Miller's theorem, the input impedance of the amplifier in Fig. 1(b) can be

$$R_{in} = \frac{R_F}{1 - A} = \frac{R_F}{1 + g_m Z_L} \quad (3)$$

Furthermore, this input impedance can be designed to match the input 50ohm termination according to eq. (3).

B. The proposed TIA

Based on Fig. 1(b), the proposed TIA is presented in Fig. 2 by using the inductive series and shunting peaking techniques [8]. Compared to the conventional TIAs [1-5], the proposed one can have several advantages: self-bias operation, low input impedance, and high gain for low-voltage and low-power applications.

The small-signal model for the proposed TIA is shown in Fig. 3. An inductor L_S can be inserted between a photodiode C_{PD} and a shunt-shunt feedback amplifier in order to increase the bandwidth. In practical, the core amplifier exhibits one pole system. Thus, series peaking with a damping factor of $1/\sqrt{2}$ can multiply the bandwidth by 1.4 times. The inductive shunting peaking technique is used in high-speed output buffers to ease the trade-off between output matching, speed, and voltage headroom. An inductor L_P in series with the resistance R_P can enlarge the
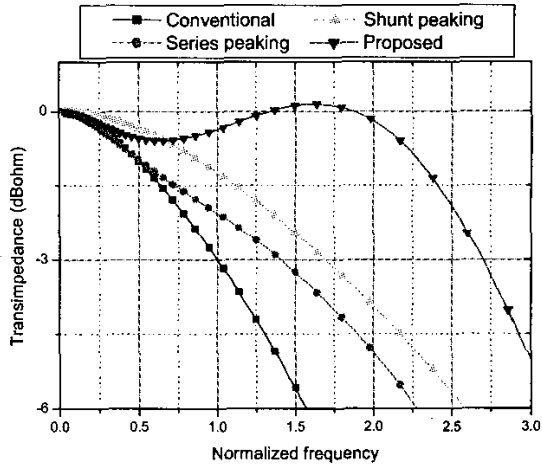

Fig. 4 Simulated bandwidths for the conventional TIA, the series peaking one, the shunting peaking one and the proposed one, respectively.

bandwidth. Therefore, the shunt peaking technique can also have a flat response to enhance the bandwidth by a factor of 1.7. The simulated bandwidth enhancement factors for the conventional TIA, the series peaking one, the shunting peaking one and the proposed one, respectively, are shown in Fig. 4. Compared to the conventional amplifier, the bandwidth enhancement factor for the conventional TIA, the series peaking one, the shunting peaking one and the proposed one is 1.4, 1.7 and 2.7, respectively. Obviously, the proposed TIA can have a larger bandwidth enhancement factor.

C. Devices selection for the proposed TIA

In considerations of DC biasing, the selection for the bipolar transistors should trade off among headroom of V_{CE}, collector current density (Jc), unity-gain frequency (f_t), gain, noise, and power consumptions. In addition, a bipolar device with Jc of 640 uA/um^2 is selected for the high-speed date rates of 10Gb/s. Each identical bipolar transistor in the proposed TIA obtains 1.1v headroom and achieves the current gain of 160 with f_t of 40GHz.

III. Experimental results

The proposed TIA has been implemented in a 0.35um 3P3M SiGe process and measured by on-wafer probing. Fig. 5 shows two TIAs: the top one is the proposed TIA with eight inductors and the bottom one is a series peaking TIA with four inductors. Due to high-speed considerations, the small inductors below 1nH are used. Two core circuits separately occupy the area of 900um × 400um and 900um × 200um, respectively. Operating from the supply voltage of 1.2V, both of them consume the same current of 15mA.
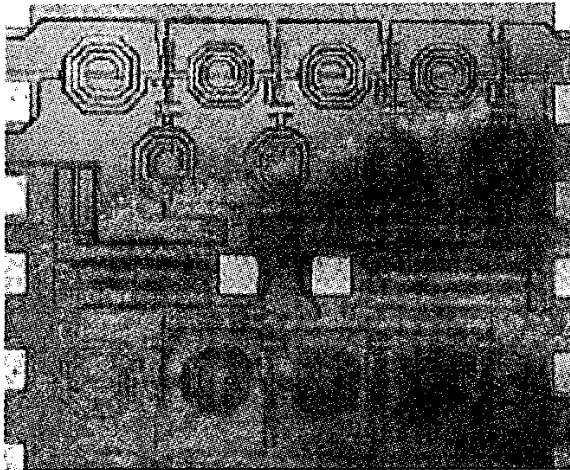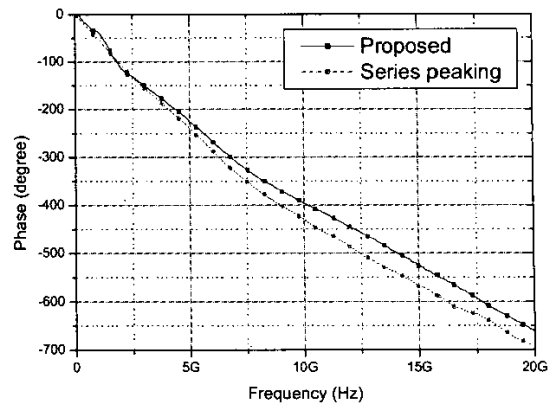
Fig. 5 The die micrograph for the proposed TIA (top) and the series peaking one (bottom).

With an equivalent photodiode capacitance of 0.15pF, both TIAs are measured by on-wafer probing. For a supply voltage of 1.2V, the measured transimpedance gain for the proposed TIA and the series peaking one is 61.6dBΩ and 58dBΩ, respectively, as shown in Fig. 6(a). The measured bandwidth, f_{3dB}, for the proposed TIA and the series peaking one is 7.4GHz and 4.4GHz, respectively. The measured bandwidth enhancement factor is 2.45 and 1.46 for the proposed TIA and the series peaking one, respectively. Fig. 6(b) illustrates the approximately linear phase response for both TIAs. Fig. 7 shows the transimpedance response for different power supplies. It is demonstrated that the proposed TIA can normally work 1.2V and further below 1V. Fig. 8 shows the measured frequency response for the proposed TIA under 1.2V, where s11 and s22 are almost below -10dB. When the supply voltage is 1.2V, the measured eye diagrams by PRBS of $2^{31}-1$ are shown in Fig. 9. It can achieve the highest data rate of 12.5Gb/s.

(b)

Fig. 6 (a) the measured transimpedance gain for the proposed TIA and the series peaking one.
(b) the measured phase response for the proposed TIA and the series peaking one.
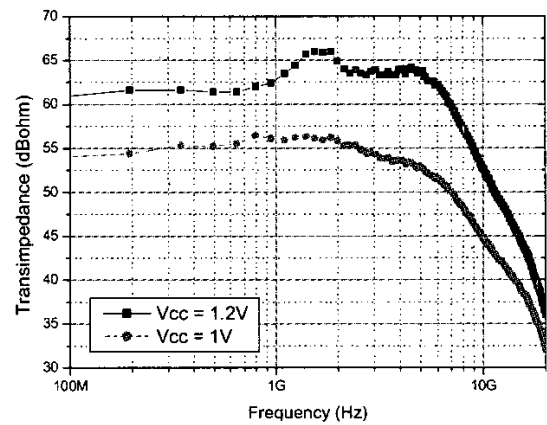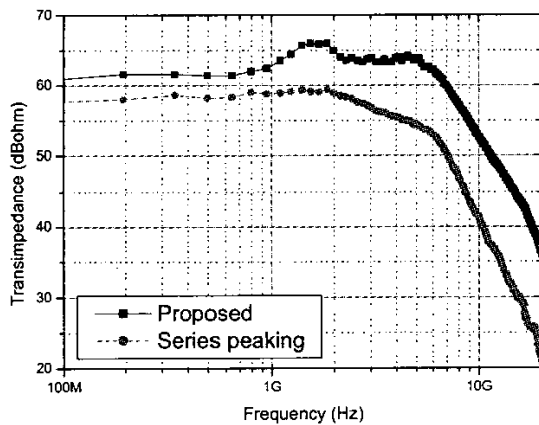

Fig. 7 Measured gain of the proposed TIA is 54.3 dBΩ and 61.6 dBΩ for 1V and 1.2V supply voltages, respectively.
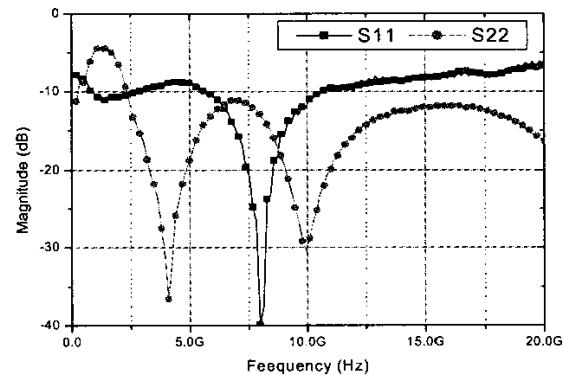

Frequency (Hz)

(a)

Fig. 8 Measured frequency response for the proposed TIA with the supply voltage 1.2V

IV. Conclusions

Table I summarizes the measured performances of the proposed TIA, compared with other literatures. This TIA can operate under the supply voltage of 1.2V and 18mW power dissipations. To authors' knowledge, it is the first 10Gb/s SiGe transimpedance amplifier (TIA) with 1.2V supply voltage. By using both the inductive series and shunting peaking techniques, the gain of 61.6dBΩ and the bandwidth of 7.4GHz can be achieved for 10GB/s applications.

Acknowledgement

V. References

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(a)

(b)

Fig. 9 Measured eye-diagrams for the proposed TIA with input equivalent current of 100uA$_{p-p}$, 1.2V supply, and input data

(a) 10Gb/s of PRBS 2^{31}-1   (Horizontal scale: 50ps/div, vertical scale: 20mV/div).

(b) 12.5Gb/s of PRBS 2^{31}-1 (Horizontal scale: 20ps/div, vertical scale: 20mV/div).

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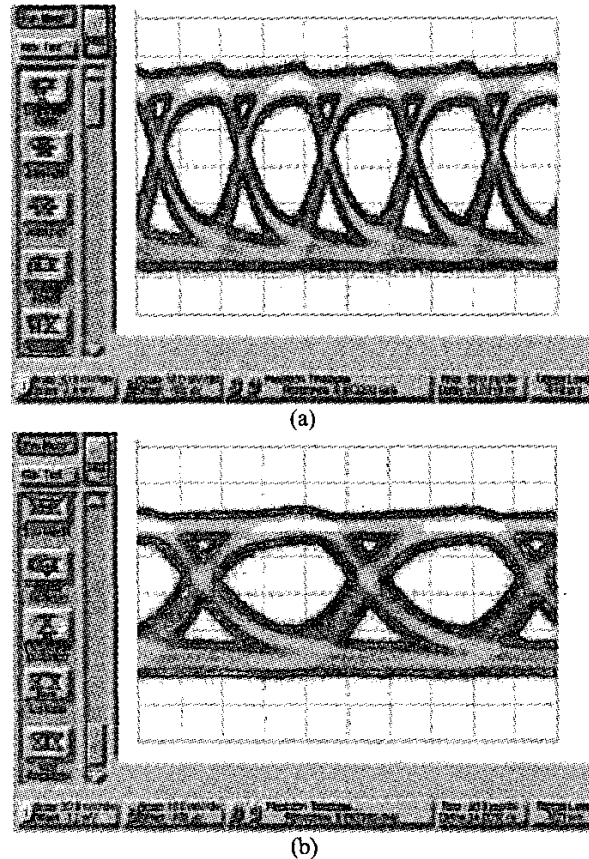
Table I. Performance summary (X: not mentioned)

Reference	ISSCC00[1]	CICC02 [2]	ISSCC02[3]	JSSC01[4]	ESSCIRC02 [5]	*This work*
Technology	0.6um CMOS	0.35um CMOS	0.25um CMOS	0.25um BiCMOS	0.18um BiCMOS	*0.35um BiCMOS*
Supply voltage	3V	3V	2.5V	5V	2.5V	*1.2V*
Speed	622Mb/s	2.5Gb/s	1Gb/s	10Gb/s	10Gb/s	*10Gb/s*
Transimpedance gain	8.7kΩ	530Ω	10kΩ	560Ω	500Ω	*1.2kΩ*
PD Capacitance	X	0.5pF	1pF	0.15pF	0.5pF	*0.15pF*
Input referred noise current density (/√Hz)	4.5pA	800nA	130nA	X	17pA	*22pA*
Power dissipation	30mW (Excluding buffer)	25mW	27mW	140mW (Buffer: 80mW)	138mW	*18mW*
Chip area	0.2mm^2	0.02mm^2	0.02mm^2	X	0.64mm^2	*0.45mm^2*