A 45.6-GHz Matrix Distributed Amplifier in 0.18-μm CMOS

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***Abstract*—This paper presents a fully integrated matrix distributed amplifier fabricated in a standard 0.18-μm CMOS process. With periodically loaded coplanar waveguides (CPW) as the synthetic transmission lines and cascode amplifiers as the gain cells, the 2×4 matrix amplifier is proposed to achieve a high gain over an extended frequency band. The fabricated circuit exhibits a gain of 6.7 dB with a 3-dB bandwidth of 45.6 GHz. Both input and output return losses are better than 10 dB within the entire frequency range. The chip size of the matrix amplifier is 1.8×1.05 mm^2 including the testing pads.**

I. INTRODUCTION

The concept of distributed amplifiers was first proposed by Percival in 1936 to alleviate the limitations imposed on the gain-bandwidth product of the conventional cascaded amplifiers. By incorporating the capacitance from the active devices into the artificial transmission lines, the distributed amplifier exhibits flat pass-band gain, good phase linearity and excellent impedance matching over a very wide frequency band. In the past few decades, distributed amplifiers fabricated in III-V compound semiconductor technologies [1]-[3] have been widely used to provide signal amplification for broad-band systems.

With recent advances in deep-submicron fabrication technology, the development of CMOS distributed amplifiers has attracted great attention due to the lower cost and higher level of integration. CMOS distributed amplifiers with a bandwidth up to tens of gigahertz [4]-[6] have been reported, providing a promising solution to the implementation of fully integrated transceivers for high-speed optical systems. However, the gain of CMOS distributed amplifiers is limited due to the nature of additive gain mechanism and the lack of high-Q on-chip passive components. In order to take the advantage of the multiplicative gain from the amplifier stages, cascaded single-stage distributed amplifiers [7] have been proposed to boost the gain at the price of reduced bandwidth. In this paper, a matrix distributed amplifier is presented in a standard 0.18-μm CMOS process. With the proposed circuit topology, the fabricated amplifier exhibits a remarkable gain enhancement while maintaining the wideband characteristics of a distributed amplifier.

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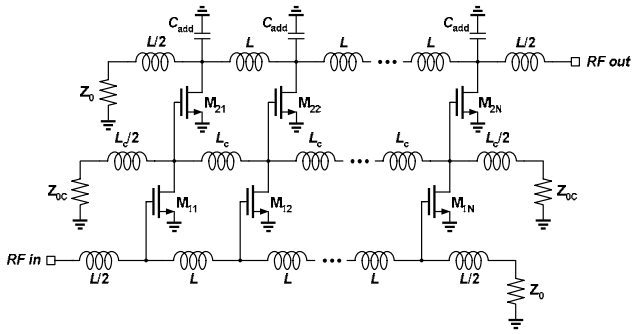

Fig. 1. The schematic of a conventional matrix distributed amplifier.

The organization of this paper is as follows. Section II describes the principle of matrix distributed amplifiers. The design of the proposed circuit is presented in Section III. The experimental results are shown in Section IV, and a conclusion is given in Section V.

II. THE PRINCIPLE OF MATRIX DISTRIBUTED AMPLIFIERS

In order to apply the additive and multiplicative gain mechanism simultaneously for optimum amplifier performance, a matrix architecture for distributed amplifiers has been employed for circuit implementations [8]-[10]. Figure 1 shows the most widely used circuit topology for a two-tier matrix amplifier which is composed of three periodically loaded synthetic transmission lines: input line, central line, and output line. According to the distributed amplifier theory, the three transmission lines are imposed to have the same cut-off frequency and consequently the same phase velocity.

Typically, the cut-off frequency f_c and the characteristic impedance Z_0 of the input and the output line can be expressed as [11]

$$f_c = \frac{\omega_c}{2\pi} = \frac{1}{\pi\sqrt{LC_{gs1}}} = \frac{1}{\pi\sqrt{L(C_{ds2}+C_{add})}} \quad (1)$$

$$Z_0 = \sqrt{\frac{L}{C_{gs1}}} = \sqrt{\frac{L}{(C_{ds2}+C_{add})}} = 50\Omega \quad (2)$$

where C_{gs1} is the input capacitance of the gain cells in the first tier, C_{ds2} is the output capacitance of the gain cells in the

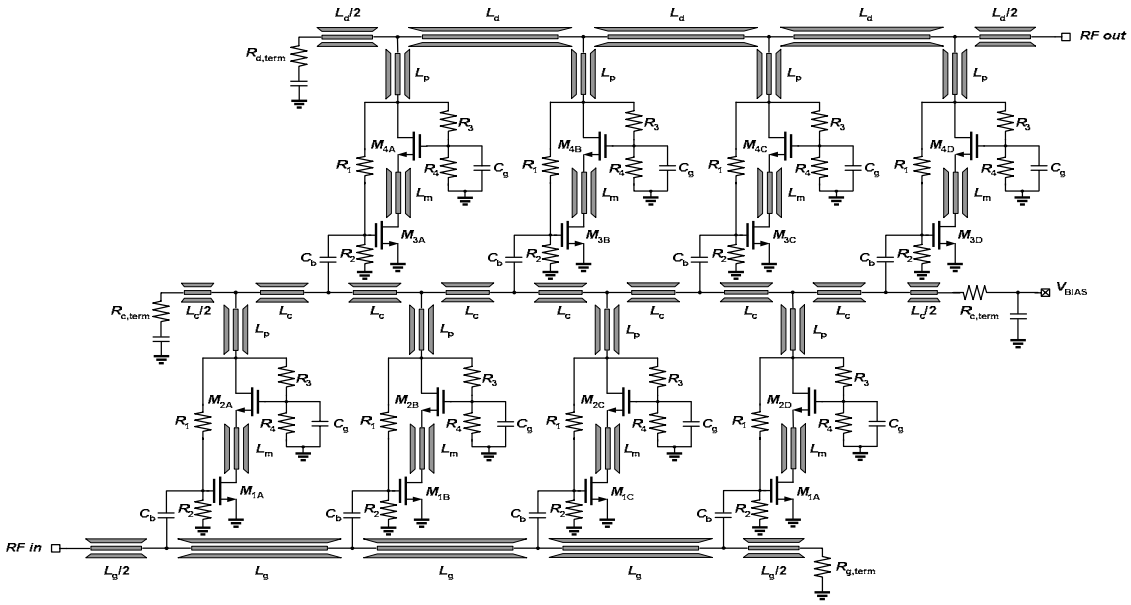

Fig. 2. The complete schematic of the 2×4 matrix distributed amplifier implemented in a CMOS technology.

second tier, and C_{add} represents the additional capacitive loading for the output line. Since the central line is loaded with the output capacitance of the first tier (C_{ds1}) and the input capacitance of the second tier (C_{gs2}), the inductance L_c required to achieve the same cut-off frequency f_c as specified in (1) is given by

$$L_c = \frac{1}{\pi^2 f_c^2 (C_{gs2} + C_{ds1})} = \frac{C_{gs1}}{C_{gs2} + C_{ds1}} L \cdot \tag{3}$$

Therefore, the resulting characteristic impedance of the central line is

$$Z_{0c} = \sqrt{\frac{L_c}{C_{gs2} + C_{ds1}}} = \frac{C_{gs1}}{C_{gs2} + C_{ds1}} Z_0 \cdot \tag{4}$$

In addition to the synthetic line equations as depicted in (1)-(4), the line attenuation has strong influence on the overall performance of the matrix amplifier. By employing the loss analysis developed for distributed amplifiers [12], the circuit parameters and the optimum stage number can be obtained in a practical circuit implementation.

III. Proposed Topology and Circuit Design

To further alleviate the gain-bandwidth limitations imposed on the conventional matrix amplifier, a novel circuit topology is presented. Implemented in a standard 0.18-μm CMOS process, the proposed circuit is designed to demonstrate a high gain with a bandwidth over 40 GHz. The complete schematic of the fully integrated matrix amplifier including all on-chip components is shown in Fig. 2 where a total of eight gain cells are arranged in the form of a 2×4 matrix. Each tier of the matrix is composed of four identical cells in a distributed amplifier architecture while all the synthetic lines are terminated with the characteristic impedances by on-chip resistive loads. In this design, high-impedance CPW sections are used to connect the gain cells for the synthesis of the artificial transmission lines. To minimize the line attenuation associated with the conductor losses and the possible penetration of EM fields through the lossy silicon substrate, the CPW structures are realized by the top metal layer in the CMOS process. Based on the full-wave EM simulation, the CPW employed in this design exhibits an unloaded characteristic impedance of 108 Ω within the cut-off frequency.

In stead of using common-source transistors, cascode stages are employed as the gain cells in the matrix amplifier due to the superior characteristics in gain, bandwidth, stability and input-to-output isolation. The inherently high output resistance provided by the cascode stages effectively reduces the attenuation of the synthetic transmission lines, yielding an enhanced performance of the matrix distributed amplifier. To simplify the bias scheme of the cascode stages, voltage dividers (R_1-R_2, R_3-R_4) are used to specify the gate voltages of the transistors. The drain currents of the first and the second tier are provided by the central and the output synthetic line, respectively. The capacitance C_b is added at the input of the gain cells for dc blocking, while the capacitance C_g are used as the by-pass capacitance for the common-gate transistors. In order to achieve the highest possible gain at the high frequency band, CPW sections L_m and L_p are adopted in this design for inter-stage matching and gain peaking, respectively.

In a conventional matrix amplifier, the central line is loaded with the output node of the first tier and the input node of the second tier at the same point. The excess capacitance and the finite resistance associated with the loading nodes impose stringent limitations on the frequency-dependent attenuation

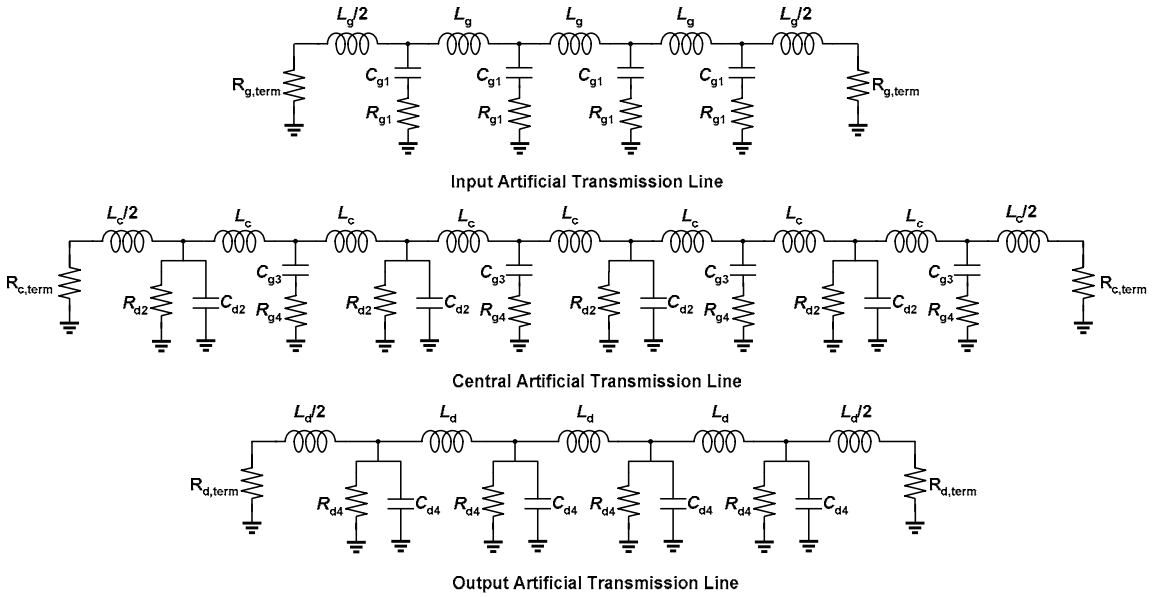

Fig. 3. The simplified small-signal presentation for the artificial transmission lines in the 2×4 matrix distributed amplifier.

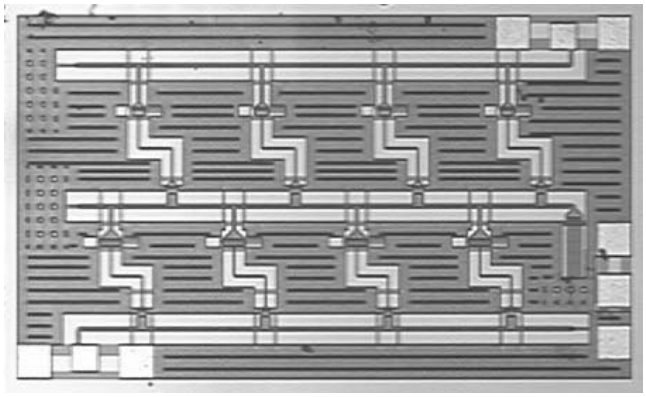

Fig. 4. The die photograph of the fabricated matrix amplifier.

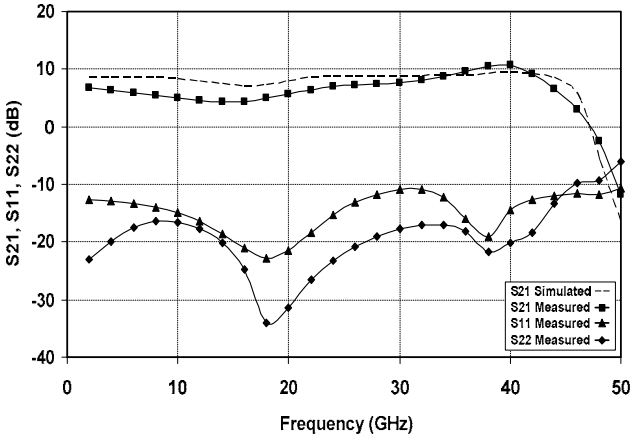

Fig. 5. The measured S-parameters of the matrix amplifier.

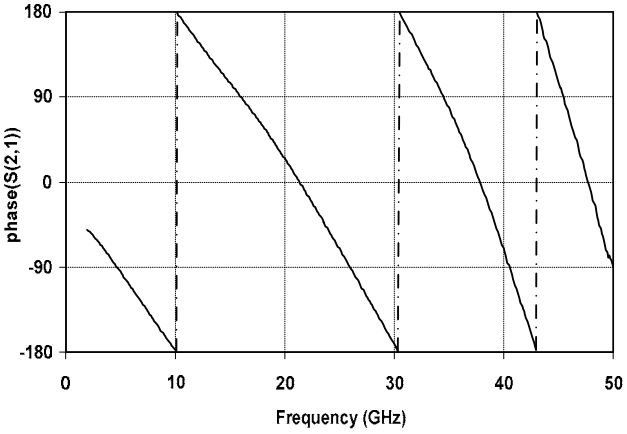

Fig. 6. The measured phase response of the matrix amplifier.

and cut-off frequency of the central line. In order to overcome the design limitations, the output loading of the first tier and the input loading of the second tier are separated by an equivalent inductance L_c in the proposed circuit topology. With the distributed loading technique, a significant performance improvement in terms of the gain and bandwidth of the matrix amplifier can be achieved. A simplified small-signal presentation of the synthetic lines is illustrated in Fig. 3. Due to the use of cascode stages, the sizes of the common-source and the common-gate transistors can be chosen independently to achieve the required input and output capacitance. Therefore, identical cut-off frequency of the artificial transmission lines can be achieved by setting $C_{d2}=C_{g3}=2C_{g1}=2C_{d4}$ and $L_c=L_g/2=L_d/2$.

IV. Experimental Results

By employing the proposed circuit topology, the 2×4 matrix

TABLE I
PERFORMANCE SUMMARY OF THE MATRIX DISTRIBUTED AMPLIFIER

Technology	0.18-μm CMOS
Gain	6.7 dB
Bandwidth	45.6 GHz
Gain-bandwidth product	213 GHz
Return loss	>10 dB
Power consumption	497 mW
Chip size (including pads)	1.8×1.05 mm^2

distributed amplifier is designed and implemented in a standard 0.18-μm CMOS process. Figure 4 shows the die photograph of the fabricated circuit with a chip size of 1.8×1.05 mm^2 including the testing pads. On-wafer probing was performed to characterize the S-parameters of the matrix amplifier.

Since the characteristic impedance of the output line is higher than that of the central lines, higher bias currents are intentionally provided to the gain cells in the first tier for a balanced gain contribution from the tiers. The bias voltages for the first and the second tier of the cascode stages are 3.8 and 3.3 V, respectively, resulting in a total power consumption of 497 mW for the amplifier core. The measured S-parameters from 2 to 50 GHz are shown in Fig. 5, exhibiting a low-frequency gain of 6.7 dB with a 3-dB bandwidth of 45.6 GHz. Due to the use of the peaking inductance L_p in the cascode stages, a 3.7-dB gain peaking is observed in the vicinity of 40 GHz. The gain flatness can be improved by decreasing the value of the peaking inductance L_p and increasing the value of the by-pass capacitance C_g. With on-chip terminations for the synthetic lines, input and output return losses better than 10 dB have been achieved up to 46 GHz. The phase response of the matrix amplifier is illustrated in Fig. 5, indicating a linear phase variation within the entire frequency band. The performance of the fabricated matrix distributed amplifier is summarized in Table I.

V. CONCLUSION

A novel circuit topology for monolithic matrix amplifiers is presented in this paper. Using a standard 0.18-μm CMOS process, a 2×4 matrix distributed amplifier is designed and implemented for demonstration. The fabricated circuit exhibits a gain of 6.7 dB and a 3-dB bandwidth of 45.6 GHz while maintaining excellent input and output impedance matching over the entire frequency band. A gain-bandwidth product of 213 GHz has been achieved in this design. To the authors' best knowledge, this is the first successful implementation of matrix distributed amplifier in a bulk CMOS technology.

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