A 2V CMOS Programmable Pipelined Digital Differential Matched Filter for DS-CDMA System

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Abstract

This paper presents a 2V DS-CDMA programmable digital matched filter with a differential and pipelined structure. Differential PN (Pseudo-Noise) code scheme is adopted to reduce the number of multiplication and summations (M&S). The PDDMF (Pipelined Digital Differential Matched Filter) not only saves the hardware and the power, but also improves the operation speed, which makes PDDMF more suitable, for personal communication at high speed and low power requirements than the conventional approach. The PDDMF implemented in a 0.6μm CMOS technology is clocked at 2.5 MHz and consumes 1.6mW from a single power supply 2V.

Introduction

Direct Sequence Code Division Multiple Access (DS-CDMA) has been successfully applied to many low bandwidth wireless communication systems. In these systems, matched filter is usually employed for code acquisition since it offers significant advantages in the speed of synchronization. However, the primary limitation of the conventional digital filters is the number of stages that is greatly associated with the hardware implementation of multiplication and accumulation. This paper describes a CMOS low-voltage low-power programmable pipelined digital matched filter that employs a differential PN code scheme [1] in order to reduce hardware complexity and hence the chip size and power.

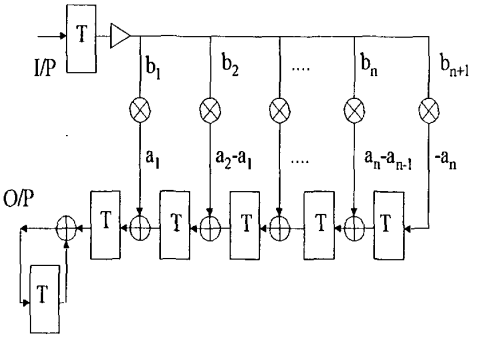
Pipelined Digital Differential Matched Filter

The total number of multiplication and summation in conventional matched filter M_c is 2^r-1, where r is the order of the PN code polynomial generator. Obviously as the number of stages increases, the number of M&S significantly increases. A differential PN code scheme (Fig.1) [1] is employed to avoid this problem. The output function of the matched filter can be described as :

$$f_D(T)=[b_{N+1}x_0+b_Nx_1+b_{N-1}x_2...+b_2x_{T-1}+b_1x_T]+f_D(T-1)$$
$$=[-a_Nx_0+(a_N-a_{N-1})x_1+(a_{N-1}-a_{N-2})+.....+(a_2-a_1)x_{T-1}$$
$$+a_1x_T]+f_D(T-1)$$

where b_i for i from 0 to N+1 is the multiplication coefficients of the PDDMF, and a_i is the PN code coefficient of the conventional matched filter. Since the coefficients a_i of the PN code can be either –1 or +1, b_i must therefor be 0, -2, or +2. There is no need to do M&S on coefficients "0", the number of M&S is therefore significantly reduced with long PN code stage. The total number of M&S M_d in such a pipelined differential digital matched filter is $2^{(r-1)}$.

Fig1: The pipelined digital differential matched filter



The pipelined structure, simplifies the summation circuit of the multiple input, and improves the speed of the PDDMF. Furthermore, the throughput of the PDDMF is independent of the PN code length.

Circuit Architecture

Fig.2 is a block diagram of the PDMMF for DS-CDMA receiver. The 9.6kHz input data are spread into a signal band 1.2288MHz in IS-95 based CDMA systems. Because the SNR of the spreading signal is very low, the 4bits soft

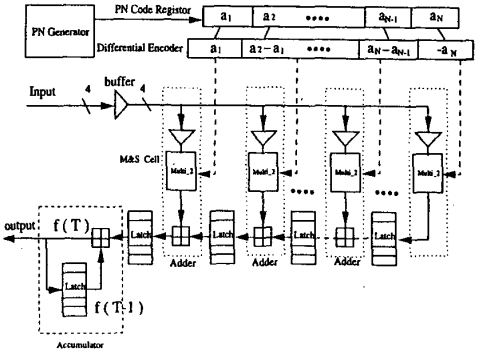


Fig.2 The programmable PN coefficients of PDDMF

decision matched filter is adopted to increase the reliability of data detection. The multiplication coefficients of PDDMF are user programmable by the PN code generator. The PN code generated by the PN generator is first stored in the PN code register. Then the differential encoder generates the multiplication coefficients according to the differential PN code scheme. It controls the M&S cell for coefficients setting. The new coefficient will be 0 when adjacent coefficients are the same value.

Fig.3 shows the circuit of two's complementary M&S with coefficient 2 and –2. The input data d1, d2, d3, d4 multiply the coefficient first. If the multiplication coefficient b_i is -2 the pins neg and cin are set to logic 1; otherwise they will be set to logic 0 for bi=2.

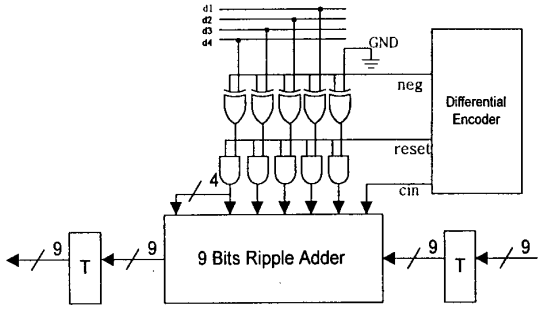


Fig.3 Circuit design for M&S cell circuit of 2 and –2

A 9 bits ripple adder performs the summation in the final. Ripple adder is chosen for low power rather than for high speed. The chip-rate of the PN code used is 1.2288MHz, the tap length is 16 and the number of multiplication coefficients for $b_i = a_i - a_{i-1} = 0$ is 7. Only 8 coefficients need to be multiplied, rather than 32 coefficients in the conventional 16 taps length matched filter with 2 over-sampling per chip-time. The number of M&S is reduced to 1/4. Fig.4 is the die photo of the programmable 16 taps length PDDMF. It is fabricated in a 0.6μm CMOS technology. The chip area is 1500μm by 1500μm.

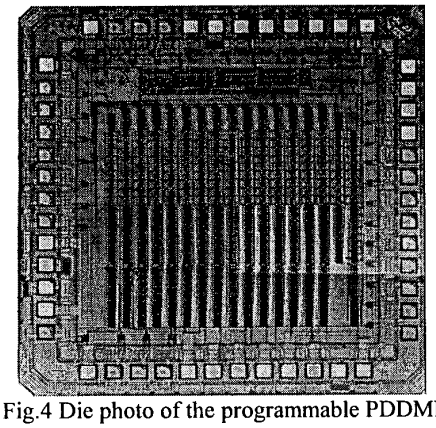


Fig.4 Die photo of the programmable PDDMF

Experimental Results

Fig.5 shows the testing results of the PDDMF by IMS logic master, The testing mode can be programmed either automatic self-test mode or normal mode. In self-test mode, the input PN code and coefficients are generated automatically. Under normal test mode whose input code is fed externally, while filter coefficients are chosen by user. In both modes, the auto-correlation results can track the PN sequence correctly.

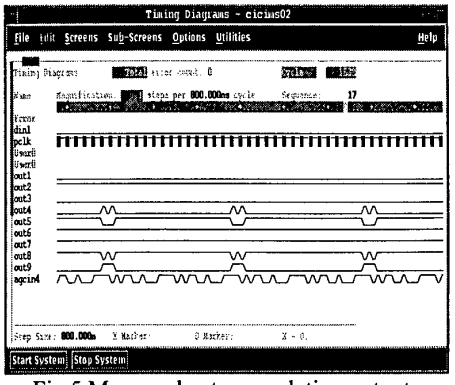


Fig.5 Measured auto-correlation output

The chip clocks at a rate from 1.25MHz to 5MHz under 2V-power supply. It only consumes 1.6mW including pads for clock rate 2.5MHz. Table 1 shows the summary of the testing results

PDDMF Performance Summary	
Power Supply	2V
Technology	0.6 μm CMOS
Tap Length	16
Samples/Chip	2
PN Code Rate	1.25MHz
Clock Rate	2.5MHZ
Power Consumption	1.6mw
Chip Area	1500um *1500um

Table 1. Measure performance summary

Acknowledgment

The authers wish to thank Mr. Kuang-Chan Liu for fruitful discussions through the works.

Conclusion

A programmable PDDMF implemented in 0.6μm CMOS technology has been provided. With the differential PN code scheme and pipelined structure, it not only saves the hardware and power by almost a half but also improves the speed of the programmable PDDMF.

Reference

[1] Kuang-Chan Liu, Wun-Chang Lin and Chorng-Kuang Wang, " A Pipelined Digital Differential Matched Filter FPGA Implementation & VLSI Design", *IEEE 1996 Custom Integrated Circuits Conference*