

An Automatic Synthesizer for CMOS Operational Amplifiers

Chin-Yuan Kuo Liang-Gee Chen Tai-Ming Pamg

Department of Electrical Engineering
National Taiwan University, Taipei, Taiwan, R.O.C.

Abstract

A design methodology with a good trade-off between design time and quality in the automatic synthesis of CMOS operational amplifiers is presented. It is based on an iterative device sizing approach in which a multivariate interpolation technique provides a way to improve the design and the SPICE simulator gives quantitative evaluation of the resultant circuit performance in each design iteration. The methodology has been implemented and proved to be very practical and promising.

1. Introduction

Generally speaking, the design of an analog circuit like an operational amplifier (op-amp) is more complicated than a digital one because there are many factors the designer must be concerned with and these factors are not only in the time domain but also in the frequency domain. Furthermore, these factors are interrelated rather than independent.

A few researches about automatic synthesis of op-amps have been published [1,2,3,4]. The two recent ones that are closely related to ours are surveyed. Koh et al. [3] proposed an algorithmic method. They use a predefined cost function and a multi-start steepest-gradient descent algorithm to seek the candidate solutions. Its resultant design may be far from the optimal one because the SPICE simulations are not used in selecting the candidate solutions. Sheu et al. [4] proposed a knowledge-based system for automatic op-amp design. First of all, the expert system guesses the device sizes. Secondly, the expert system proposes an improved design based on the difference between the specifications and the SPICE-simulated results of the previous design until the design meets the specifications. If equipped with sufficient design knowledge, this approach can achieve very accurate results. However, because there are many degrees of freedom involved and the total search space becomes very complicated and huge, this approach is usually very time-consuming.

To have a better trade-off between design time and quality, we propose an alternative approach. Like the knowledge-based system discussed above, ours is also an iterative approach using SPICE simulations. However, instead of using an expert system, we use an algorithm-based device sizing approach. For each design iteration, a multivariate

interpolation functions are developed, based on all the design data and the simulation results obtained in the previous iterations, and used to obtain a better design, i.e., a design which is closer to the desired specifications. Consequently, while SPICE simulation runs guarantee the accuracy of our approach, the algorithmic interpolation technique facilitates efficiently locating the solution through a large possible design space.

The next section gives a brief overview of the proposed methodology. Section three presents the performance parameters of an op-amp. Section four describes how to evaluate the device sizes. In section five, we introduce multivariate interpolating functions and discuss how to apply the interpolating technique to improve our design. Also, the detail algorithm of the iterative device sizing procedure is presented. Section six outlines synthesis results and comparisons. Finally, conclusions are given in the last section.

2. The Proposed Approach to Automatic Design of Op-Amps

The design flows of automatic op-amp design based on the proposed approach is shown in Fig. 1. This approach is capable of doing synthesis for various topological architectures of op-amps. Currently, only one architecture as shown in Fig. 2 was implemented. In fact, this proposed methodology can also be applied to circuits other than op-amps.

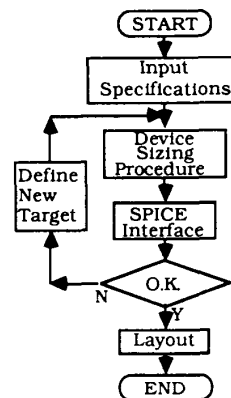


Fig. 1 Block Diagram of Our System

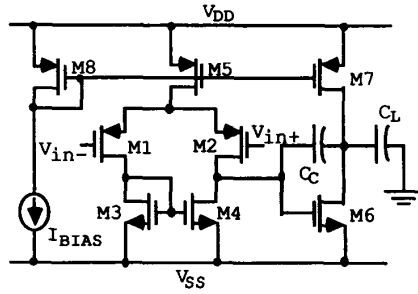


Fig. 2 Operational Amplifier

The whole design process is as follows. First of all, the specifications, i.e. a set of characteristic parameters of the op-amp, must be given. Initially, the specifications are assigned to be the target performance. Based on the target performance, the device sizing procedure obtains a design by computing the set of device sizes using a set of device size models. The performances of the design is then obtained by means of SPICE simulations. If the design of current iteration cannot meet the specifications, all the designs and previous simulation results are fed into a multivariate interpolation procedure to compute a new target for the next iteration. The whole cycle repeats until the performances of the design meet the specifications. Finally, the layout procedure can be invoked to generate the mask layout of the successful design. Currently, we use the level 1 model for MOS device in SPICE simulation, and other level models for MOS device are also applicable if available.

Since there are many characteristic parameters involved, we must reduce the design space to apply an algorithmic approach. In other words, the device sizing procedure inevitably uses heuristic knowledge to restrict some parameters, which will be detailed in section 4. On the other hand, how to define the target for the device sizing procedure also plays an essential role in our system. Before giving details on these topics, we describe the specification parameters that concern our approach in the next section.

3. Specification Parameters of an Op-Amp

For an op-amp, there are seven characteristic parameters that we are concerned with. They are:

- i) unity-gain bandwidth, denoted by ω_0 , which is approximated by the product of the location of lowest frequency pole and the gain at that frequency,
- ii) slew rate, denoted by SR ,
- iii) phase margin, denoted by ϕ ,
- iv) open-loop gain, denoted by A_{o0} ,
- v) output voltage range, denoted by VOR ,
- vi) input common-mode range, denoted by CMR ,
- vii) power dissipation, denoted by P_{diss} .

The power supply rejection ratio (PSRR) of op-amps mainly depends on the architecture, and therefore is not a major concern of the device sizing procedure. In addition, some other characteristic parameters, e.g. the CMRR (common-mode rejection ratio), settling time, noise and area, are also not considered in current implementation.

4. Device Sizing

By means of circuit analysis technique, the formulae of the characteristic parameters can be derived as illustrated in [5]. We are able to manipulate those formulae to express all the device sizes in terms of the characteristic parameters we are concerned with. The following equations, which form the device size models of our approach, are the derived formulae for all device sizes:

$$S = \frac{\text{channel width}}{\text{channel length}} = \frac{W}{L}$$

$$C_C = \frac{1 + m \tan(\phi)}{m(m - \tan(\phi))} C_L \quad (1)$$

$$S_1 = S_2 = \frac{C_C \cdot \omega_0^2}{K_p' \cdot SR} \quad (2)$$

$$S_3 = S_4 = \frac{SR \cdot C_C}{K_n' \cdot V_{sat}^2} \quad (3)$$

$$S_5 = S_8 = \frac{2SR \cdot C_C}{K_p' \cdot V_{sat}^2 \cdot (1 + \lambda_p \cdot V_{SD5})} \quad (4)$$

$$S_6 = \frac{m \cdot \omega_0 \cdot C_C}{K_n' \cdot V_{sat} \cdot (1 + \lambda_n \cdot V_{DD})} \quad (5)$$

$$S_7 = \frac{m \cdot \omega_0 \cdot C_C}{K_p' \cdot V_{sat} \cdot (1 + \lambda_p \cdot V_{DD})} \quad (6)$$

where the m and V_{sat} are defined as follows:

- 1° The transfer function of the op-amp is a second-order one, which has two poles and a right-half plane (RHP) zero [5,6,7,8,9]. The RHP zero will severely deteriorate the frequency response if its frequency is not high enough. Therefore, we assume that the frequency of the zero is m times higher than ω_0 ; the rule-of-thumb value of m is ten.
- 2° To simplify the analysis task, we assume that the magnitudes of positive and negative output voltage swing are equal. That is, the saturation voltage of M6 and M7 are equal. We use V_{sat} to denote the saturation voltage of M6, then the following equations hold.

$$V_{sat} = V_{DS3sat} = V_{DS4sat} = V_{DS6sat} = V_{SD7sat} = V_{SD5sat}$$

The definitions of m and V_{sat} presented above are the very heuristic knowledge utilized to simplify the analysis task and reduce the design space.

From the economical point of view, the aspect ratio of each transistor can neither be too large nor too small because both these two extreme cases cause larger transistor area. Therefore, the aspect ratio of each transistor should have its own upper and lower bounds, that is,

$$SiMIN \leq S_i \leq SiMAX, i = 1, \dots, 7 \quad (7)$$

where $SiMIN$ and $SiMAX$ represent the lower and upper bounds of transistor M_i , respectively.

By inspection of Eqs.(1)-(6), we find that all the device sizes can be determined if V_{sat} and the three characteristic parameters, ω_0 , SR and ϕ , are specified. By combining Eq.(3) and Eq.(7), the range of V_{sat} can be derived as shown in the following:

```

1° Procedure Transistor_Sizing (target, CC, S2, S3, S5, S6, S7)
2°   Var Av0, Pdist, CMR, VOR, Vsat, SR, ω0, φ, m
3° Begin
4°   SR = target of SR
5°   ω0 = target of ω0
6°   φ = target of φ
7°   m = 10
8°   Using Eq.(1) to evaluate CC
9°   Using Eq.(2) to evaluate S2
10°  If Not (S2MIN ≤ S2 ≤ S2MAX) Then
11°    Return Fail
12°  For Vsat=(VDS3sat)max To (VDS3sat)min Step -1 mV
13°    Using Eqs.(3)-(6) to evaluate S3, S5, S6, S7
14°    Calculate Av0, Pdist, CMR, VOR
15°    If (every parameter satisfies its constraint) Then
16°      Return Success
17°    Next Vsat
18°  Return Fail
19° End Procedure

```

Fig. 3 Transistor Sizing Algorithm

$$(V_{DS3sat})_{min} \leq V_{sat} \leq (V_{DS3sat})_{max}$$

where $(V_{DS3sat})_{max} = \left[\frac{I_{DS}}{K_n \cdot S3MIN} \right]^{1/2}$, $(V_{DS3sat})_{min} = \left[\frac{I_{DS}}{K_n \cdot S3MAX} \right]^{1/2}$.

The device sizing algorithm is shown in Fig. 3. If we assign ω_0 , SR and ϕ to be its own target value and V_{sat} to be $(V_{DS3sat})_{max}$ initially, we can obtain the device sizes from Eqs.(1)-(6) and the prediction values of all characteristic parameters from the formulae derived by means of circuit analysis technique. We must check whether these device sizes and characteristic parameters satisfy their own constraints expressed in Eq.(7) and specifications, respectively. If there is any violation, V_{sat} is decremented by one mV and the whole procedure is repeated.

5. Applying Multivariate Interpolation Functions

We attribute the improvement of a design during each design iteration in our approach to the exploitation capability of the multivariate interpolation technique we developed. In the following subsections, first we describe the formulation of the interpolation technique. Then the derivation of multivariate interpolation functions are detailed and the detail algorithm of the whole iterative device sizing approach based on the multivariate interpolation technique is given.

5.1. Formulation of the Interpolation Technique

For convenience of mathematical description, we define the so-called first, second, and third characteristic parameters to be unity-gain bandwidth (ω_0), slew rate (SR), and phase margin (ϕ), respectively, which are the three independent parameters in our method. We use $performance[i, j]$ and $target[i, j]$ to denote the j -th ($j=1,2,3$) performance and target characteristic parameter of the i -th iteration, respectively, and use $spec[j]$ ($j=1,2,3$) for the three specification parameters.

We know that one set of targets for device sizing procedure corresponds to a set of performance values obtained via SPICE circuit simulation. Assume that we have experienced M iterations. For the i -th iteration, these two sets of data are normalized with respect to the specifications and denoted by D_{ij} and K_{ij} , $j=1,2,3$, respectively. The D_{ij} and K_{ij} can be expressed as follows:

$$D_{ij} = \frac{target[i, j]}{spec[j]}, \text{ for the } i\text{-th iteration} \quad (8)$$

$$K_{ij} = \frac{performance[i, j]}{spec[j]}, \text{ for the } i\text{-th iteration} \quad (9)$$

We assume that the relation between D_{ij} and K_{ij} can be formulated by functions, that is,

$$D_{ij} = C_j(K_{i1}, K_{i2}, K_{i3}), \quad i=1, \dots, M \quad (10)$$

Since we anticipate that $performance[M+1, j]$ is equal to $spec[j]$, i.e., all $K_{(M+1)j}$ are equal to one, if the functions $C_j()$ are known, we can compute the new target for the device sizing procedure in the next iteration by using the following equation.

$$target[M+1, j] = D_{(M+1)j} \cdot spec[j] = C_j(1, 1, 1) \cdot spec[j] \quad (11)$$

Based on the new target, the device sizing procedure finds a new set of device sizes and restart the design iteration.

Because the explicit forms of the functions $C_j(t_1, t_2, t_3)$ are unknown, it should be derived in some ways. We approximate them via multivariate interpolating functions which are detailed in the next subsection.

5.2. Our Interpolation Function

The interpolation function of an unknown one is a linear combination of some basis functions, which are known. Therefore, the form of our interpolation function is determined if the basis functions are defined. The type of the basis functions we adopt is a monomial, which is recommended by Kunz[10] and Thacher[11]. We define $T(n, t_1, \dots, t_p)$ to be the n -th basis function of p variables. The definition of $T(n, t_1, \dots, t_p)$ that we adopt is shown in Fig. 4.

With the basis functions defined, the functions $C_j(t_1, t_2, t_3)$ in Eq.(10) can then be replaced by their own interpolation functions $F_{Mj}()$ which denotes the multivariate interpolation function for $C_j()$ and $F_{Mj}(t_1, t_2, t_3) = \sum_{n=1}^M A_{nj} \cdot T(n, t_1, t_2, t_3)$. If M previous results are available and thereby the following equations can be obtained:

```

1° Function Partial_Sum(Count, X1, ..., Xp)
2°   Var Sum, G, N1, ..., Np
3° Begin
4°   Sum = 0
5°   For G = 0 To ∞
6°     For Np = 0 To G
7°       For Np-1 = 0 To G - Np
8°         For Np-2 = 0 To G - Np - Np-1
9°           ...
10°          For N2 = 0 To G - Np - Np-1 - ... - N3
11°            If (Count > 0) Then
12°              N1 = G - Np - ... - N2
13°              Sum = Sum + XpNp Xp-1Np-1 ... X2N2 X1N1
14°              Count = Count - 1
15°            Else
16°              Return Sum
17° End

```

$$T(n, t_1, \dots, t_p) = \text{Partial_Sum}(n, t_1, \dots, t_p) - \text{Partial_Sum}(n-1, t_1, \dots, t_p)$$

Fig. 4 Definition of $T(n, t_1, \dots, t_p)$

$$F_{M_j}(K_{i1}, K_{i2}, K_{i3}) = \sum_{n=1}^M A_{nj} \cdot T(n, K_{i1}, K_{i2}, K_{i3}) = D_{ij}, 1 \leq j \leq 3, 1 \leq i \leq M \quad (12)$$

or, expressed in matrix form,

$$\bar{T} \bar{A}_j = \bar{D}_j, j=1,2,3 \quad (13)$$

where \bar{A}_j and \bar{D}_j are column vectors with $(\bar{A}_j)_i = A_{ij}$ and $(\bar{D}_j)_i = D_{ij}$, and \bar{T} is a matrix with $(\bar{T})_{ij} = T(j, K_{i1}, K_{i2}, K_{i3})$.

The explicit forms of $F_{M_j}()$ can be obtained if A_j can be solved uniquely from Eq.(13). Then the next task is to use them to evaluate the new targets for the three independent characteristic parameters with the expectation that the performances of the synthesized circuit will be equal to the specifications. In other words, we anticipate that $performance[M+1, j]$ is equal to $spec[j]$, $j=1,2,3$, or, equivalently, the normalized performance of each characteristic parameter, $K_{(M+1)j}$, is set to one. It can be expressed mathematically,

$$D_{(M+1)j} = C_j(1, 1, 1) = F_{M_j}(1, 1, 1) = \sum_{n=1}^M A_{nj} \cdot T(n, 1, 1, 1), j=1,2,3 \quad (14)$$

for the j -th normalized target of the corresponding characteristic parameter. Combining Eq.(8) and Eq.(14), we can obtain the new denormalized targets which will be fed into the device sizing procedure in the next iteration.

Based on the discussions presented above, the detail algorithm of the iterative device sizing approach based on the multivariate interpolation technique is summarized in Fig. 5.

In using the multivariate interpolating technique, several special cases must be considered beforehand in order to reduce the execution efforts or prevent program from failure. These cases are described as follows:

1) The Interpolation Function Does Not Exist

The interpolation function of single variable functions always exists, while the existence of interpolation function of functions with several variables cannot be guaranteed [11]. In this case, we cannot solve A_{ij} from Eq.(12). To continue the design process, we decrease M by one and discard arbitrarily one function value among the M points known to us and start another iteration.

2) The Target Is the Same as That for Some Previous Iteration

It is not necessary for us to repeat the work that has been done before. Hence, we discard the current target and replace it with a set of random numbers.

3) Unreasonable Target

If a target of some characteristic parameter is negative, it is unreasonable obviously. In this case, we use a set of random numbers to replace the unreasonable target.

It is worth noting that, in the second iteration, our interpolation functions will be 1, i.e., $F_{ij}() = 1$. In other words, the target obtained in the second iteration is the same as that for the first iteration. Therefore, we encounter the second special case described above and must resort to using a set of random numbers as a new target. This randomly generated target may affect the convergent rate to some extent.

6. Experimental Results

Based on the proposed approach, an automatic synthesis

```

1° COMMENT : For the convenience of mathematical
description, we define the so-called first, second, and third
characteristic parameters to be unity-gain bandwidth ( $\omega_0$ ),
slew rate ( $SR$ ), and phase margin ( $\phi$ ), respectively, which
are the three independent parameters in our method. We
use  $performance[i, j]$  and  $target[i, j]$  to denote the  $j$ -th
( $j=1,2,3$ ) performance and target characteristic parameter of
the  $i$ -th iteration, respectively, and use  $spec[j]$  ( $j=1,2,3$ )
for the three specification parameters.

2° Success = False, M = 1, target[M, j] = spec[j] ; COM-
MENT : Initialization

3° REPEAT {

4°   Input target[M, j] into DEVICE SIZING PRO-
CEDURE and do SPICE simulation

5°   Compute performance[M, j]

6°   IF performance[M, j] satisfies spec[j] THEN

7°     Success = True

8°   ELSE

9°     Using Eq.(9) to compute  $K_{Mj}$ 

10°    Apply  $K_{ij}$ ,  $1 \leq i \leq M$ ,  $1 \leq j \leq 3$  to Eq.(12)

11°    Evaluate the multivariate interpolation func-
tions  $F_{Mj}()$  by solving Eq.(12)

12°    Use Eq.(14) to compute target[M+1, j]

13°    M = M+1

} UNTIL Success = True

```

Fig. 5. Algorithm of Iterative Device Sizing Using Multivariate Interpolation Technique

program for op-amps has been implemented in C programming language on the SUN3/110 workstation. There are about 1800 lines in the program.

Experimental results are illustrated in Table 1 and Table 2 for different specifications. As demonstrated in Table 1, the design of the tenth iteration can meet its specifications. If we permit 2% deviation between design performance and specifications, the program can be halted at the sixth iteration. If the deviation we can tolerate is 12%, the desired design can be achieved at the second iteration.

The experimental results show that the proposed methodology is very promising. To accomplish Table 1, our system spends 49 seconds CPU time and the SPICE simulation spends about 1700 seconds CPU time. While the accuracy of our results is guaranteed by SPICE simulations, the run-time performance of our approach is still comparable to that of Koh [3], which took 70 to 280 CPU seconds for synthesis and 200 CPU seconds for SPICE simulation on VAX 8800, a 6 MIPS machine.

7. Conclusions

A new methodology for automatic synthesis of op-amps has been presented. By using an iterative device sizing approach based on a multivariate interpolating technique, our approach can be very efficient at locating a qualified design solution. Also, SPICE simulations are used to provide quantitative evaluations of the resultant circuit performance. Consequently, a better trade-off between design time and quality can be achieved. A program based on the proposed approach

has been implemented and proved to be very practical and promising. Finally, it is worth noting that, although only one topology of op-amp has been used, the interpolating technique may also be applied to other topologies of op-amps and even other analog and digital design fields which have many interrelated parameters.

References

- [1] R. Harjani, R. A. Rutenbar, and L. R. Carley, "A Prototype Framework for Knowledge-Based Analog Circuit Synthesis," *Proc. of 24th ACM/IEEE Design Automation Conferences*, pp.42-49, 1987
- [2] E. Berkcan, M. d'Abreu, and W. Laughton, "Analog Compilation Based on Successive Decompositions," *Proc. of 25th ACM/IEEE Design Automation Conferences*, pp.369-375, 1988
- [3] Han Young Koh, Carlo H. Séquin, and Paul R. Gray, "OPASYN : A Compiler for CMOS Operational Amplifiers," *IEEE Transactions on Computer-Aided Design*, vol.9, no.2, pp. 113-125, Feb. 1990
- [4] Bing J. Sheu, Antony H. Fung and Ying-Nan Lai, "A Knowledge-Based Approach to Analog IC Design," *IEEE Transactions on Circuits and Systems*, vol.35, pp. 256-258, Feb. 1988
- [5] Phillip E. Allen, Douglas R. Holberg, *CMOS Analog Circuit Design*, Holt, Rinehart and Winston, New York NY, 1987
- [6] Paul R. Gray and Robert G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 2nd ed. John Wiley & Sons 1984
- [7] Alan B. Grebene, "The Operational Amplifier in Custom LSI Design -- A Tutorial Study," *IEEE 1984 CUSTOM INTEGRATED CIRCUITS CONFERENCE*, pp. 540-545
- [8] Paul R. Gray and Robert G. Meyer, "MOS Operational Amplifier Design -- A Tutorial Overview," *IEEE Journal of Solid-State Circuits*, vol. SC-17, pp. 969-982, Dec. 1982
- [9] R. Gregorian and G. C. Temes, *Analog MOS Integrated Circuits for Signal Processing*, New York Wiley and Sons, 1986
- [10] Kaiser S. Kunz, *Numerical Analysis*, McGraw-Hill 1957, pp. 249-253
- [11] Henry C. Thacher, Jr., and W. E. Milne, "Interpolation in Several Variables," *Society for Industrial and Applied Mathematics*, vol. 8, no. 1, pp. 33-42, March 1960

Table 1 Performance and Device Sizes Obtained under the First Specification

Performance and Device Sizes specifications	Parameters								Device Sizes						
	A_v	f_0 (MHz)	CMR (V)	SR (V/ μ s)	VOR (V)	P_{diss} (mW)	ϕ_M (Deg.)	W_1 (μ m)	W_3 (μ m)	W_5 (μ m)	W_6 (μ m)	W_7 (μ m)	C_c (pF)	I_{bias} (μ A)	
iteration 1	5000	1	3	2	4	10	60	52	11	10	326	160	5.32	10.32	
iteration 2*	16440	0.89	3.4	2.13	4.12	1.44	57.5	40	17	16	356	175	4.82	11.32	
iteration 3	19400	0.88	3.3	1.62	4.04	1.54	57.3	52	11	10	325	160	4.89	8.81	
iteration 4*	20140	0.92	3.3	1.59	4.02	1.82	59.4	64	13	12	395	194	5.76	10.22	
iteration 5	32060	1.08	3.5	1.85	4.35	1.82	59.3	98	52	46	961	474	7.34	15.69	
iteration 6	24970	1.05	3.4	1.99	4.31	1.81	59.3	76	35	32	698	344	6.52	14.72	
iteration 7	17320	0.93	3.3	1.85	4.06	1.83	59.3	56	14	13	380	188	5.57	11.45	
iteration 8	22650	1.02	3.4	1.97	4.25	1.82	59.5	70	28	26	602	297	6.27	13.91	
iteration 9	19910	1.00	3.4	2.08	4.20	1.83	59.4	62	24	22	531	262	5.99	13.92	
iteration 10	25920	1.03	3.4	2.02	4.36	1.82	60.5	78	45	41	808	398	7.15	16.36	

Conditions : $C_L = 20\text{pF}$, $V_{DD} = 5\text{V}$, $V_{SS} = -5\text{V}$
 * use random numbers as target in this iteration
 $f_0 = \omega_0/2\pi$, $\phi_M = 180^\circ/\pi$, $W_1 = W_2$, $W_3 = W_4$, $W_5 = W_8$, $I_{bias} = I_{D5}$, $L_n = 10\mu\text{m}$, $n=1, \dots, 8$
 W_n and L_n denote the channel width and length of MOS transistor n

Table 2 Performance and Device Sizes Obtained under the Second Specification

Performance and Device Sizes specifications	Parameters								Device Sizes						
	A_v	f_0 (MHz)	CMR (V)	SR (V/ μ s)	VOR (V)	P_{diss} (mW)	ϕ_M (Deg.)	W_1 (μ m)	W_3 (μ m)	W_5 (μ m)	W_6 (μ m)	W_7 (μ m)	C_c (pF)	I_{bias} (μ A)	
iteration 1	5000	1.5	3	3	4	10	45	43	11	10	295	146	2.93	8.64	
iteration 2*	18000	1.17	3.4	2.55	4.07	1.38	46.5	46	19	18	405	200	2.93	10.80	
iteration 3	22260	1.47	3.5	3.72	4.28	1.39	42.1	52	34	32	572	282	2.93	13.45	
iteration 4	19340	1.28	3.5	2.97	4.12	1.39	45.2	45	17	16	380	188	2.93	10.25	
iteration 5	18770	1.08	3.4	2.36	4.11	1.23	46.9	40	11	10	284	140	2.93	7.93	
iteration 6	33370	1.46	3.6	3.15	4.46	1.39	43.1	63	57	52	997	491	3.08	12.78	
iteration 7*	21450	1.18	3.4	2.25	4.09	1.38	46.4	52	12	10	332	164	3.07	8.08	
iteration 8	30210	1.64	3.6	3.80	4.45	1.39	38.4	68	57	52	851	420	2.93	14.74	
iteration 9	19320	1.20	3.4	2.58	4.10	1.37	46.3	44	12	11	318	157	2.93	8.81	
iteration 10*	19860	1.25	3.5	2.72	4.10	1.38	45.5	46	14	13	351	173	2.93	9.37	
iteration 11	20960	1.19	3.4	2.31	4.09	1.36	45.7	50	11	10	317	156	2.93	7.95	

Conditions : $C_L = 20\text{pF}$, $V_{DD} = 5\text{V}$, $V_{SS} = -5\text{V}$