A Novel Low-Voltage Silicon-On-Insulator (SOI) CMOS Complementary Pass-Transistor Logic (CPL) Circuit using Asymmetrical Dynamic Threshold Pass-Transistor (ADTPT) Technique

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Abstract

This paper reports a novel low-voltage silicon-on-insulator (SOI) CMOS complementary pass-transistor logic (CPL) circuit using asymmetrical dynamic threshold pass-transistor (ADTPT) technique. Using the ADTPT technique to dynamically control the body bias of the pass-transistor via only one auxiliary transistor, the new SOI CMOS complementary pass-transistor logic (CPL) circuit provides superior speed performance at a low supply voltage as compared to the conventional pass-transistor logic circuits without the ADTPT technique as verified by the MEDICI simulation results. The ADTPT technique is especially effective for use in CPL circuits with serially-connected multiple inputs.

Summary

I Introduction

CMOS Dynamic Threshold (DTMOS) technique [1] has been used to realize ultra-low-voltage silicon-on-insulator (SOI) VLSI circuits with a supply voltage of smaller than 0.7V. By directly connecting the body of an SOI MOS device to its gate, its driving current can be enhanced without increasing the off-state leakage current. However, this body-tied-to-gate DTMOS technique is difficult to be adopted for VLSI circuits with a supply voltage higher than 0.7V. In order to take full advantage of the body bias control capability of the DTMOS technique designed for SOI CMOS technology, the smart body-contact techniques using added auxiliary transistors have been proposed [2]-[4]. However, the increased transistor count from using the smart body-contact techniques makes DTMOS circuits become a major drawback. Thus, the DTMOS technique has not been often used to implement VLSI logic circuits.

Pass-transistor logic circuits have been known for their advantages in high density, high speed and low power [5]. The reduced logic-1 signal from its supply voltage in a pass-transistor may refrain itself from low-voltage applications. SOI DTMOS technique using two extra auxiliary transistors for each pass-transistor — symmetrical dynamic threshold pass-transistor (DTPT) technique as shown in Fig. 1 [6] has been utilized to resolve this reduced logic-1 signal problem. However, the layout area of the DTPT circuit may increase substantially. In addition, as shown in the figure, since the body node is in the middle of the two extra auxiliary devices, the enhancement of the body bias provided by the structure for the DTPT circuit may not be effective.

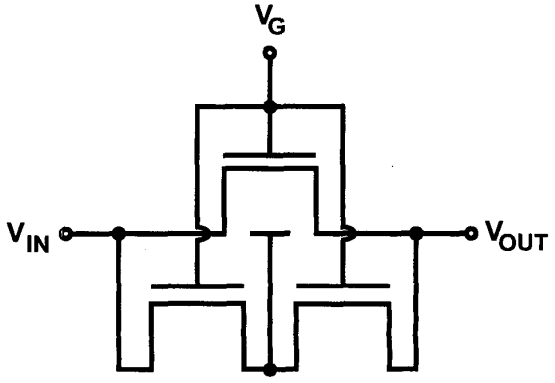

Figure 1. Conventional symmetrical dynamic threshold pass-transistor (DTPT) circuit with two auxiliary transistors.

In this paper, a new asymmetrical dynamic threshold pass-transistor (ADTPT) technique using SOI CMOS dynamic threshold (DTMOS) technique to dynamically control the body bias of the pass-transistor via only one auxiliary transistor, for high-speed operation at a low supply voltage is described. It will be shown that using this ADTPT technique, the complementary pass-transistor logic (CPL) circuit [7] — CPL-ADTPT circuit provides a superior speed improvement at a low supply voltage as compared to the conventional pass-transistor logic circuits without the ADTPT technique, as verified by the MEDICI simulation results. It will also be shown that the ADTPT technique is especially effective for use in CPL-ADTPT circuits with serially-connected multiple inputs. In Section II, the operation of the ADTPT technique is described first, followed by the CPL-ADTPT circuit, which adopts the ADTPT technique in the complementary

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pass-transistor logic (CPL) circuit in Section III and conclusion.

II Asymmetrical Dynamic Threshold Pass-Transistor (ADTPT) Technique

Fig. 2 shows the new asymmetrical dynamic threshold pass-transistor (ADTPT) circuit using NMOS devices. Different from the conventional dynamic threshold pass-transistor (DTPT) circuit, which includes two extra auxiliary transistors symmetrically as shown in Fig. 1, the ADTPT circuit as shown in Fig. 2 needs only one extra auxiliary transistor to control the body bias of the pass-transistor. In the conventional dynamic threshold pass-transistor (DTPT) circuit as shown in Fig. 1, the body of the main pass-transistor is connected to the source/drain node of the two auxiliary transistors with their gates tied to the gate of the main pass-transistor. In addition, the other source/drain nodes of these two auxiliary transistors are connected to the source and the drain of the main pass-transistor, respectively. Furthermore, the bodies of these auxiliary transistors are floating. In contrast, as shown in Fig. 2, in the ADTPT circuit, the body of the main pass-transistor is connected to the source/drain node of the auxiliary transistor, whose gate is also tied to the gate of the main pass-transistor and its body is tied to the source/drain node of the main pass-transistor, instead of floating as in the conventional DTPT case.

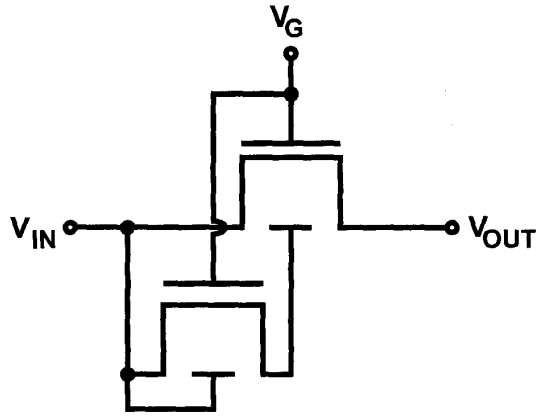

Figure 2. Asymmetrical dynamic threshold pass-transistor (ADTPT) circuit.

The advantage of the new ADTPT circuit can be understood by considering its logic operation. When V_G is high (V_{DD}), both the pass-transistor and the auxiliary transistor are on. During the pass-logic-1 operation, the logic-1 level is propagated from the input V_{IN} to the output V_{OUT}. When the input V_{IN} increases from low to high, due to the function of the auxiliary transistor, the body of the main pass-transistor (V_B) is raised to V_{DD}-V_{TN}(V_B=V_{DD}), where V_{TN}(V_B=V_{DD}) is the threshold voltage of the auxiliary transistor biased with a body bias of V_B=V_{DD}. Compared to the conventional dynamic threshold pass-transistor (DTPT) circuit as shown in Fig. 1, the new ADTPT circuit has a faster speed owing to a higher body voltage provided by its auxiliary transistor — in the conventional dynamic threshold pass-transistor (DTPT) circuit, due to its two auxiliary transistor structure, the body bias of the main pass-transistor is half-way between the input V_{IN} (=V_{DD}) and the output V_{OUT}, which rises from 0V to V_{DD}-V_{TN}. In the new ADTPT circuit, owing to the single-auxiliary transistor structure, the body bias of the main pass-transistor is tied to a higher level V_{DD}-V_{TN}(V_B=V_{DD}). Therefore, the effective threshold voltage of the main pass-transistor of the new ADTPT circuit is much smaller as compared to the conventional case. As a result, a higher speed in passing the logic-1 signal from the input V_{IN} to the output V_{OUT} can be obtained.

Fig. 3 shows the transient waveforms of (a) conventional pass-transistor circuit without an auxiliary transistor, (b) conventional dynamic threshold pass-transistor (DTPT) circuit with two auxiliary transistors, and (c) ADTPT circuit, during the pass-logic-1 operation, with 1V imposed at the gate and a voltage step from 0V to 1V applied at the input of the main pass-transistor, based on MEDICI simulation results [8]. All transistors are SOI NMOS devices with a channel length of 0.25-μm. The channel width of the main pass-transistor in the ADTPT circuit and the conventional

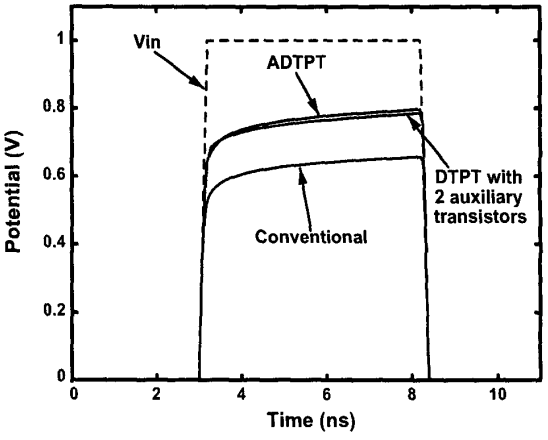

Figure 3. Transient waveforms of (a) conventional pass-transistor circuit without an auxiliary transistor, (b) conventional dynamic threshold pass-transistor (DTPT) circuit with two auxiliary transistors, and (c) asymmetrical dynamic threshold pass-transistor (ADTPT) circuit, during the pass-logic-1 operation, with 1V imposed at the gate and a voltage step from 0V to 1V applied at the input of the main transistor, based on MEDICI simulation results.

dynamic threshold pass-transistor (DTPT) circuit with two auxiliary transistors is 1-μm. The channel width of the conventional pass-transistor without the auxiliary device is 2-μm. The channel width of all auxiliary transistors is 0.3-μm. As shown in Fig. 3, due to the negative influence caused by the body effect, the output voltage V_{OUT} of the conventional pass-transistor without an auxiliary transistor can only be raised to 0.66V in 5ns after the input V_{IN} turns high to 1V. In contrast, the output of the conventional dynamic threshold pass-transistor (DTPT) circuit with two auxiliary transistors is raised to 0.75V at 5ns. Among three, ADTPT circuit has the best performance — its output rises to 0.8V at 5ns, which is a 20% improvement as compared to the conventional pass-transistor without an auxiliary transistor. Although the two auxiliary transistors in the DTPT circuit provide an extra conduction path from the input to the output, the body voltage of its main pass-transistor cannot be enhanced effectively as compared to the ADTPT case, where the input voltage V_{IN} affects the body voltage V_B of the main pass-transistor and the auxiliary transistor simultaneously. Therefore, the threshold voltage of the main transistor in the ADTPT circuit can be reduced more effectively, which leads to a higher conduction capability of the main pass-transistor.

III SOI Complementary Pass-Transistor Logic (CPL) with ADTPT

Complementary pass-transistor logic (CPL) circuit [7] is a major technique for realizing digital VLSI logic circuits. A CPL circuit contains pass-transistors and inverters used as buffers at the end to recover the logic-1 level. The new ADTPT technique is especially useful for implementing the CPL circuit. Fig. 4 and Fig. 5 show the AND/NAND logic circuits implemented by the ADTPT technique and conventional DTPT technique with two auxiliary transistors,

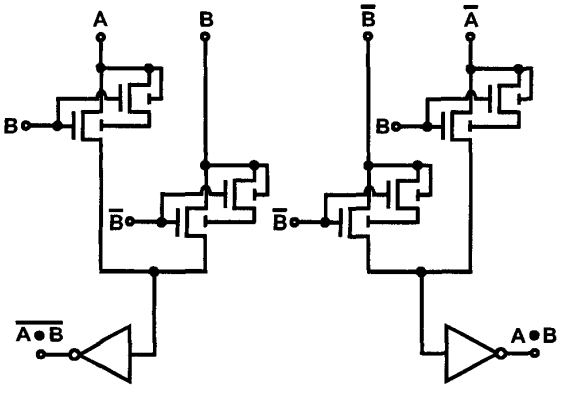

Figure 4. AND/NAND CPL circuit implemented by ADTPT technique.

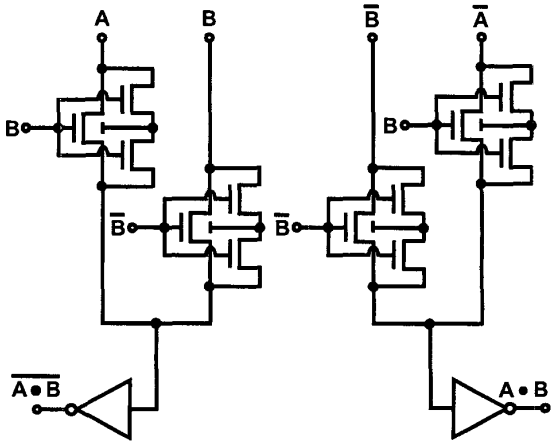

Figure 5. AND/NAND CPL circuit implemented by conventional DTPT technique with two auxiliary transistors.

respectively. Fig. 6 shows fall time versus V_{DD} of the three CPL circuits using (a) conventional pass-transistor circuit without an auxiliary transistor, (b) conventional DTPT technique with two auxiliary transistors, and (c) ADTPT technique. As shown in the figure, among three cases, the ADTPT one has the smallest fall time. In addition, at a smaller V_{DD}, the advantages of the ADTPT technique are more noticeable — ADTPT technique is the most advantageous for use at a low supply voltage. Plus, the ADTPT technique is more concise as compared to the DTPT technique with two auxiliary transistors — only one auxiliary transistor is required.

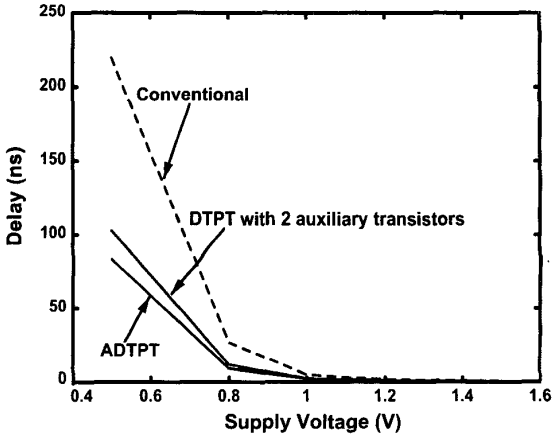

Figure 6. Fall time versus V_{DD} of the three CPL circuits using (a) conventional pass-transistor circuit without an auxiliary transistor, (b) conventional DTPT technique with two auxiliary transistors, and (c) ADTPT technique.

The compactness of the ADTPT technique used for realizing low-voltage SOI CPL is beyond our description so far. The strength in the conciseness of the ADTPT technique for low-voltage SOI CPL can be demonstrated in a 4-to-1 multiplexer circuit implemented by SOI CPL using ADTPT technique as shown in Fig. 7. Note that in Fig. 7, due to the complementary structure, only half of the circuit is drawn in the figure. As shown in the figure, instead of using an independent auxiliary transistor for each main pass-transistor in each row in the circuit, only one auxiliary transistor for each row is sufficient.

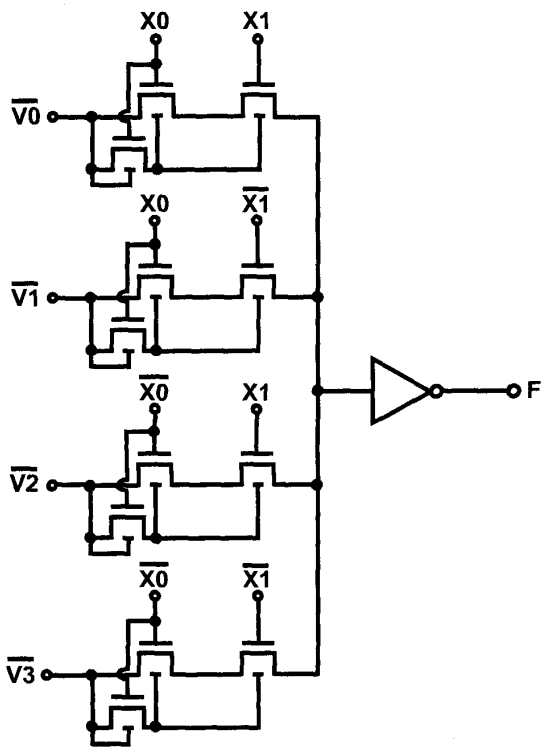

Figure 7. A 4-to-1 multiplexer implemented by CPL using the ADTPT technique.

IV Conclusion

In this paper we report a novel low-voltage silicon-on-insulator (SOI) CMOS complementary pass-transistor logic (CPL) circuit using asymmetrical dynamic threshold pass-transistor (ADTPT) technique. Using the ADTPT technique to dynamically control the body bias of the pass-transistor via only one auxiliary transistor, the new SOI CMOS complementary pass-transistor logic (CPL) circuit provides superior speed performance at a low supply voltage as compared to the conventional pass-transistor logic circuits without the ADTPT technique as verified by the MEDICI simulation results. The ADTPT technique is especially effective for use in CPL circuits with serially-connected multiple inputs.

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