coefficient has been obtained by changing to the new configuration.

Conclusions: A new waveguide six-port reflectometer covering the frequency range 26·5–40 GHz, which makes use of a symmetrical five-port junction, has been described. In comparison with a previous design, the new configuration has been shown to be more nearly ideal, providing improvement measurement resolution as a function of frequency. Studies of further configurations based on the five-port junction are in progress.

6th December 1992

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* Employed by Siemens Plessey Assessment Services Limited and is working under contract at the National Physical Laboratory

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ANALYTICAL DELAY MODEL OF CMOS INVERTER INCLUDING CHANNEL-LENGTH MODULATION

H.-C. Chow and W.-S. Feng

Indexing terms: Semiconductor devices and materials, Field-effect transistors

An analytical delay model of a CMOS inverter is introduced for the first time which includes channel-length modulation, source-drain resistance and high-field effects. Calculations of the rise, fall and delay times show good agreement with SPICE simulations.

Introduction: Transient analysis of a CMOS inverter has been performed by many authors [1–6]. The models in References 1–3 were based on the Shockley MOSFET model which does not include the carrier velocity saturation effects. Therefore, these models are not suitable for applications to short-channel MOSFET circuits. Although other models [4, 5] were developed with high-field effects, both the channel-length modulation effect and the parasitic source-drain resistance effect were neglected. Despite the proposal of another, better, model [6], the deficiency of the linear region operation was observed and the channel-length modulation effect was not included. Therefore, we report for the first time an analytical delay model of a CMOS inverter which considers channel-length modulation, the source-drain resistance, and high-field effects.

Model development: For the drain currents under linear and saturation operation, we incorporate our improved analytical short-channel current–voltage model [*] into the switching analysis. The MOSFET I–V model includes all second-order effects for an accurate reproduction of the static characteristics of submicrometre MOS devices. Drain current expressions are summarised as

$$I_{DL} = \frac{-A_2 + \sqrt{(A_2^2 + 4A_1 I_{D0})}}{2A_1} \qquad (V_{DS} \le V_{DSAT}) \quad (1)$$

$$I_{DSAT} = \frac{I_{DS}}{1 - \dfrac{L_{SAT}}{L_{eq}}} \qquad (V_{DS} > V_{DSAT}) \quad (2)$$

where V_{DSAT} is the drain saturation voltage, i_{ds} the drain current at the onset of saturation and L_{SAT} the channel shortening length. The details have been given elsewhere [7].

In this work the delay time T_D of a CMOS inverter is approximately defined as (fall time T_f + rise time T_r)/2. In the evaluation of delay times we focus on the discharging process of the loading capacitance under the assumption of a step input. The fall time consists of two intervals as follows:

(1) T_{f1} period, during which the loading capacitor voltage V_{out} drops from $0{\cdot}9V_{DD}$ to V_{DSAT}

(2) T_{f2} period, during which the loading capacitor voltage V_{out} drops from V_{DSAT} to $0{\cdot}1V_{DD}$.

The differential equation which governs the behaviour of the inverter during the first period is

$$C_{load}\frac{dV_{out}}{dt} + I_{DSAT} = 0 \quad (3)$$

where C_{load} is the loading capacitance. Rewriting eqn. 3, we obtain

$$C_{load}\frac{dV_{out}}{dt} = -I_{DSAT} = -\frac{I_{DS}}{1 - L_{SAT}/L_{eq}} \quad (4)$$

Integrating eqn. 4 with respect to the corresponding variable with suitable boundaries, we obtain

$$\int_{V_{DSAT}}^{0{\cdot}9V_{DD}} \left(1 - \frac{L_{SAT}}{L_{eq}}\right) dV_{out} = \frac{I_{DS}}{C_{load}} T_{f1} \quad (5)$$

The second term of the left part is the contribution of channel-length modulations. By changing the integrating variable from V_{out} to L_{SAT}, the integration can be carried out in a straightforward manner. As for the relationship between V_{out} and L_{SAT}, it is derived from a quasi-two-dimensional analysis for an MOSFET operated in the saturation region [7]:

$$dV_{out} = \left[E_c \cosh(L_{SAT}/l) + \frac{\left(V_{DSAT} - V^*_{dsat} + \dfrac{q\eta N_A l^2}{\varepsilon_s}\right)}{l} \sinh(L_{SAT}/l)\right] \times dL_{SAT} \quad (6)$$

Incorporating the relationship into eqn. 5, the final result of the left part is

$$\text{left part} = (0{\cdot}9V_{DD} - V_{DSAT}) - \frac{1}{L_{eq}}(A + B) \quad (7)$$

where $A = l^2E_c(x \sinh x - \cosh x + 1)$, $B = l(V_{DSAT} - V^*_{dsat} + q\eta N_A l^2/\varepsilon_s)(x \cosh x - \sinh x)$ and $lx = L_{SAT}|_{V_{DS}=0{\cdot}9V_{DD}}$. Therefore, T_{f1} is obtained and the channel-length modulation effect is introduced into the analysis for the first time as compared to others [1–6]. As for the derivation of T_{f2} we assume no source-drain resistance for simplicity. During this discharging interval the *n*MOS device is operated in the linear region and the drain current is I_{D0}. Substituting this current into eqn. 3, we obtain the following results:

$$\frac{\beta}{C_{load}} T_{f2} = \frac{M}{a_0} \ln \frac{(V_{GS} - V_T - 0{\cdot}1a_0 V_{DD})}{(V_{GS} - V_T - a_0 V_{DSAT})} + N \ln \frac{V_{DSAT}}{0{\cdot}1V_{DD}} \quad (8)$$

* CHOW, H.-C., and FENG, W.-S.: 'An improved analytical model for short-channel MOSFET's', submitted to *IEEE Trans. Electron Devices*

where $\beta = W_{eff}\mu_{eff}C_{ox}/L_{eff}$, $M = 1/(L_{eff}E_c) + a_0/(V_{GS} - V_T)$ and $N = 1/(V_{GS} - V_T)$. Because the fall time T_f is given as $T_{f1} + T_{f2}$, it can be determined analytically. Applying the similar analysis to the charging process, the rise time T_r can be obtained due to the symmetry of CMOS circuits. Therefore, we can approximately express the delay time T_p as $(T_f + T_r)/2$.

Results and conclusions: In this Section we first demonstrate the superior advantages of the I–V model used in this work over existing models. Fig. 1*a* and *b* show the simulated current–voltage characteristics of an *n*MOS device with $L_{eff} = 0{\cdot}806\,\mu m$, $W_{eff} = 10\,\mu m$ and $t_{ox} = 250\,Å$ for both $R_{sd} = 0$ and $60\,\Omega$, respectively. Note that R_{sd} denotes the total parasitic source-drain series resistance. In Fig. 1 both DC models used by the authors [4, 5] which include the carrier velocity saturation effects are also plotted. For comparison we fit these three models to $V_{DS} = 5\,V$ and $V_{GS} = 5\,V$. It is observed that much better agreement between the results of this improved model and MINIMOS 2D numerical simulations is obtained over the whole bias range than for the other two models. This accuracy is due to the adequate consideration of channel-length modulations and the source-drain resistance which both become important for submicrometre MOS devices.

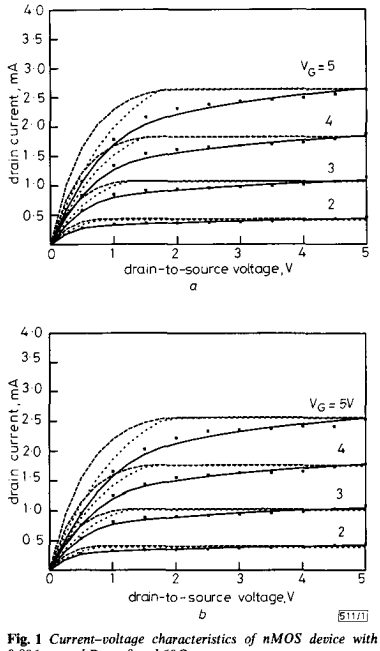

Fig. 1 *Current–voltage characteristics of nMOS device with $L_{eff} = 0{\cdot}806\,\mu m$ and $R_{sd} = 0$ and $60\,\Omega$*

$v_{sat} = 7 \times 10^6$ cm/s and $\mu_0 = 500\,cm^2/V\,s$
a $R_{sd} = 0\,\Omega$
b $R_{sd} = 60\,\Omega$
■ MINIMOS
——— model (this work)
------- Sodini *et al.*
– – – – Donald *et al.*

The calculated results of the fall, rise and delay times of a CMOS inverter plotted against the loading capacitance as a function of the source-drain resistance are presented in Fig. 2*a–c*, respectively, with SPICE MOS level 3 simulations. The used aspect ratio of the inverter is $W_{eff}/L_{eff} = 20\,\mu m/1\,\mu m$ for the *p*MOS and $10\,\mu m/1\,\mu m$ for the *n*MOS devices. For SPICE simulations we also insert both a source and drain resistor associated with the source and drain terminals of the *n*MOS and *p*MOS devices to account for the source-drain resistance effect. As for our proposed model it is capable of handling both the source-drain resistance and the channel-length modulation effect explicitly for the first time in the literature.

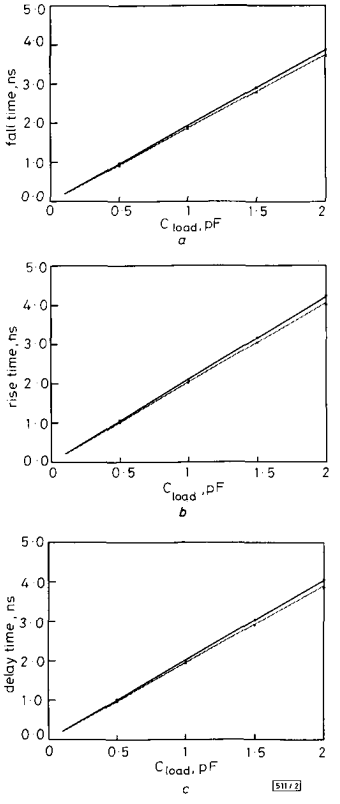

Fig. 2 *Calculated results with SPICE simulations plotted against loading capacitance as function source-drain resistance*

——— $R_{sd} = 60\,\Omega$
------- $R_{sd} = 0\,\Omega$
a Fall time
b Rise time
c Delay time
■ SPICE
——— model (this work)
····· model (this work)

Good agreement with SPICE simulations is also obtained due to the above two important reasons. Therefore, this analytical delay model is favourable for applications of time-delay optimisations of submicrometre MOSFET circuits.

4th December 1991

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INVESTIGATION OF OPTICAL FIBRE SWITCH USING ELECTRO-OPTIC INTERLAYS

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Indexing terms: Optical switching, Optical fibres, Integrated optics

Efficient switching of power (>95%) between an optical fibre, side polished close to the core, and a high index multimode overlay waveguide can be induced by variation of the overlay waveguide parameters. Using lithium niobate sandwiched between two optically transparent indium-tin-oxide electrodes as the overlay, electro-optic switching has been observed. By applying a second side-polished fibre to the overlay top surface, power may be switched between the two fibres. The feasibility of such an electro-optically controlled optical fibre routing switch is demonstrated.

Introduction: At the present time, there is a requirement for components such as optical fibre switches and variable ratio couplers or taps for applications in areas such as telecommunications, optical signal processing and sensing systems, e.g. signal routing, element weighting, detection purposes, etc. The current methods of implementing these components are generally of a mechanical nature relying on the relative transverse movement of exposed fibre cores in evanescent contact [1] or the relative movement of butt coupled fibres. Nonmechanical implementations require the use of integrated optics and thus suffer from severe fibre to device interfacing problems due to the need to break the fibre for device insertion. We present results of an investigation of an all solid state structure, free from interfacing problems, in which switching or tap weight control may be achieved electro-optically.

It has been previously demonstrated [2] that power can be switched between a singlemode optical fibre, side-polished close to the core, and a multimode planar waveguide overlay of index greater than the fibre effective index n_{ef}. Strong directional coupling of power occurs when the highest order mode of the overlay is matched in effective index to the single fibre mode [2–4]. This can be achieved by variation of the waveguide parameters, i.e. material index or thickness or wavelength. We propose a switch structure (Fig. 1), based on the above principle, which comprises a polished fibre block evanescently coupled to a thin (1–20 μm) planar interlay of electro-optic material sandwiched between optically transparent indium-tin-oxide electrodes. A second fibre is applied to the top surface of the interlay to collect power coupled from the first fibre. The output response of both fibres in the switch structure is related to the dispersion equation for the interlay waveguide [5]:

$$\frac{2\pi d}{\lambda}(n_0^2 - n_{eo}^2)^{1/2} = m\pi + 2\tan^{-1}\xi\left(\frac{n_{eo}^2 - n_c^2}{n_0^2 - n_{eo}^2}\right)^{1/2} \quad (1)$$

where λ is the input wavelength, d is the overlay thickness, n_{eo} is the mode effective index, m is the mode order and ξ is a polarisation dependent constant. The modes of the waveguide can range in effective index from the fibre cladding index n_c, to the waveguide material index n_0. For phasematching conditions, $n_{eo} = n_{ef}$, and because $n_0 > n_{ef}$, and n_{ef} is approximately equal to n_c, the value of the arctan function is negligible. Therefore, coupling of power from the fibre to the waveguide will be polarisation insensitive, in the absence of material birefringence, due to the symmetry of the structure. Eqn. 1 can then be reduced to

$$2d(n_0^2 - n_{ef}^2)^{1/2} = m\lambda \quad (2)$$

As the mode structure of the waveguide is tuned by varying either n_0 or d or λ, the number of supported modes varies and eqn. 2 holds for a discrete number of m values. As each new highest order mode is tuned in and out of a phasematching condition, power transfer to the overlay occurs [2–4] and a periodic transmitted intensity function is expected for both arms of the switch. Low loss transmission occurs in the input arm of the switch structure under phase mismatch conditions. Applying an electric field to the interlay will cause a shift in the waveguide material index, allowing tuning to a phasematching condition, and induce switching of power between the two fibres.

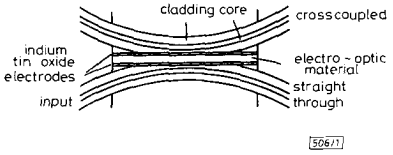

Fig. 1 *Cross-section of optical fibre routing switch*

Experimental investigation: To investigate the feasibility of the proposed switch structure, two test devices, of a similar device geometry but minus the electrodes, were fabricated. Tuning of the interlay waveguide mode structure was achieved by variation of the input wavelength using a scanning monochromator. This method of tuning was selected for test purposes due to its ease of implementation because variation of any of the waveguide parameters will achieve the same result of shifting the mode effective indices to a phasematching condition. For the first test device a piece of z-cut lithium niobate was bonded to the surface of a 1·3 μm singlemode polished fibre block [1] and lapped and polished to a thickness of approximately 10 μm. A second polished fibre block was then applied to the top surface of the $LiNbO_3$ and aligned to collect the optical power present in the interlay under phasematching conditions. The second test device was fabricated by depositing a thin film (2·5 μm) of zinc sulphide (ZnS), a high index dielectric material, directly onto the surface of a polished fibre block followed by alignment of the second polished fibre block. At specific wavelengths the highest order interlay mode effective index matches the fibre mode effective index and power couples to the interlay and then to the second fibre. Hence, the switching of power between the two fibres was expected to be wavelength dependent and of a periodic nature. A polarisation controller [6] was used in the input fibre of both test devices because $LiNbO_3$ is materially birefringent and waveguide birefringence may be significant in the ZnS structure.

Figs. 2 and 3, respectively, show the wavelength response of the transmitted and crosscoupled power for the 10 μm

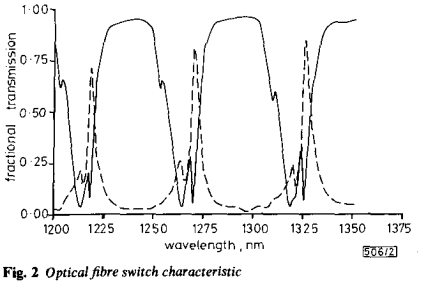

Fig. 2 *Optical fibre switch characteristic*
~10 μm $LiNbO_3$ interlay, TM polarisation
—— input arm
- - - - coupled arm