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A Coded Block Adaptive Neural Network Structure for Pattern Recognition VLSI

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Abstract

In this paper, a coded block adaptive neural network structure with a Hamming-Error-Correction-Technique (HECT), which can be used to greatly enhance the VLSI implementation capability of the block system using a parallel processor architecture, is presented. According to simulation results, the coded block system with HECT provides a shorter learning time, and a better reconfigurability, and an order-of-magnitude more efficient VLSI implementation capability.

Summary

A pattern recognition system, as shown in Fig. 1(a), is composed of a translation-invariant network and a standard adaptive two-layer network. The translation-invariant network is used to map a retinal image into multi-bit outputs [1]-[4]. The standard adaptive two-layer network [5], [6] can be trained to provide output responses corresponding to the original image as required. The block adaptive network structure for an $n \times n$ input array as shown in Fig.1(b) has been used to enhance the VLSI implementation capability and the learning speed [7][8]. However, the block adaptive network structure requires n^2 local blocks, which is still a bottleneck for VLSI implementation. In this paper, a coded local block systems with HECT, which requires an order-of-magnitude fewer local blocks, is presented. It will be shown that the coded local block system, which is suitable for VLSI implementation using a parallel processor architecture, has a better reconfigurability and a better learning speed. In order to investigate the potential of the coded local block structure for pattern recognition, an 8×8 local block system with eight local blocks and with 36 alphanumerics coded in ASCII format as training patterns is studied. In each coded local block, there are four neurons in the first layer and one neuron in the second layer. With the coded local block structure, the hardware needed to realize the parallel processor architecture is eight times smaller as compared to the local block system. Fig. 2 shows the learning curves of the system with the coded local blocks using the back propagation algorithm for various learning rates ($\eta's$). With the coded structure, a smaller η provides a shorter learning time, which is correlated to the initial weight values. HECT has been used to raise reliability of data transmission [9]. With HECT, the coded local block system, as shown in Fig. 3, requires four additional local blocks for the 8×8 system. Fig. 4 shows the learning time of each local block for the coded local structure with HECT for various learning rates. For the system implemented by the parallel processor architecture, the total learning time is determined by the local block with the longest learning time. As shown in Fig. 4, with $\eta = 0.5$, all local blocks converge quickly to the desired

output patterns except block 1 and 8.

With HECT, the coded local block system has a much shorter learning time by ignoring the local block with the longest learning time. In addition to a shorter learning time and a more efficient VLSI implementation capability, the coded local block structure with HECT has a better reconfigurability. As shown in Fig. 5, the recognition rate of the coded block system with HECT is better. In fact, the number of first layer neurons in the local block structure is critical in determing the learning time. Fig. 6 shows the learning time as a function of the number of neurons in the first layer of each local block for the coded local block system with various learning rates. With $\eta = 0.5$, the coded block system with four neurons in the first layer of each local block has a relatively short learning time. This means a reduction in complexity of the system. In conclusion, an efficient adaptive neural network structure with coded local blocks suitable for pattern recognition VLSI is presented. According to simulation results, the coded local blocks structure with HECT provides a better reconfigurability, a shorter learning time, and a much more efficient VLSI implementation capability using a parallel processor architecture.

Acknowledgments

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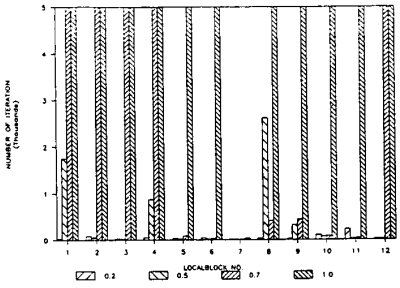

Fig.2 The learning curves of the coded local block system neural network for 8×8 inputs using the back propagation algorithm.

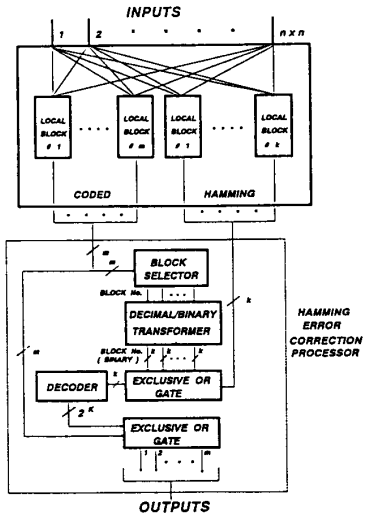

Fig. 3 The coded local block structure with HECT

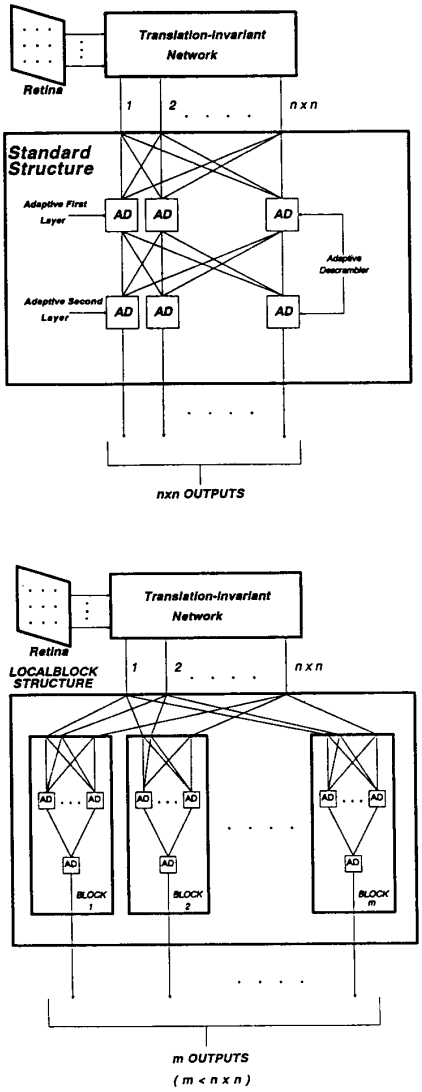

Fig.1 A pattern recognition system composed of a translation-invariant neural network and an adaptive two-layer network. (a)The conventional adaptive structure. (b)The adaptive structure with local blocks.

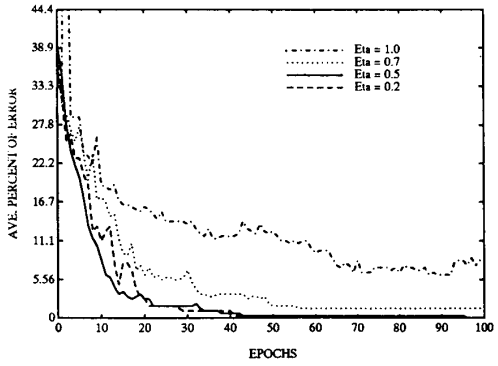

Fig. 4 The learning time of each local block in the coded local structure with HECT for various learning rates.

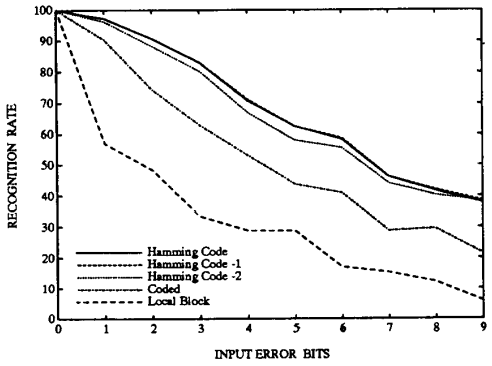

Fig. 5 The reconfigurability of the local block system with and without coding outputs for 8×8 inputs.

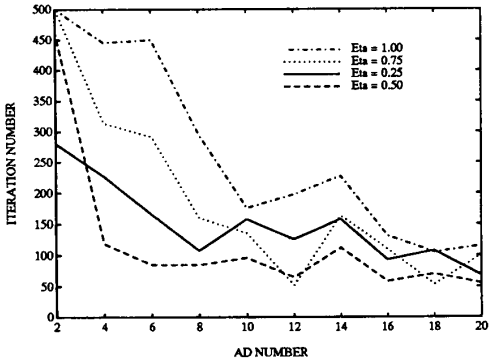

Fig. 6 The learning time vs. number of first layer neurons curves for the coded local block system