A Closed-form Physical Back-Gate-Bias Dependent Quasi-Saturation Model for SOI Lateral DMOS Devices with Self-Heating for Circuit Simulation

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Abstract

This paper reports a closed-form physical back-gate-bias dependent quasi-saturation model for silicon-direct-bonded lateral SOI DMOS devices with self-heating. By solving Poisson's equation in the substrate direction with the thermal equation, a closed-form physical SOI DMOS quasi-saturation model considering lattice temperature suitable for circuit simulation has been derived. Based on the analytical model, the surface state above the field oxide may effectively decrease the back gate bias effect on the quasi-saturation behavior in the SOI DMOS device. With a more negative back gate bias, the thermal effect on quasi-saturation is less influential.

Summary

SOI technology has been used for realizing high-voltage MOS devices for its advantages in integration density and latch up immunity [1]. For an ultra-thin SOI MOS device, the back gate bias effect on its device performance is complicated [2]. In addition, due to the field oxide, thermal effect cannot be overlooked for an SOI DMOS device. As in a bulk DMOS device, quasi-saturation may limit the performance of an SOI DMOS device [3]. In this paper, an analytical back-gate-bias dependent quasi-saturation model for a lateral SOI DMOS device [4] considering lattice temperature effect suitable for circuit simulation is described.

Fig. 1 shows the cross section of the lateral SOI DMOS device with its parameters as shown in Table 1 under study[4].

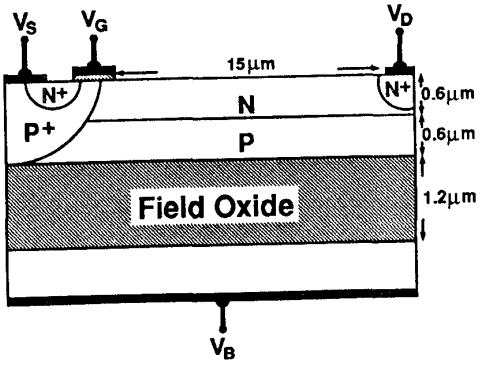

Figure 1: The cross section of the lateral SOI DMOS device under study.

Parameters	
N_D	8.5×10^{15} cm^3
N_A	1.5×10^{15} cm^3
t_n	0.6 μm
t_p	0.6 μm
W	200 μm
t_{oxb}	1.2 μm
L	15 μm
N_s	8×10^{11} cm^3
R_{th}	10^3 K/W
$v_{sat(300K)}$	7×10^6 cm/s
$\mu_{n(300K)}$	1000 cm^2/V·s
E_c	1.8×10^4 V/cm

Table 1: Important parameters of the SOI lateral DMOS device [10].

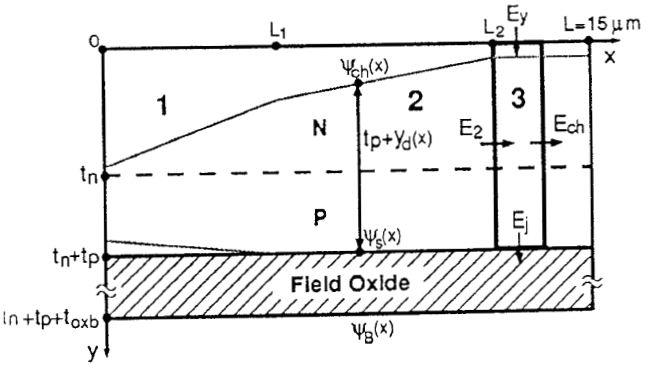

Figure 2: Partitioning of the thin film of the Lateral SOI DMOS device under study.

The SOI DMOS device has an n+ polysilicon gate and a front gate oxide of 400Å and a $1.2\mu m$ thin film above an oxide insulator of $1.2\mu m$. In the thin film, an n-type drift region of $15\mu m$ in length with a doping density of $8.5 \times 10^{15} cm^{-3}$ sits atop a $0.6\mu m$ p-type layer with a doping density of $1.5 \times 10^{15} cm^{-3}$. On the surface of the field oxide, an $8 \times 10^{11} cm^{-2}$ surface state is assumed. As in the bulk vertical DMOS device [3], the drain current of a lateral SOI DMOS device biased at quasi-saturation is determined by the current conduction in the n-type drift region. A more negative back gate bias leads to a smaller channel depth in the drift region. As the back gate bias is more negative, hole accumulation atop the field oxide exists. In order to simplify the analysis, as indicated in Fig. 2, the n-type drift region is divided into three regions – (1) the hole accumulation region, (2) the low electric field region, and (3) the high electric field region. In Region (1), due to hole accumulation, the potential above the field oxide is a constant: $\psi_s(x) = \phi_{fp}$ for $x \leq L_1$. In Region (2), the p-type region is fully depleted. From the 1D Poisson's equation in the substrate direction, the potential difference across the depletion region is as shown in Eq. (1) in Fig. 3. Applying Gauss' Law in Region (2), one obtains Eq. (2). As $V_{BS} < V_{BS1}$ (Note V_{BS1} is shown in Eq. (3)), Region (1) exists. The current in Region (2) is expressed as Eq. (4). From Eqs.(1)(2)(4), the drain current at quasi-saturation is as shown in Eq. (5). As indicated in Eq. (5), the effect of Region (1) is included by variable F as shown in Eq. (6). In Region (3), as a result of a high electric field, channel pinches off and electrons travel at a saturated velocity. Considering the lateral voltage drop in three regions, one obtains Eqs.(7)-(9). Applying Gauss' Law in the high electric

$$\psi_{ch}(x) - \psi_s(x) = \frac{qN_D}{2\epsilon_{si}} y_d(x)^2 + \frac{qN_D}{\epsilon_{si}} y_d(x) t_p - \frac{qN_A}{2\epsilon_{si}} t_p^2 \quad (1)$$

$$qN_D y_d(x) - qN_A t_p = C_{ox}(\psi_s(x) - V_{BS}) - Q_s \quad (2)$$

$$V_{BS1} = \phi_{fp} + \frac{C_n Q_D}{C_p C_{ox}} + \frac{Q_A}{C_{ox}} - \frac{Q_s}{C_{ox}} - \frac{C_n}{C_{ox}} \sqrt{(\frac{Q_D}{C_p})^2 + \frac{2Q_D}{C_n}(\frac{Q_A}{2C_p} + \phi_{fn} - \phi_{fp})} \quad (3)$$

$$I_D = W(Q_D - Q_A + Q_s - C_{ox}(\psi_s(x) - V_{BS})) \cdot \frac{v_{sat}}{\frac{1}{2} + \frac{E_c}{\frac{2(\psi_{ch}(x)}{dx}}} \quad (4)$$

$$I_D = \frac{W v_{sat}(N1 + N2) + E_c F}{\frac{1}{2}D + E_c L_2} \quad (5)$$

$$N1 = k1(Q_D - Q_A + Q_s + C_{ox}V_{BS})(\psi_s(L_2) - \psi_s(L_1)) - \frac{C_{ox}^3}{3C_n Q_D}(\psi_s(L_2)^3 - \psi_s(L_1)^3)$$

$$N2 = \frac{1}{2}(\frac{C_{ox}^2}{C_n Q_D}(Q_D - Q_A + Q_s + C_{ox}V_{BS}) - k1 C_{ox})(\psi_s(L_2)^2 - \psi_s(L_1)^2)$$

$$D = k1(\psi_s(L_2) - \psi_s(L_1)) + \frac{C_{ox}^2}{2C_n Q_D}(\psi_s(L_2)^2 - \psi_s(L_1)^2)$$

$$k1 = 1 + \frac{C_{ox}}{C_p} + \frac{C_{ox}}{C_n Q_D}(Q_A - Q_s) - \frac{C_{ox}^2 V_{BS}}{C_n Q_D}$$

$$F = \frac{W q \mu_n N_D (y_d(L_1) - y_d(0))(\psi_{ch}(L_1) - \psi_{ch}(0))}{ln(t_n - y_d(0)) - ln(t_n - y_d(L_1))} \quad (6)$$

$$\psi_{s1}(L_2) = V_{BS} + \frac{Q_D - Q_A + Q_s}{C_{ox}} \quad (7)$$

$$\psi_{s2}(L_2) = E_c L \quad (8)$$

$$\psi_s(L_2) = \psi_{s1}(L_2) + \psi_{s2}(L_2) - \sqrt{\psi_{s1}(L_2)^2 + \psi_{s2}(L_2)^2} \quad (9)$$

$$L_2 = L - \sqrt{\frac{\epsilon_{si}(t_n + t_p)}{C_{ox}}} sinh^{-1}\left(\frac{V_{DS} + \phi_{fn} - \frac{(Q_A - Q_s + (\psi_s(L_2) - V_{BS}))^2}{2C_n Q_D}}{2E_c\sqrt{\frac{\epsilon_{si}(t_n + t_p)}{C_{ox}}}} - \frac{\frac{1}{2}Q_A - Q_s + C_{ox}(\psi_s(L_2) - V_{BS})}{C_p} - \psi_s(L_2)}{2E_c\sqrt{\frac{\epsilon_{si}(t_n + t_p)}{C_{ox}}}}\right) \quad (10)$$

$$v_{sat}(T) = v_{sat}(300) - 5.7 \times 10^3 \cdot \Delta T \quad (11)$$

$$\mu_n(T) = \mu_n(300) - 6.47 \cdot \Delta T + 0.011 \cdot \Delta T^2 \quad (12)$$

$$\Delta T = \frac{-B - \sqrt{B^2 - 4AC}}{2A} \quad (13)$$

$$A = \frac{0.011 \cdot R_{th} V_{DS} E_c F}{\mu_n(300)}$$

$$B = \frac{-6.47 \cdot R_{th} V_{DS} E_c F}{\mu_n(300)} - 5.7 \times 10^3 \cdot R_{th} V_{DS} W(N1 + N2) - \frac{1}{2}D - E_c L_2$$

$$C = R_{th} V_{DS} E_c F + R_{th} V_{DS} W(N1 + N2) v_{sat}(300)$$

Figure 3: Important equations.

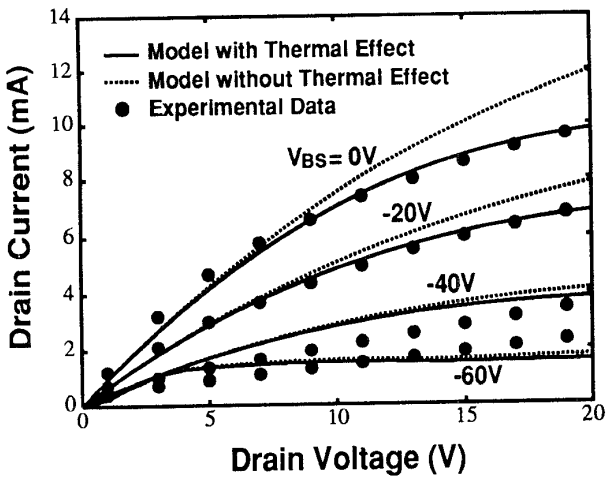

Figure 4: The drain current versus drain voltage curves for the lateral SOI DMOS device biased at quasi-saturation ($V_{BS} = 0V, -20V, -40V, -60V$) based on the analytical model and experimental data [4].

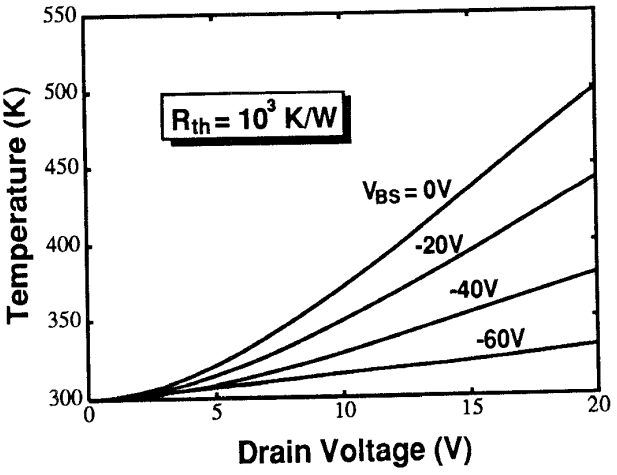

Figure 5: The lattice temperature versus the drain current for the lateral SOI DMOS device biased at quasi-saturation ($V_{BS} = 0V, -20V, -40V, -60V$).

field region - as shown in Fig. 2, the length of Region (3) is as shown in Eq. (10). Considering the thermal effect ($\Delta T = R_{th} I_D V_{DS}$) with the temperature dependent mobility and saturated velocity model [4] as shown in Eqs.(11)(12), the lattice temperature due to self-heating effect is Eq.(13). From Eqs.(5)(11)-(13), a closed-form analytical back-gate-bias dependent quasi-saturation model considering self-heating effect has been derived.

In order to verify the validity of the closed-form analytical model for the lateral SOI DMOS device, the analytical model results have been compared to the experimental data [4]. Fig. 4 shows the drain current versus the drain voltage curves for the SOI DMOS device biased at quasi-saturation ($V_{BS} = 0V, -20V, -40V, -60V$) based on the analytical model and the experimental data [4]. A more negative back gate bias makes the drain current at quasi-saturation smaller. In addition, a higher drain voltage leads to a higher drain current at quasi-saturation. Considering thermal effect, the drain current at quasi-saturation declines at a large drain voltage due to the degraded mobility and saturated velocity at an elevated lattice temperature. As shown in Fig. 5, a higher back gate bias will lead to a smaller increase in the lattice temperature. Fig. 6 shows the drain current at quasi-saturation vs. the doping density of the p-type region. A higher p-type doping density leads to a smaller drain current. In addition, with a more negative back gate bias, the thermal effect is less influential. Fig. 7 shows the drain current versus the surface state density above the field oxide. As shown in the figure, the drain current at quasi-saturation can be increased by raising the surface state density above the field oxide. For a more negative back gate bias, the drain current at quasi-saturation stays almost unchanged regardless of surface state density above the field oxide as a result of hole accumulation atop the field oxide. For a less negative back gate bias, the thermal effect is serious. On the other hand, with a more negative back gate bias, thermal effect is small. Fig. 8 shows the drain current at quasi-saturation versus the field oxide thickness for various back gate biase. As shown in the figure, a thicker field oxide leads to a higher drain current at quasi-saturation because of a thinner depletion layer in the n-type drift region. With a more negative back gate bias, the drain current at quasi-saturation is more sensitive to the field oxide thickness. In addition, for a more negative back gate bias, the thermal effect is less influential.

Conclusion

In this paper, a closed-form physical back-gate-bias dependent quasi-saturation model for silicon-direct-bonded lateral SOI DMOS devices with self-heating. By solving Poisson's equation in the substrate direction with the thermal equation, a closed-form physical

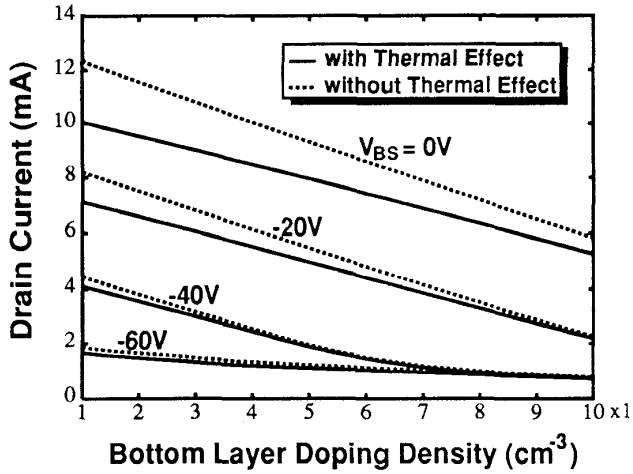

Figure 6: The drain current versus the doping density of the p-type bottom layer of the SOI lateral DMOS device biased at quasi-saturation, for $V_{DS} = 20V$ and $V_{BS} = 0, -20V, -40V, -60V$ with and without considering thermal effect.

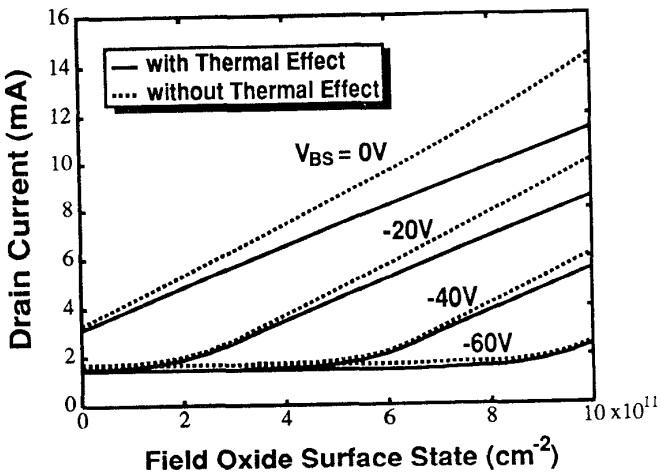

Figure 7: The drain current versus the field oxide surface state density for the lateral SOI DMOS device biased at quasi-saturation.

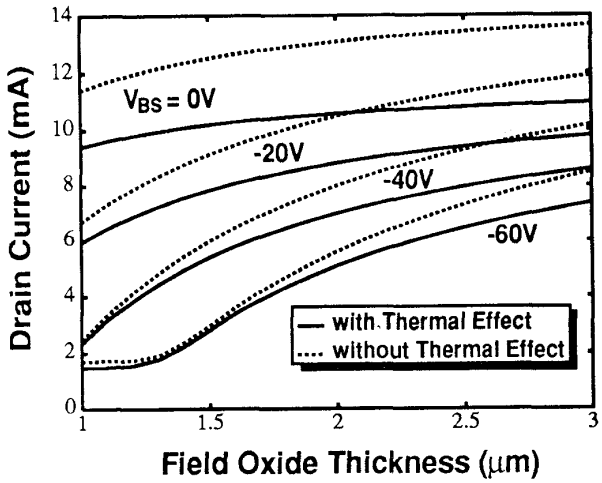

Figure 8: The drain current versus the field oxide thickness for the Lateral SOI DMOS device biased at quasi-saturation.

SOI DMOS quasi-saturation model considering lattice temperature suitable for circuit simulation has been derived. Based on the analytical model, the surface state above the field oxide may effectively decrease the back gate bias effect on the quasi-saturation behavior in the SOI DMOS device. With a more negative back gate bias, the thermal effect on quasi-saturation is less influential.

Acknowledgments

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