

DC-to-15- and DC-to-30-GHz CMOS Distributed Transimpedance Amplifiers

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Abstract — Two broadband transimpedance amplifiers (TIAs) for optical applications were realized in a 0.18- μm CMOS technology. The first TIA cascading two three-stage cascode distributed amplifiers achieves a transimpedance gain of 58 dB Ω and a bandwidth of 15 GHz. The other using a cascode distributed amplifier achieves a transimpedance gain of 48 dB Ω and a bandwidth of 30 GHz. The TIAs utilizing distributed technique with cascode gain cells to enhance the gain and bandwidth performance. This technique provides TIAs with ultra-broad bandwidth.

performance optical receiver systems. Fully integrated MMIC TIAs implemented using high performance processes, such as GaAs-based or SiGe devices, were reported [1]-[5]. Recently, the CMOS chips are more popular due to the improvement of the RF performance, integration capability with baseband circuits, and low cost.

A TIA using common gate topology in an 80-nm CMOS process achieved 45-dB Ω transimpedance gain and 19-GHz bandwidth [6]. Using a 0.18- μm CMOS process, a fully differential TIA demonstrated a transimpedance gain of 62 dB Ω , with 9 GHz bandwidth [7]. Using multi-pole bandwidth enhancement technique in a 0.18- μm BiCMOS process, a CMOS TIA demonstrated a gain of 54 dB Ω with 9.2-GHz bandwidth [8]. The operating frequencies of the previously published CMOS TIAs are all below than 10 GHz or insufficient gain and gain flatness across the band.

I. INTRODUCTION

Advancement in multimedia applications, which require data links with ever-increasing systems capacity, is necessitating high-speed optical communication systems. A trans-impedance amplifier (TIA) is located at the front-end of optical-electric conversion and is a key component in high

Technology	Bandwidth (GHz)	Transimpedance Gain (dB Ω)	TZ-BWP (Ω -THz)	I_{noise} (pA/ $\sqrt{\text{Hz}}$)	Power Dissipation (mW)	Ref.
InP HBT	60	71	216	15 - 20	797	[1]
0.15 μm MHEMT	50	66	100	-	350	[2]
0.15 μm InP HEMT	49	62	62	-	520	[3]
SiGe HBT	50	49	14	10 - 22	-	[4]
0.18 μm SiGe BiCMOS	46	47	10	18 - 30	300	[5]
80nm CMOS	19	45	3.4	-	6.5	[6]
0.18 μm CMOS	9	62	11	-	108	[7]
0.18 μm CMOS*	9.2	54	4.6	-	138	[8]
0.18 μm CMOS	15	58	12	8 - 16	200	This work
0.18 μm CMOS	30	48	7.5	12 - 20	50	This work

Table 1. Recently reported performance of fully integrated MMIC TIAs for optical applications. *: CMOS TIA in BiCMOS process. I_{noise} : input-referred current noise.

This paper presents two broadband TIAs using a standard 0.18- μm CMOS technology for optical applications. The first TIA utilizing two three-stage cascode distributed amplifiers achieves a transimpedance gain of 58 dB Ω and 15-GHz bandwidth. To overcome the low gain nature of the distributed topology, two cascode distributed amplifiers were cascaded design to achieve enough gain and a source follower dc-coupling stage is used to extend the gain performance to dc, which could get rid of using a large capacitor. The other using a cascode distributed amplifier achieves a transimpedance gain of 48 dB Ω and 30-GHz bandwidth. The cascode distributed topology is adopted to achieve sufficient bandwidth and gain flatness. Table 1 summarizes the recently reported performance of CMOS TIAs compared with this work. Our chips demonstrated the highest transimpedance-bandwidth product among the reported CMOS TIAs.

II. 15-GHz TIA WITH 58-dB Ω TRANSIMPEDANCE GAIN

The performance of a conventional lumped-element designed transimpedance circuit is limited by the characteristics of the active device because they use a simple feedback circuit. It is thus difficult to achieve an over-10-GHz bandwidth with a flat gain. One way to overcome this problem is to use a distributed amplifier in the gain stage of the TIA to achieve wider bandwidth. The gain-bandwidth product of distributed amplifiers substantially exceeds the transistor unit-gain frequency f_T because the input and output capacitances of the active devices can be absorbed in the distributed structures. However, the gain of the available CMOS distributed amplifiers has been limited to less than 10 dB.

To achieve high gain with wide bandwidth, two low-gain wideband distributed amplifiers could be cascaded to implement a high-gain wideband TIA. However, for a high gain-bandwidth performance, cascode gain cells are frequently used and will lead to dc level mismatch in the interstage connection. A blocking capacitor is usually used in the RF design but will decrease the broadband performance, especially in the very low frequency. On the other

hand, a source-follower level shift circuit is usually used in the analog circuit but exhibits poor gain in several tens of GHz. The blocking capacitor and the source follower circuit are combined in our interstage circuit design to keep the broadband performance to dc without degrading the high frequency performance.

The schematic of the proposed CMOS TIA is shown in Fig. 1. It consists of two three-stage distributed amplifiers to achieve high gain and broad bandwidth, and a broadband coupling circuit used to couple the signal down to dc. The broadband coupling circuit combines the blocking capacitor and the source follower circuit with the current source.

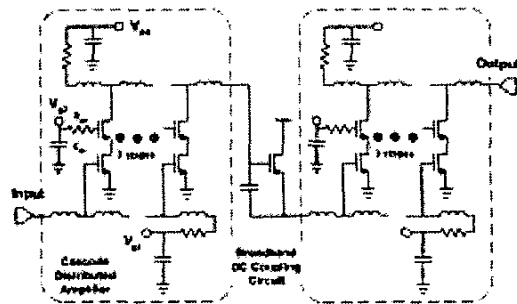


Fig. 1. The schematic of the 15-GHz CMOS TIA with 58-dB transimpedance gain.

Additionally, the cascode configuration is used to improve the gain-bandwidth product of the distributed amplifier. Conventional cascode FETs suffer from a large feedback capacitance, the drain-source capacitance of the common-gate transistor. This makes it unstable and thus more difficult to use in an amplifier circuit than a common-source FET. Since the stability is an important issue in an amplifier design, a small damping resistor R_{gx} is usually added in the gate of common-gate transistor to improve the amplifier stability.

To reduce the size of the inductor and the coupling effect between the spiral inductor, the spiral inductors were enclosed by the ground of CPW. To prevent unexpected stability problems and noise, all blank area was covered with fully connected ground. The S-parameters of the inductors were simulated by the full-wave EM simulation tool. The models of the

capacitors and resistors were provided by the foundry. The MIM capacitor gives Q of 100 and 40 at 2.4 GHz and 5.3 GHz respectively at 1.1 pF. The cascode devices employ a 20- Ω damping resistor. A die micrograph is shown in Fig. 2. The chip size is approximately 2.0 x 1.0 mm² including testing pads.

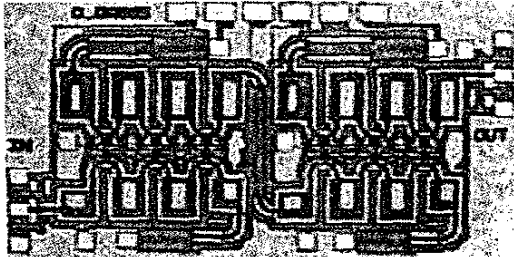


Fig. 2. Microphotograph of the 15-GHz CMOS TIA.

The CMOS TIA was tested via on-wafer probing. Fig. 3 shows the measured noise figure, input/output return losses and calculated transimpedance gain from S-parameters. The measure power gain is 18 dB. The mean calculated transimpedance gain from S-parameters is 58 dB Ω . The worse-case input return loss has a value 11 dB at 4 GHz and remains better than 12 dB from dc to 15 GHz. The output return loss is 9 dB or better than 12 dB over most of the bandwidth. The reverse isolation is 38 dB or better over the entire bandwidth as well. The measured results agree with the simulated results very well. The noise figure is between 3.7 and 6 dB over the interested bandwidth and this corresponds to an input-referred current noise is between 8 and 16 pA/ $\sqrt{\text{Hz}}$.

III. DISTRIBUTED TIA WITH 30-GHZ BANDWIDTH

A one-stage distributed TIA with 2 gain cells has also been designed. Each gain cell contains a cascode device, a 10- Ω damping resistor to stabilize the common-gate device and a bypass capacitor. This amplifier is dc-coupled at the input and output. Fig. 4 shows the circuit schematic. The microphotograph is shown in Fig. 5. The chip size is 0.8 x 1.3 mm² including testing pads.

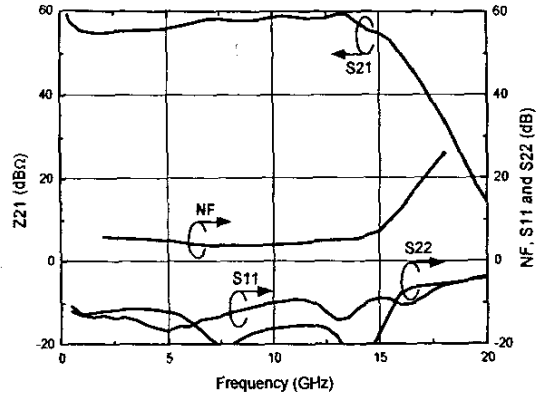


Fig. 3. Measured transimpedance gain, input/output return loss and noise figure of the 15-GHz CMOS TIA.

The CMOS TIA was tested via on-wafer probing. Fig. 6 shows the measured input/output return losses, noise figure and calculated transimpedance gain from S-parameters. The bias condition for this measurement is 28 mA at 1.8 V. The measured power gain is 8 dB. The mean calculated transimpedance gain is about 48 dB Ω with 30-GHz bandwidth. Up to 15 GHz the measured output return loss is better than 12 dB. The measured noise figure is between 5.5 and 7.5 dB from 1 to 18 GHz. To our knowledge, this chip demonstrated the highest frequency and bandwidth of operation for a CMOS TIA. The calculated input-referred current noise from the measured noise figure is between 12 and 20 pA/ $\sqrt{\text{Hz}}$ from 1 to 18 GHz.

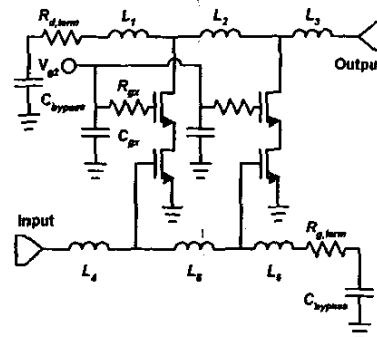


Fig. 4. Circuit schematic of the 30-GHz CMOS distributed TIA.

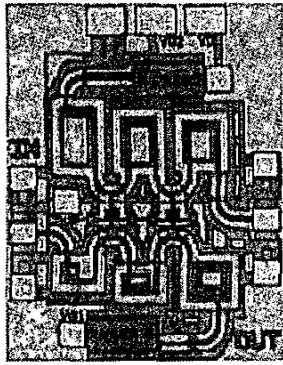


Fig. 5. Microphotograph of the 30-GHz CMOS distributed TIA.

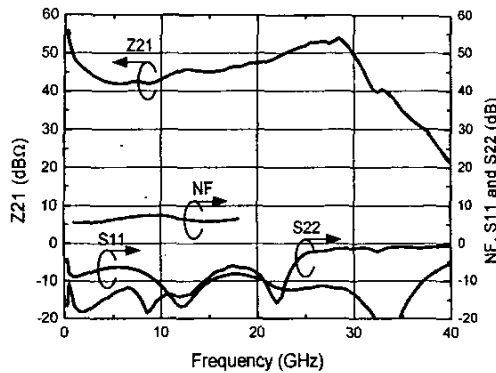


Fig. 6. Measured input/output return loss, noise figure and calculated transimpedance gain from S-parameters for the 30-GHz CMOS TIA.

IV. CONCLUSION

Two fully integrated CMOS TIAs have been designed, fabricated and tested. The first CMOS TIA demonstrates a transimpedance gain of 58-dB Ω with 15-GHz bandwidth, which is believed to be the highest transimpedance-bandwidth product among the reported CMOS TIAs. The second CMOS TIA achieves 48-dB Ω transimpedance gain and 30-GHz bandwidth and has the widest bandwidth of operation.

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