Single-stage resonant converter with power factor correction

R.-T. Chen and Y.-Y. Chen

Abstract: A novel single-stage resonant converter with power factor correction is presented. Most of the researched power factor corrected rectifiers cascade a boost-type converter with the system. It is found that the half-bridge resonant converter, when the duty cycles are greater than 50%, can simplify the front end of the boost-type converter to a novel single-stage converter. To reduce the converter size and weight and to achieve ripple-free input current, coupled inductor techniques are used in the proposed converter. The operation principle and system steady analysis of the adopted converter are discussed in detail. A prototype has been built to demonstrate the system performance.

1 Introduction

In most resonant power supplies, the DC–DC converters are driven by equivalent DC voltage sources obtained from a rectifying circuit connected to the AC mains, as shown in Fig. 1. Because the rectified current only draws power in a small time interval, it results in a poor input power factor. To improve the power factor and reduce the harmonic components of the input current, active power factor correction circuits can be used. In most cases, the active power factor correction circuit employs a boost converter, as shown in Fig. 2*a*. To reduce the overall size and cost, researchers attempted to integrate the functions of power factor correction (PFC) and resonant converter, into a single power stage. In recent years, a number of single-stage input current shaping converters have been introduced [1–7]. The major disadvantages of the conventional two-stage conversion approach are the added cost, stress and the complexity of the two-control loop, two-power-stage nature. Single-stage PFC converters that integrate the two power stages into one, thus reducing significantly the component count and cost, have gained much attention in many low-power applications during the past ten years.

Figure 2*a* shows the pre-regulated boost converter with a half-bridge resonant converter. The two converters are controlled independently to achieve power factor correction and voltage regulation. The duty cycles of the switches S_1, S_2, and S_3 are 50%, 50%, and D_b respectively. The duty ratio D_b may be larger or less than 50%. Figure 2*b* shows the switching sequence of the three main switches. Thus, with a proper control circuit design, the input current can be regulated to have a sinusoidal waveform and to be in phase with the input voltage. Consequently, high power factor can be obtained from these converters.

An application of the zero-ripple technique to the converter structure is described in [8]. In this paper, the zero-ripple technique is applied to the proposed resonant converter. For basic consideration, it seems to be that only by extending a basic converter structure by a well defined magnetic coupling of the input and filter inductors can a complete elimination of the input current ripple be obtained. It is shown that the ripple suppression can be achieved only on the input side or on the output side. A circuit consisting of passive elements cannot have an infinitely high effective input inductance for all frequencies. The impossibility of a complete suppression of the input current ripple of the converter becomes clearly understandable. Therefore, the system should be called 'better low-ripple boost converter' and not 'zero-ripple boost converter'. In addition, coupled inductor techniques supply a method to reduce the converter size and weight and to achieve ripple-free current. A prototype has been built to demonstrate the theoretical prediction.

In this paper, we propose a novel single-stage resonant converter with power factor correction. One major disadvantage of such power factor correction circuits is that the switching frequency is limited because of the switching loss. Since the switching loss in resonant converters can be minimised, the disadvantage is overcome.

2 Circuit configuration

To explain clearly the proposed resonant converter, we first want to consider the circuit configuration in the following.

2.1 Single-stage resonant converter

There are several interesting state-of-the-art single-stage solutions [1–5]. Single stage solutions supply the load with a constant and fast-regulated DC voltage, while in most cases the line current is not sinusoidal. The pulsed current deteriorates the line voltage, produces radiated and conducted electromagnetic interference, and leads to poor utilisation of the capacity of the power sources. For single-phase electronics applications, passive power filters, active one- and two-stage PFC rectifiers are typical approaches used to achieve high power factor and low total harmonic distortion (THD). Compared with the two-stage approach, many

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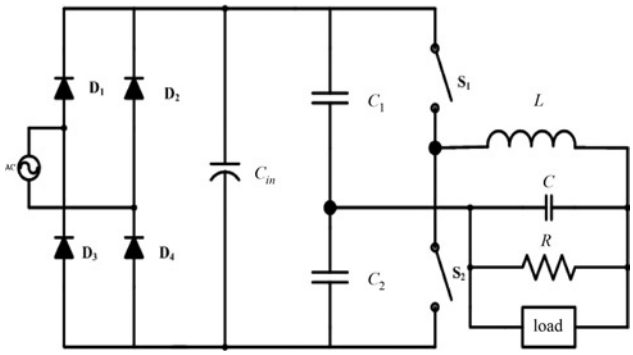

Fig. 1 *Conventional AC–DC rectifying circuit, which drives a half-bridge resonant converter*

strategies have been developed to reduce the size and the cost and to improve the efficiency.

In this paper, an improved boost-derived resonant converter is proposed, as shown in Fig. 3*a*. It is found that the resonant converter, when the duty cycles are greater than 50%, can operate in an interesting condition. Therefore, it acts as a combination of the front end of the boost-type converter and a novel single-stage converter. If the duty cycles of S_1 and S_2 are made variable and always greater than 50%, and it can be eliminated as shown in Fig. 3*a*; (i.e. if S_1 and S_2 have overlapping conduction interval) then S_3 is no longer needed. Figure 3*b* shows the switching sequences of the two main switches and a pseudo switch S_3'. As a result, the proposed single-stage resonant converter, as shown in Figure 4*a* integrates a ripple-free input current shaper and a half-bridge resonant converter with two shared switches and controllers. One of the advantages of the overlapping primary switch conduction is the equal division of inductor current between S_1 and S_2, thus reducing the switch stress and improving conversion efficiency. The proposed resonant converter in Fig. 4*a* with the duty cycles greater than 50% is a suitable approach for ripple-free input current. Fig. 4*b* shows the main typical waveforms of the converter in a switching cycle. This will be verified in the following Sections.

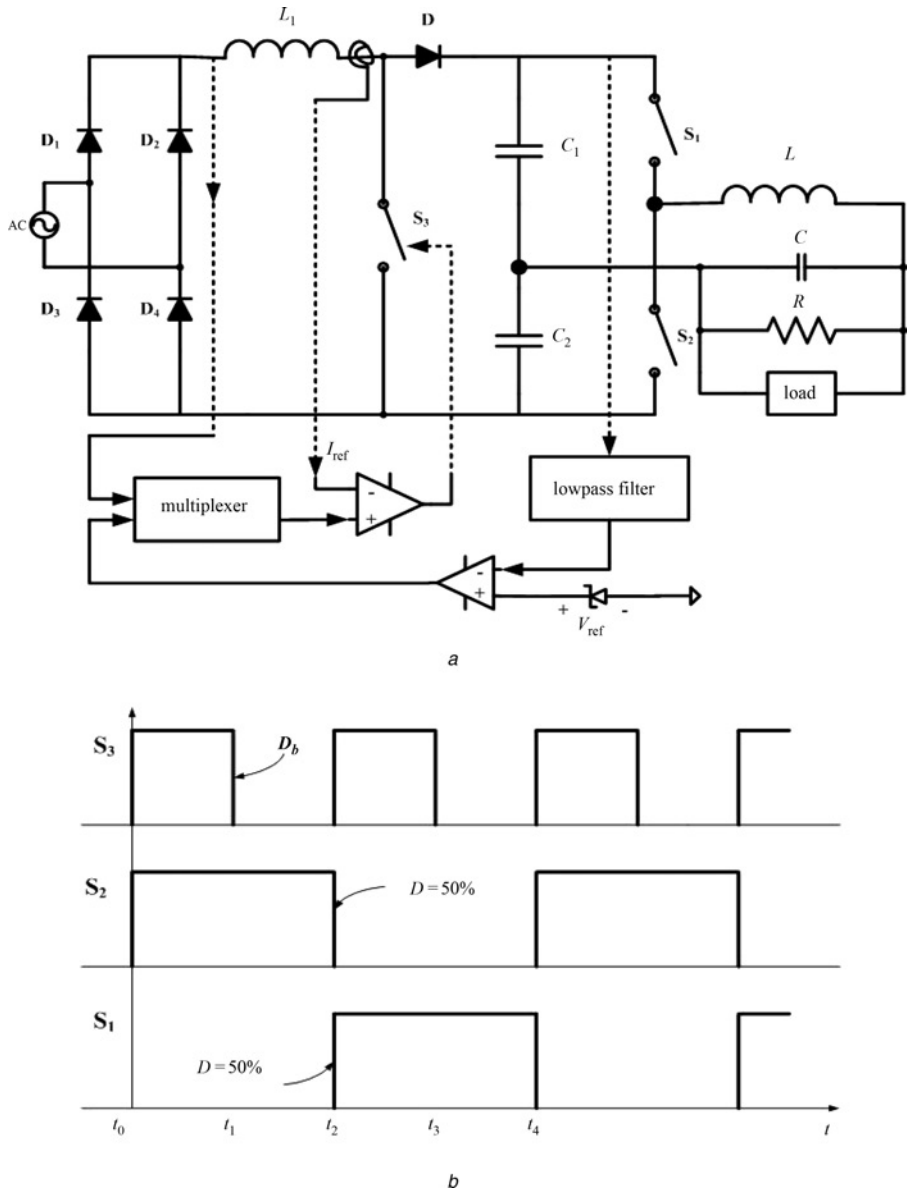

Fig. 2 *Pre-regulated resonant converter*

a Power circuit
b Switching sequences with S_1 and S_2 duty ratio equal to 50%

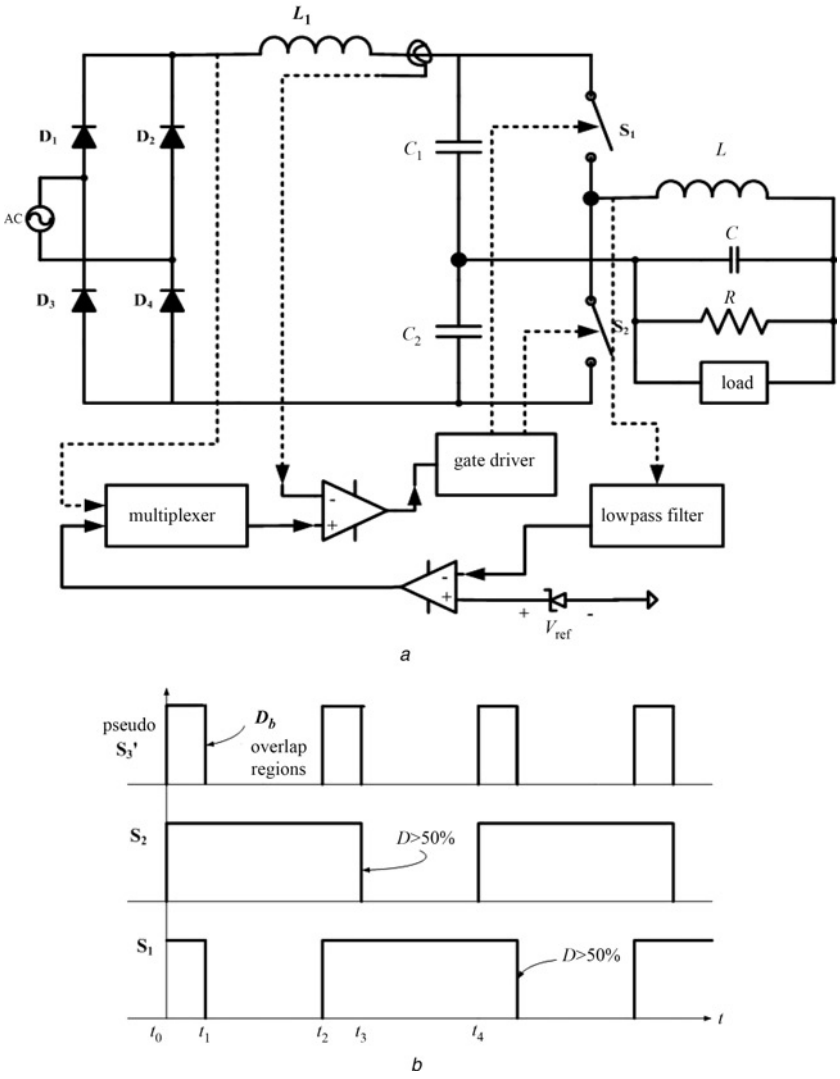

Fig. 3 *Improved half-bridge resonant converter*

a Power circuit
b Switching sequences with S_1 and S_2 duty ratio greater than 50%

2.2 Ripple-free input current shaper

To explain the effect called zero-ripple phenomenon in Fig. 4*a* [8], we want to consider briefly the relationships given for magnetic coupling of the two ports networks shown in Fig. 4*a*, the nodes of which are indicated by ①, ②, and ③. The two-port network is part of Fig. 4(*a*), the equivalent circuit of which is represented by an ideal transformer $(N_1 : N_2)$ and a mutual inductance L_M, where $L_M = \sqrt{(L_1 L_2)}$ under ideal conditions. The elimination of the ideal transformer results in the simple model by transformation from primary to secondary side. The secondary equivalent inductance is $(N_2/N_1)^2 L_M$. The following mathematical derivation is used to analyse the ripple cancellation [8].

Let us now make the assumption that it is possible to reduce the value of i_{in} to zero in our model, as shown in Fig. 4*a*; and let us examine the circuit currents and voltages that result from our assumption. If i_{in} is zero, then the AC voltage drop across L_1 must also be zero, as illustrated in Fig. 4*a*. The voltage appearing across L_M must therefore be equal to that of the secondary voltage source, $(N_2/N_1)V_{in}$, reflected through the ideal transformer in the model. Also, the current through L_2 and L_M must be equal to that produced by the secondary voltage, V_{L2}. These conditions lead to the two-port circuit of Fig. 4*a*, where

$$\frac{N_2}{N_1} V_{L1} = \left(\frac{N_2}{N_1}\right)^2 L_M \frac{\mathrm{d}\, i_r}{\mathrm{d}t} \tag{1}$$

$$V_{L2} + V_{L_{ex}} = L_{ex} \frac{\mathrm{d}\, i_r}{\mathrm{d}t} + \left(\frac{N_2}{N_1}\right) L_M \frac{\mathrm{d}\, i_r}{\mathrm{d}t} \tag{2}$$

where i_r is the current through ripple capacitor C_r and L_{ex} is the external trimming inductor, which is in series with L_2.

Combining (1) and (2) by the elimination of the common $\mathrm{d}\, i_r/\mathrm{d}t$ factor gives

$$L_{ex} = \left(\frac{N_2}{N_1}\right) L_M \left(\frac{V_{L2} + V_{L_{ex}}}{V_{L1}} - \frac{N_2}{N_1}\right) \tag{3}$$

The relationship between secondary leakage inductance and that of the core material set by (3) is important and worth dwelling on for a moment. First, recall that this equation was derived based on the premise that no input ripple current existed in our model and, if satisfied, must produce this condition. It is known that there are several advantages to having L_1 and L_2 wound on the same core. One viable method is to wind primary and secondary turns together tightly to reduce the leakage inductance of

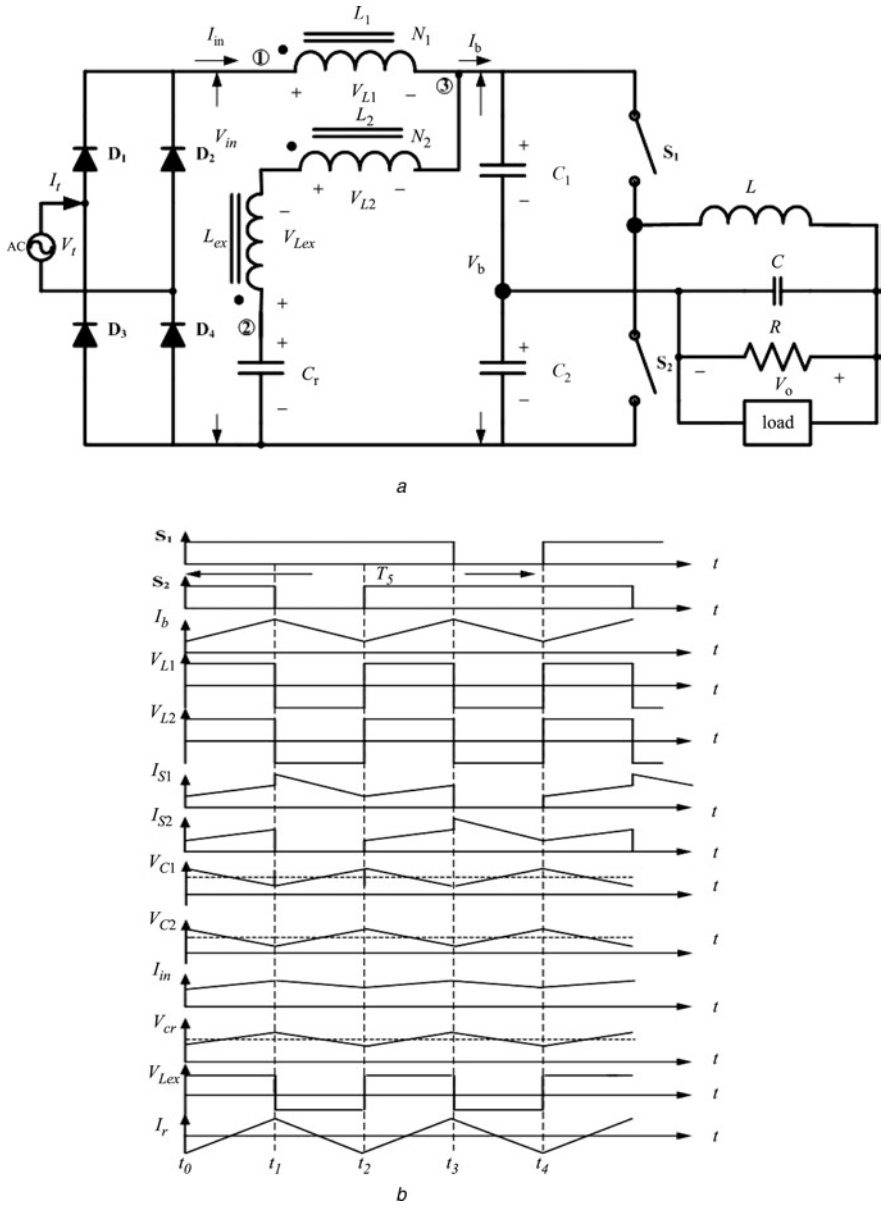

Fig. 4 *Proposed half-bridge resonant converter*

a Power circuits
b Theoretical waveforms

L_1 and L_2 to essentially zero, and then insert a small external trimming inductor in series with the secondary sides to emulate the desired value of L_{ex}.

The initially analysed basic principle of ripple elimination can now be applied to the proposed resonant converter. A coupling capacitor C_r has to be provided in order to suppress the occurrence of a DC voltage component across L_2. If the capacitance C_r is selected sufficiently large, identical voltages across L_1 and L_2 will result. The zero-ripple phenomenon will be obtained only for the theoretical limiting $C_r \rightarrow \infty$. Therefore, the assumptions mentioned in Fig. 4*a* are present for suppressing the ripple of the input current i_1 by proper choice of L_{ex}. For a practical system realisation a capacitance value C_r as small as possible is desired to minimise size and weight of the converter. The average value V_{Cr} of the coupling capacitor is equal to the input voltages in the stationary case. That is, $V_{Cr} = V_{\text{in}}$. Then, it follows that, for a small finite ripple of the input current, $\Delta i_{\text{in}} \simeq \Delta v_{cr}\ T_s/2\pi(L_1 - L_M)$. It acts like a lowpass filter lying at the converter input.

It should be pointed out that the lowpass filter is already an integral part of the basic converter structure. Thus, it does not have to be realised by additional power components; however, C_r for the conventional boost converter acts as an essential element of the energy transfer between the input and output sides. Therefore, the current stress on C_r is basically different from that of a conventional filter capacitor. A circuit consisting of passive elements L_1, L_2 and C_r cannot have an infinitely high effective input inductance for all frequencies. Thus, a complete suppression of the input current ripple is impossible. The system shown in Fig. 4*a* should be called 'better low-ripple converter' and not 'zero-ripple converter'.

As a result, the inductances L_1 and L_2 have the same voltage waveforms during the whole cycle. It is possible to couple them and to achieve a reduced component count, reducing the amount of material, increasing the energy density, and achieving ripple-free input current [8]. The voltage relationships of Fig. 4, along with the right choice of leakage inductances (L_{ex}) associated with the inductor windings, are the key factors in achieving

zero-ripple current at the input of the proposed resonant converter.

3 Operation principles

In boost-derived resonant converters, as shown in Fig. 4*a*, switch duty cycle (D) is greater than 50% and a separate drive circuit will be necessary for each DC isolated switch element. Twice during each switching cycle T_s, the two main switches are ON simultaneously. At the beginning of a switching cycle, $S_1$and S_2 are ON. Inductor current therefore flows through S_1 and S_2. When S_2 turns OFF and switch S_1 closes, it now allows the inductor current to flow through the capacitors of C_1, C_2 and to deliver its stored energy to the resonant tank. In the proposed converter the capacitor divider is viewed as constant voltage source because the two capacitances are much larger than the resonant tank. The divider capacitor voltage is equal to one-half the input voltage V_{in}. When switch S_1 turns OFF and switch S_2 is ON, the operation principle is symmetrical on the former situation. In addition, a two-port magnetic coupling cell is used for the input filter. L_{ex} is small leakage inductance of the coupled inductor. C_r is used for the clamp capacitor. The AC output load is direct parallel to resonant capacitor C. The load is a linear ultrasonic motor in this paper.

The principle of operation in steady-state condition is described with the following assumptions

(i) All the switches and components are ideal.
(ii) The converter is operated in the continuous conduction mode.
(iii) Inductances L_1 and L_2 are tightly coupled to each other.
(iv) The resonant period by the clamp capacitance C_r and coupled inductance L_2 is greater than the turn-off time of the main switch.

The switching sequences and theoretical waveforms of the proposed converter are shown in Fig. 4*b*. S_1 and S_2 are driven complementary with an overlap interval. The output voltage can be regulated by varying this controllable interval as PWM with a constant switching frequency. According to the voltage–second balance, the inductor L_1 works in one switching cycle (T_s) as shown in Fig. 4*b*. We can derive

$$V_{in}\left(D-\frac{1}{2}\right)T_s=(V_b-V_{in})(1-D)T_s \tag{4}$$

where D is the duty ratio, V_{in} is the rectified line voltage and V_b is the input voltage of the half-bridge resonant stage.

Thus, the following voltage gain can be derived

$$\frac{V_b}{V_{in}}=\frac{1}{2(1-D)} \tag{5}$$

The source voltage V_g of the resonant tank is divided from the input voltage V_b of the half-bridge resonant converter, that is

$$V_g=\frac{V_{in}}{4(1-D)} \tag{6}$$

From the switching sequences and theoretical waveforms shown in Fig. 4*b*, there are four modes of operation interval in one switching period [9–11]. Figure 5 shows equivalent circuits for each stage of the proposed converter.

(*a*) Mode 1 $[t_0 \le t < t_1$; Fig. 5*a*]

In this stage with switches S_1 and S_2 ON as shown in Fig. 5*a*, the inductor L_1 is grounded. The input current I_{in} is increased, resulting in energy stored in L_1. The current through L_2, I_r is increasing and then resonant with C_r. The voltage across inductor L_1 is the input voltage, V_{in}, and the voltage across coupled inductor L_2 is $V_{Cr}=V_{in}$. In this stage the input voltage of the resonant tank, V_g, is shorted by the switches S_1 and S_2 being ON at the same time. Thus, the sources of the resonant tank are the initial value of the inductor, $I_L(t_0)$, and capacitor, $V_c(t_0)$. This stage is ended when main switch S_2 is turned off at time $t=t_1$.

The output load is supplied by the resonant capacitor. The resonant voltage v_c and current i_L at the resonant tank can be expressed as

$$v_c(t)=(-1)(V_c(t_0)\cos\omega t+\sqrt{\frac{L}{C}}I_L(t_0)\sin\omega t) \tag{7}$$

$$i_L(t)=(-1)\sqrt{\frac{C}{L}}V_c(t_0)\sin\omega t+I_L(t_0)\cos\omega t \tag{8}$$

where the resonant angular frequency ω and characteristic

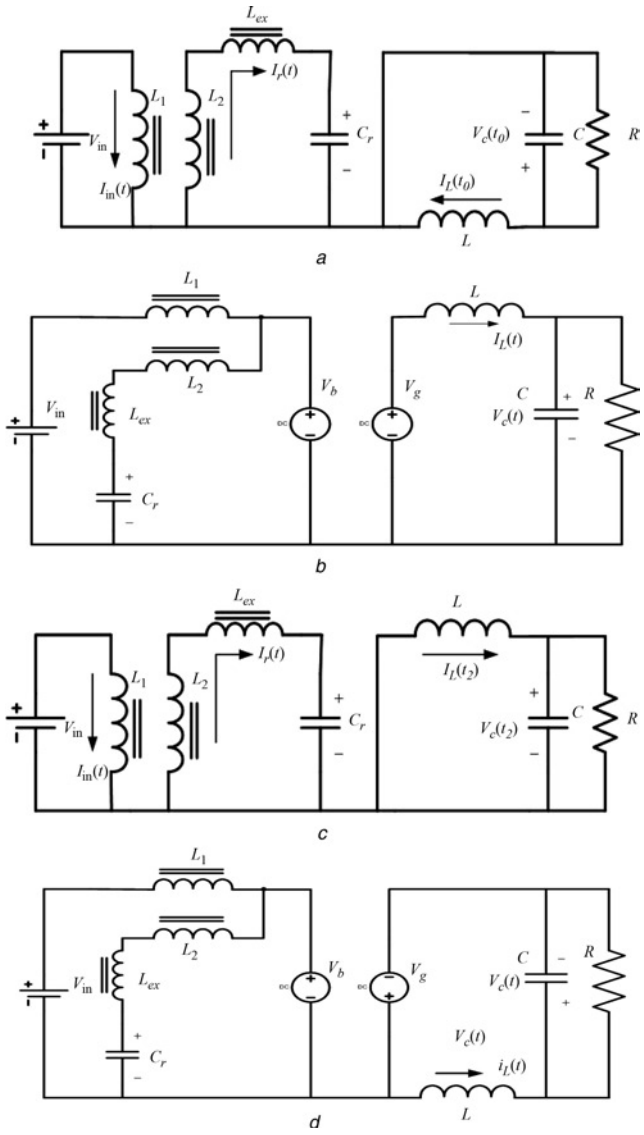

Fig. 5 Principle of operation circuits
a Mode 1
b Mode 2
c Mode 3
d Mode 4

impedance Z are given by

$$\omega = \frac{1}{\sqrt{LC}}, \quad Z = \sqrt{\frac{L}{C}} \tag{9}$$

(*b*) Mode 2 [$t_1 \le t < t_2$; Fig. 5(*b*)]
This stage starts when the main switch S_2 is turned off. In this stage the switch S_1 is still turned on. With switch S_1 ON and S_2 OFF, as shown in Fig. 5*b*, in this situation the energy stored in L_1 releases to the conventional half-bridge converter. The current I_r is still keeping its positive direction; however, it is decreasing. The capacitor C_r is charged by I_r. The voltage across inductor L_1 is $(V_{\text{in}} - V_b)$. The voltage across inductor L_2 should be $(V_{cr} - V_b)$. That is also equal to $(V_{\text{in}} - V_b)$.

The capacitances C_1, C_2 are large enough to be considered as a constant voltage source in this stage. Therefore the resonant source, V_g, is one-half the voltage V_b. The resonant voltage and resonant current in this stage can be expressed as

$$v_c(t) = V_g + \sqrt{\frac{L}{C}} I_L(t_1) \sin \omega t + (V_c(t_1) - V_g) \cos \omega t \tag{10}$$

$$i_L(t) = I_L(t_1) \cos \omega t + \sqrt{\frac{C}{L}} (V_g - V_c(t_1) \sin \omega t \tag{11}$$

where $I_L(t_1)$ is the resonant inductor current and $V_c(t_1)$ is the resonant capacitor voltage at time $t = t_1$.

(c) Mode 3 [$t_2 \le t < t_3$; Fig. 5*c*]
At time $t = t_2$ the switch S_2 is turned on. With switches S_1 and S_2 ON, as shown in Fig. 5*c*, the equivalent circuits are almost the same as in Mode 1. The system analysis in this stage is the same as the discussion for Mode 1 except that the initial value is in a different direction. Similarly, we can derive that

$$v_c(t) = V_c(t_2) \cos \omega t + \sqrt{\frac{L}{C}} I_L(t_2) \sin \omega t \tag{12}$$

$$i_L(t) = \sqrt{\frac{C}{L}} V_c(t_2) \sin \omega t + I_L(t_2) \cos \omega t \tag{13}$$

where $I_L(t_2)$ is the resonant inductor current and $V_c(t_2)$ is the resonant capacitor voltage at time $t = t_2$.

(d) Mode 4 [$t_3 \le t < t_4$; Fig. 5*d*]
At time $t = t_3$ the switch S_1 is turned off. In this stage the switch S_2 still turns on. With switch S_1 OFF and S_2 ON as shown in Fig. 5*d*, I_{in} releases the energy stored in L_1 to the half-bridge resonant converter. The converter action operates completely opposite to Mode 2 condition. In this stage the resonant tanks are expressed as

$$v_c(t) = V_g - \sqrt{\frac{L}{C}} I_L(t_3) \sin \omega t - (V_g + V_c(t_3)) \cos \omega t \tag{14}$$

$$i_L(t) = -I_L(t_3) \cos \omega t + \sqrt{\frac{C}{L}} (V_g + V_c(t_3) \sin \omega t \tag{15}$$

where $I_L(t_3)$ is the resonant inductor current and $V_c(t_3)$ is the resonant capacitor voltage at time $t = t_3$.

From the previous analysis the component stress can be derived as

$$V_{peak} = V_g + \sqrt{\frac{L}{C} I_L^2(t_1) + (V_c(t_1) - V_g)^2} \tag{16}$$

current stress

$$I_{peak} = \sqrt{I_L^2(t_1) + \frac{C}{L} (V_g - V_c(t_1))^2} \tag{17}$$

The operation principle and mathematical analysis will be used to design the proposed converter later.

4 Design considerations

The previous Section provides the detailed analysis of the proposed converter under steady-state conditions. In this Section, we will discuss the design considerations of the circuit.

4.1 Control circuit configuration

The control circuit has to perform the following two operations: (*a*) It must force the input current I_{in} to equal $k \times V_{\text{in}}(t)$, where k is a constant, in order to maintain a unity power factor; and (*b*) It must change k in response to line and load changes. In the proposed resonant converters, these can be done by changing the switching frequency to force I_{in} to follow the reference current I_{ref}, which is equal to $k \times V_{\text{in}}(t)$.

Figure 6 shows the control circuit block diagram with half-bridge resonant converter and describes the principle of operation. As stated before, the existing of an overlapping time interval is necessary to ensure zero current switching. In the control circuit given in Fig. 6, the overlapping time interval is realised by the monostable flip–flops. The T flip–flop is used to remember which switch was turned on previously. When I_{in} reaches I_{ref}, the T flip–flop is triggered by the current comparator and its outputs change their logic levels. The NAND gates are used for time delay to ensure the proper operation of the logic circuit. The feedback voltage is derived from the output voltage V_o by way of a precision rectifier circuit and a lowpass filter. It compares to the reference voltage V_{ref} at the differential amplifier, and then forces I_{in} to follow the reference current I_{ref}. It must change k in response to line and load changes. This will be derived in next Section.

4.2 Determination of input inductor and capacitor values

It can be shown from Fig. 5 that during circuit mode M_1 and M_3, the voltage source V_g is short-circuited. Thus the input current I_{in} is linearly changed upwards by the input voltage $V_{\text{in}}(t)$, as follows

$$L_1 \frac{dI_{\text{in}}}{dt} = V_{\text{in}}(t) = V_p |\sin \omega_{\text{in}} t| \tag{18}$$

where V_p is the peak value of input voltage $V_{\text{in}}(t)$.

Since the switching frequency is much greater than the line angular frequency ω_{in}, $V_{\text{in}}(t)$ can be considered as constant within the time interval $[t_0, t_1]$. Thus

$$\Delta I_{\text{in}} = I_{\text{in}}(t_1) - I_{\text{in}}(t_0) = \frac{V_p}{L_1} |\sin \omega_{\text{in}} t| \times (t_1 - t_0) \tag{19}$$

where $t_1 - t_0 = (D - 1/2)T_s$.

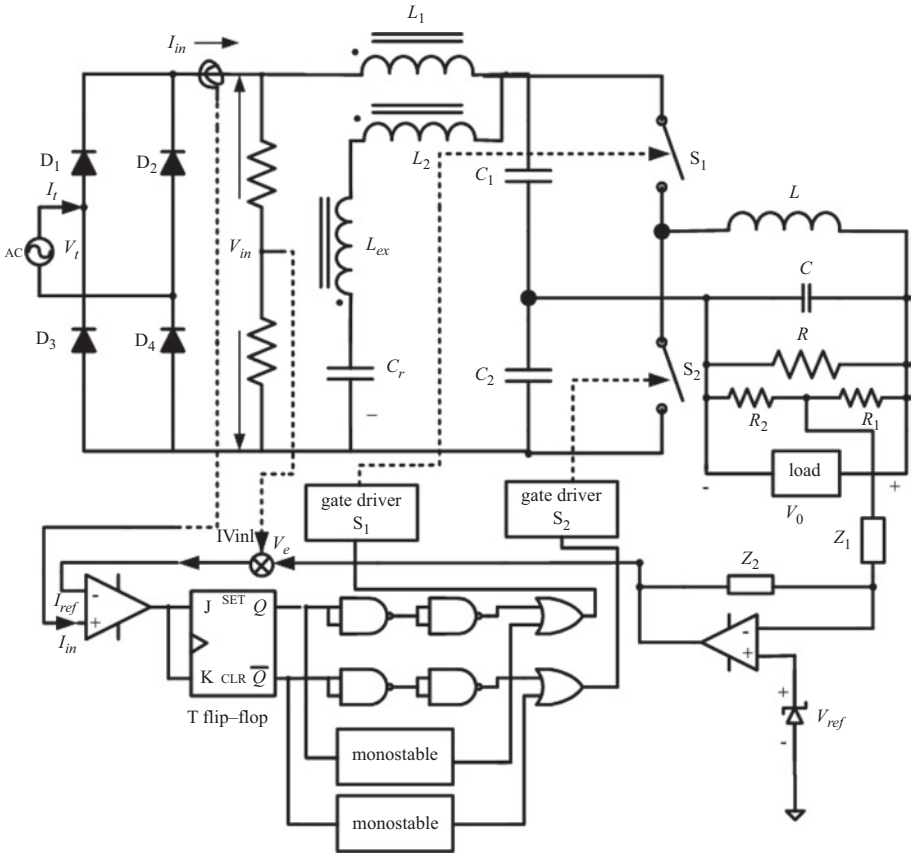

Fig. 6 *Control circuit block diagram used in half-bridge resonant converter*

Then the maximum value of ΔI_{in}, $\Delta I_{\text{in, max}}$ appears when $\omega_{\text{in}}t = \pi/2$. Therefore, we have

$$\Delta I_{\text{in,max}} = \frac{V_p}{L_1}\left(D - \frac{1}{2}\right)T_s = \frac{(D-1/2)V_p}{L_1 f_s} \tag{20}$$

where f_s is the switching frequency.

For a given $\Delta_{I_{\text{in, max}}}$, the input inductor L_1 can be calculated as follows

$$L_1 = \frac{(D-1/2)V_p}{f_s \Delta I_{\text{in,max}}} \tag{21}$$

since inductance L_1 and L_2 are tightly coupled with each other, that is $L_1 = L_2$.

From Fig. 4 the clamp capacitor and coupling inductor are resonant about one-half the resonant period. Therefore half the resonant period is approximately equal to the turn-off time of the main switch, that is

$$\pi\sqrt{(L_2 + L_{ex})C_r} = \left(D - \frac{1}{2}\right)T_s \tag{22}$$

Thus the clamp capacitance can be obtained as

$$C_r = \frac{[(D-1/2)T_s}{\pi^2(L_2 + L_{ex})} \tag{23}$$

where L_{ex} is the external trimming inductance, obtained from (3).

4.3 Determination of reference current and error voltage

Fig. 7 shows the waveforms of input current I_{in} and reference current I_{ref}. It is evident from Fig. 7 that

$$I_{\text{in. max}} = I_p + \Delta I_{\text{in,max}} \tag{24}$$

where I_{p} is the amplitude of I_{ref}.

Since the input current ripple ΔI_{in} has a triangular waveform, consideration of power yields

$$P_o = \frac{V_p}{2}\left(I_p + \frac{\Delta I_{\text{in,max}}}{2}\right) \tag{25}$$

where P_o is the output power.

For given values of P_o, $\Delta I_{\text{in, max}}$, and V_p, then I_p, can be determined from

$$I_p = \frac{2P_o}{V_p} - \frac{\Delta I_{\text{in,max}}}{2} = \frac{2P_o}{V_p} - \frac{(D-1/2)V_p}{2L_1 f_s} \tag{26}$$

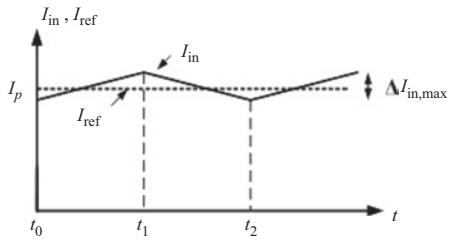

Fig. 7 *Waveforms of input current and reference current*

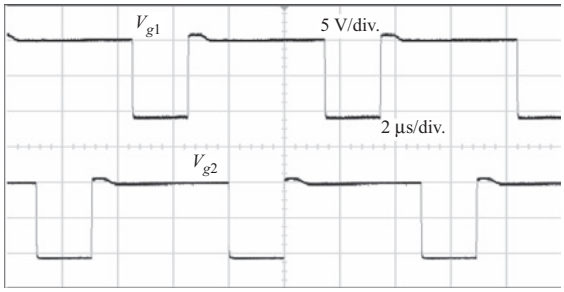

Fig. 8 *Measured switch gate voltage (V_{g1}, V_{g2}) waveforms*

Comparing $I_{\text{ref}} = I_p \sin \omega_{\text{in}} t$ with $k \times V_{\text{in}}(t)$ gives

$$k = \frac{2P_o}{V_p^2} - \frac{\Delta I_{\text{in,max}}}{2V_p} = \frac{2P_o}{V_p^2} - \frac{(D-1/2)}{2L_1 f_s} \tag{27}$$

In the proposed resonant converters, this can be done by changing the switching frequency to force I_{in} to follow the reference current I_{ref}, which is equal to $k \times V_{\text{in}}(t)$.The feedback voltage is derived from the output voltage V_o by way of a precision rectifier circuit and a lowpass filter. Then it compares to the reference voltage V_{ref} at the differential amplifier. The feedback error voltage V_e can be derived as follows

$$V_e = \left(1 + \frac{Z_2}{Z_1}\right) V_{\text{ref}} - \frac{Z_2}{Z_1} K_R V_o \tag{28}$$

where V_{ref} is the reference voltage, $K_R = R_2/(R_1 + R_2)$ is the resistor divider parameter, and Z_1, Z_2 are equivalent transfer functions of the precision rectifier circuit and lowpass filter.

5 Experimental results

The new resonant converter was implemented with the following specifications: nominal output power $P_o = 80$ W; input voltage $V_{\text{in}} = 110$–120 V; switching frequency $f_s = 150$ KHz. The power stage consists of the following

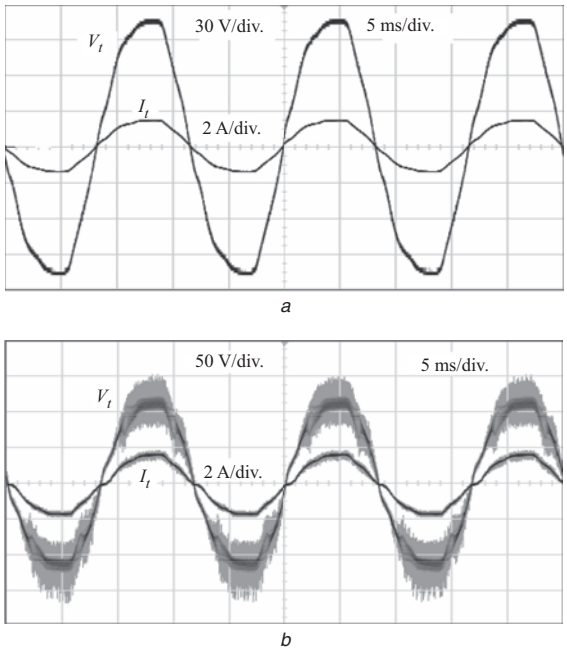

Fig. 9 *Measured input voltage (V_t) and line current (I_t) waveform*

a With input current shaper
b Without input current shaper

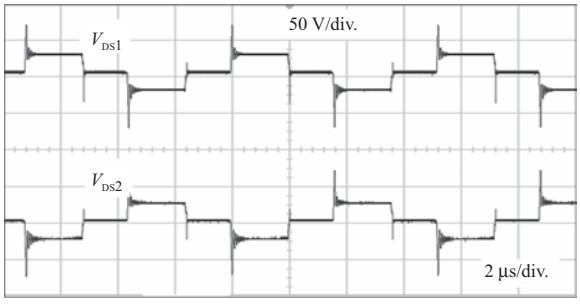

Fig. 10 *Experiment results: voltage across switches S_1 and S_2*

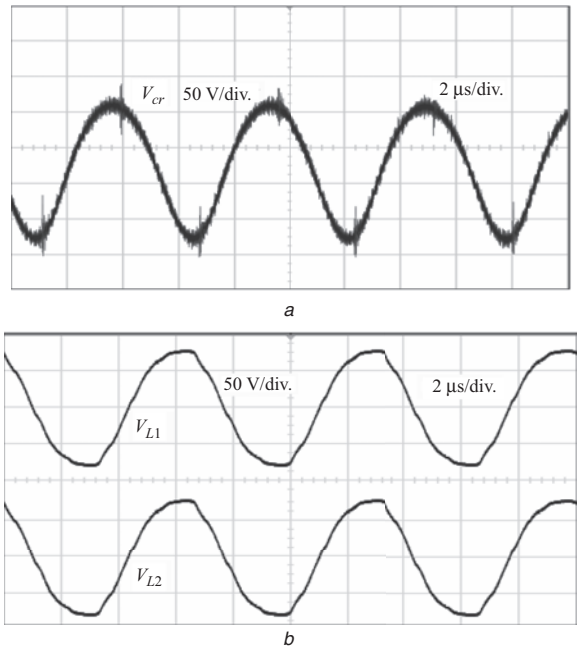

Fig. 11 *Experiment results:*

a Voltage across capacitor C_r.
b Voltage across coupled inductor L_1, L_2

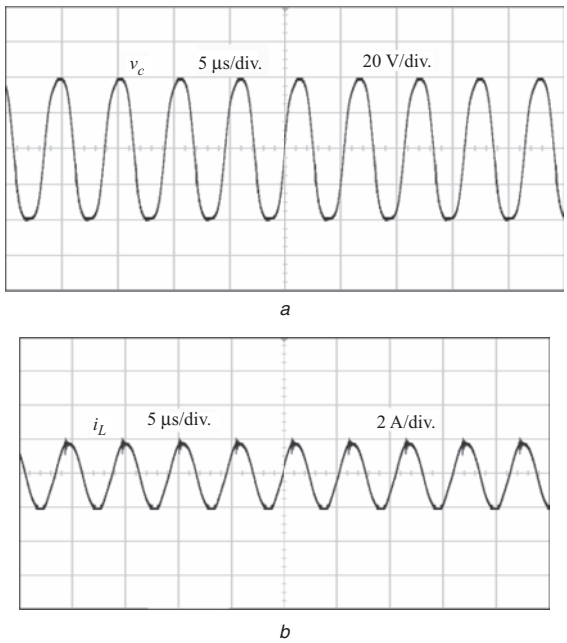

Fig. 12 *Experiment results of resonant tank*

a Resonant capacitor voltage
b Inductor current

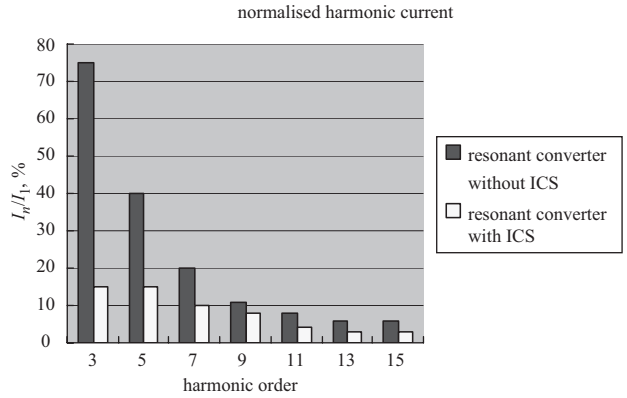

Fig. 13 *Comparison of corresponding line-current harmonics*

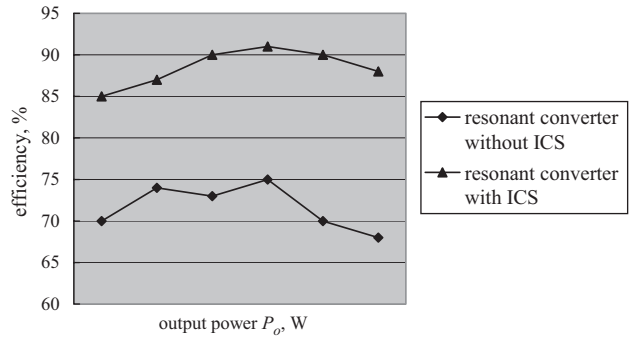

Fig. 14 *Comparison of efficiencies*

parameter: switches S_1 and S_2: power MOSFET's IRF 740; capacitors C_1, C_2: 100 μF; clamp capacitor C_r: 10 μF; couple inductor $L_1 = L_2 = 6.3$ μH; extra inductor $L_e = 1.3$ μH; core: TDK EI 35; $N_{L1} = N_{L2} = 36$ turns; $N_e = 10$ turns; resonant tank: $L = 3.64$ μH, $C = 0.34$ μF; and load R: 10 Ω.

The switch conduction sequences of the proposed converter are shown in Figure 8. It shows that the duty cycles are greater than 50%. Thus, the proposed resonant converter works in symmetrical continuous conduction boost mode. Figure 9 shows the input voltage waves and input current waveforms with and without input current shaper (ICS). The line current (I_t) and line voltage (V_t) of the proposed converter are shown in Fig. 9*a*. It can be seen that the power factor is almost one. The ICS achieves a power factor correction and low ripple in this situation. Figure 9*b* shows the distortion input voltage waves without ICS, where the ripple variation is very large. The tank voltage source is shown in Figure 10. The results are consistent with the typical waveforms in Fig. 4*b*. Figure 11*a* shows the voltage across capacitor C_r in the proposed topology. It can be seen that the voltage is the variation of V_{in}. The voltages across inductors L_1, L_2 are shown in Fig. 11*b*. It has the same wave shape and satisfies the theoretical prediction. The experimental resonant tank voltage and current waveforms are shown in Figs. 12*a* and 12*b*, respectively. To demonstrate the theoretical prediction, the proposed converters with and without ICS were implemented. The corresponding line-current harmonics are shown in Fig. 13 for two different cases. The odd-order harmonics of input currents I_h are expressed as a ratio of the fundamental current I_1. The harmonic of the converter without ICS is the worse one. It satisfies the better low-ripple condition. Finally, the efficiency of the power stage of the two different converters is shown in Fig. 14. The maximum value at full load is about 90%, and the converter without ICS filter is the worse one.

6 Conclusions

A novel simple single-stage resonant converter has been introduced. It is shown that the power factor of the proposed resonant converter can be much improved by properly designing the control circuit. This converter can achieve small converter size and near zero input current using coupled inductor techniques. The proposed circuit is of simple topology and control strategy. It has several advantages such as lower switch and lower stresses on capacitor C_r. This makes the conduction and switching losses low and may result in a high efficiency. In this paper, a small capacitor is normally used as the input filter in the proposed topology, while a significant lowpass filter is used in the conventional boost converter. It is proved that the proposed boost converter has the same steady-state properties as the conventional resonant converter. Finally, conversion performance can also be improved and component stresses reduced, provided that the integration process is well thought out and executed properly.

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