Dithering Skip Modulation, Width and Dead Time Controllers in Highly Efficient DC-DC Converters for System-On-Chip Applications

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***Abstract*—This paper proposes temperature-independent load sensor (LS), optimum width controller (OWC), optimum dead-time controller (ODC), and tri-mode operation to achieve high efficiency over an ultra-wide-load range. Higher power efficiency and wider loading current range require rethinking the control method for DC-DC converters. Therefore, a highly efficient tri-mode DC-DC converter is invented in this paper for system-on-chip (SoC) applications, which is switched to sleeping mode at very light load condition or to high-speed mode at heavy load condition. The efficiency improvement is upgraded by inserting new proposed dithering skip modulation (DSM) between conventional pulse-width modulation (PWM) and pulse-frequency modulation (PFM). In other words, an efficiency-improving DSM operation raises the efficiency drop because of transition from PWM to PFM. Importantly, DSM mode can dynamically skip the number of gate driving pulses, which is inverse proportional to load current. Simplistically and qualitatively stated, the novel load sensor automatically selects optimum modulation method and power MOSFET width to achieve high efficiency over a wide load range. Moreover, optimum power MOSFET turn-on and turn-off delays in synchronous rectifiers and reduced ground bounce can save much switching loss by current-mode dead-time controller. Experimental results show the tri-mode operation can have high efficiency about 90% over a wide load current range from 3 to 500 mA. Owing to the effective mitigation of the switching loss contributed by optimum power MOSFET width and reduction of conduction loss contributed by optimum dead-times, the novel width and dead-time controllers achieve high efficiency about 95% at heavy load condition and maintain the highly efficient performance to very light load current about 0.1 mA.**

***Index Terms*—DC-DC converter, delay-line chain, dithering skip modulation, ground bounce, load sensing circuit, optimum dead-time, width controller.**

I. Introduction

As IS well known, dynamic (or adaptive) voltage scaling (DVS or AVS) technique is widely used as one of the most effective means for achieving energy-efficient design [1]. Generally speaking, power consumption and fast transient response [2] have become the most important issues in portable battery-powered applications and high-performance desktop and server applications. The attractive salient features of DVS systems trigger the design of fast and adaptive-output-voltage DC-DC converters with high efficiency over a wide load current range. For an efficient DVS system, highly efficient power conversion achieved by DC-DC converters not only in sleeping mode at very light load condition but also in high-speed mode at heavy load condition.

A popular technique to improve the efficiency over a wide load current range is the hybrid mode, which is composed of pulse-width modulation (PWM) and pulse-frequency modulation (PFM) [3], [4]. Hybrid mode achieves a high efficiency for the load current region A and region B in Fig. 1. However, there exists an efficiency dropping in region C. It means that the efficiency curve is not smooth at the transition between PWM mode and PFM mode. It is a matter of efficiency and current load range for hybrid-mode modulation technique. The hybrid-mode modulation can maintain a high efficiency by closing the two peak efficiency values to reduce the efficiency drop at the sacrifice of load range. Thus, under a wide load range, a new technique named as DSM is required to raise efficiency drop between transitions of PWM and PFM in Fig. 1. A novel temperature-independent load sensor is proposed to dynamically switch among three modes, which are PWM, PFM, and DSM modes. Furthermore, compared with PSM mode and burst mode [5]–[7], DSM mode uses the dithering technique to reduce the output ripple [8]. Due to the insertion of DSM mode at medium load range, high power conversion efficiency over a wide load range can be achieved by arranging two peak efficiency values of PWM and PFM at light load and heavy load, respectively. In Fig. 1, the improved result is expected as smooth efficiency curve from curve I for PWM mode to curve III for DSM mode and further extending to curve II for PFM mode with a smaller output voltage ripple than that of a hybrid mode.

In order to raise efficiency of DC-DC converters at light or very light load current condition, two novel techniques are demanded to save much switching power loss. One is width controlling technique [9]–[12] and the other one is dead-time controlling technique. As we know, the major power loss at light or very light load condition is switching power loss. How to reduce power loss in every switching cycle is an important issue to get higher power conversion efficiency. A prevailing technique named as optimum width controller (OWC) is introduced to get much power loss reduction at light or very light load condition [13]. Depending on load condition decided by load sensor, OWC can dynamically adjust optimum width of power MOSFET and size of driver to save much power. Moreover, the bouncing effect

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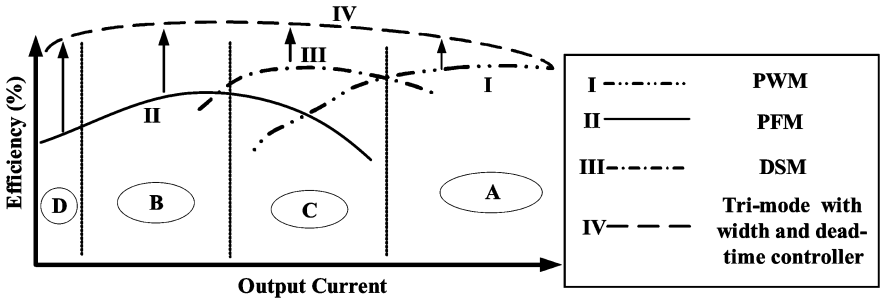

Fig. 1. Efficiency versus the output current for four control techniques. (a) Curve I is the efficiency of PWM mode. (b) Curve II is the efficiency of PFM mode. (c) Curve III is the efficiency of DSM mode. (d) Curve IV is the efficiency of proposed DC-DC converter.

can be reduced enormously because of the load dependent response drivers' control. At the same time, lower bouncing effect prevents the decision circuit of duty cycle from being disturbed.

After reduction of switching power loss by dynamically adjusting power MOSFET size, reduction of power loss due to improper switching of power MOS transistors becomes an important issue for raising power conversion efficiency from medium to very light load condition. Generally speaking, synchronous rectifiers are now widely used in essentially all low-voltage and high-frequency dc power supplies for reducing conduction losses. The optimum utilization of synchronous rectifiers depends on the ability to adjust the commutation dead-times. Hence, an optimum dead-time controller (ODC) is proposed to decide an optimum dead-times by a tradeoff technique between long searching optimum dead-times and a bulky analog implementation. Therefore, owing to OWC and ODC techniques, the final power conversion efficiency curve can be raised to curve IV in Fig. 1. Power conversion efficiency can be maintained a higher value in case of very light load current because of a reasonable small width size and an optimum dead-time. Importantly, high efficiency from medium to very light load condition is achieved by reducing switching power loss and improper switching loss. Thus, ultra wide load range power conversion efficiency about 95% is achieved by a tri-mode DC-DC converter with LS, OWC, and ODC techniques.

The architecture of DC-DC buck converter with DSM mode is illustrated in Section II. The circuit implementations of tri-mode control are described in Section III. Experimental results are shown in Section IV and we make the conclusion in Section V.

II. Architecture of Buck DC-DC Converter With DSM Mode

Fig. 2 shows the architecture of a buck DC-DC converter modulated by a tri-mode controller, which is composed of PWM, PFM, and DSM modulation modes. The load sensor estimates the load condition and sends the digital decision code $(D_1, D_{2,...,}D_N)$ to decoder in order to dynamically select an optimum modulator among these three modulators. Compared with the prior design [3], this architecture does not need an external pin to decide the optimum modulator because of automatic mode selection generated from load sensor.

A simple and accurate current sensing technique called SENSEFET topology illustrated by literature [14] is modified and shown in Fig. 3 for dynamic current sensing. The size of power pMOS and nMOS transistors varies with output of width controller according to load current. Thus, the size of sensing pMOS is needed to vary synchronously to get a ratio of power pMOS transistors to sensing pMOS transistors about 1000. In other words, the value of current flowing through sensing pMOS transistors is about one thousandth that of inductor current I_L. During the sensing period, M_{S1} is turned on to make V_a equal to V_x and V_b is equal to V_a because of closed loop constituted by op amp. Hence, the value of sensing current $I_{\rm sense}$ is equal to one thousandth that of inductor current I_L. Besides, the sensing current is converted to a sensing voltage $V_{\rm sense}$ by a sensing resistor $R_{\rm sense}$ and the detail waveforms are shown in Fig. 4. It illustrates the waveforms of inductor current I_L and $V_{\rm sense}$ at different load conditions $I_{\rm load1}$ and $I_{\rm load2}$. During the steady-state, the output current ripple is[15]

$$\Delta I = \frac{V_o(1-D)}{Lf} \tag{1}$$

where D is the duty ratio, L is the inductance, and f is the frequency of the switching signal for power pMOS/nMOS transistors. The peak value of output ripple is

$$I_{\rm peak} = I_{\rm load} + \frac{1}{2}\Delta I = I_{\rm load} + \frac{V_o(1-D)}{2Lf}. \tag{2}$$

Sensing voltage $V_{\rm sense}$ generated in Fig. 3 has peak value given by

$$V_{\rm sense\_peak} = \frac{R_{\rm sense}}{1000} I_{\rm load} + \frac{(1-D)R_{\rm sense}}{2000Lf} V_o. \tag{3}$$

Thus, the peak value of sensing voltage $V_{\rm sense}$ is proportional to output load current. As we know, it is difficult for simple comparators to decide the switching points of three modes because the value of $V_{\rm sense}$ is too small. A novel load sensor, which is composed of a current sensing circuit with SENSEFET topology and a current-mode delay-line analog-to-digital (A/D) converter, is proposed to determine the load condition in Fig. 5. As mentioned above, current sensing circuit generates sensing voltage $V_{\rm sense}$ to stand for load condition. At the same time, $V_{\rm sense}$ is sampled and held to get a peak voltage by sample and hold circuit. The V-I converter converts the peak value of $V_{\rm sense}$ to a current signal for driving the delay-line A/D converter. Owing to the temperature independent characteristic of the V-I converter [16], the current signal I is independent of temperature variation, meanwhile, the delay-line A/D converter is also independent of temperature variation. The output of delay-line

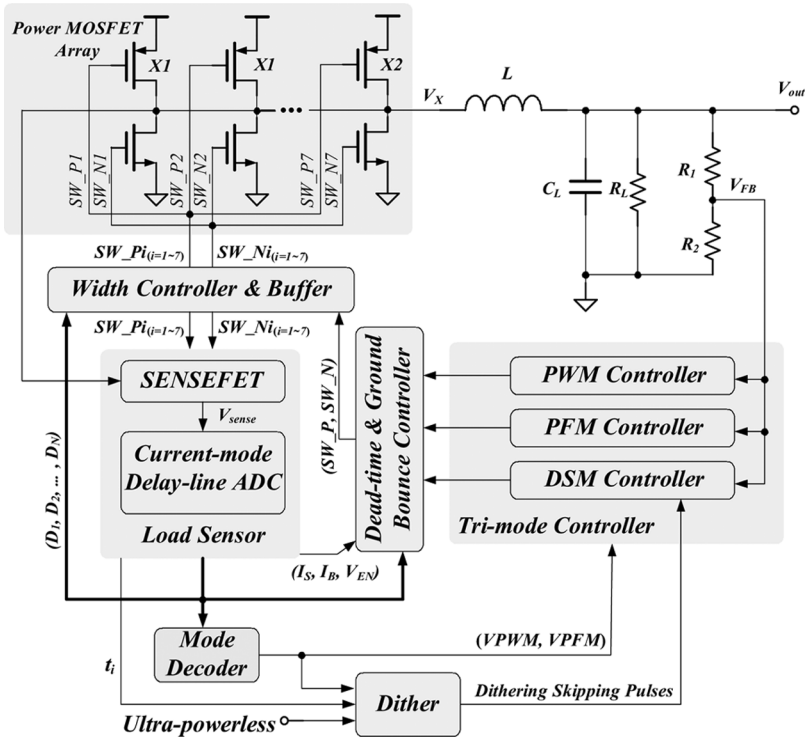

Fig. 2. Block diagram of the tri-mode buck converter.

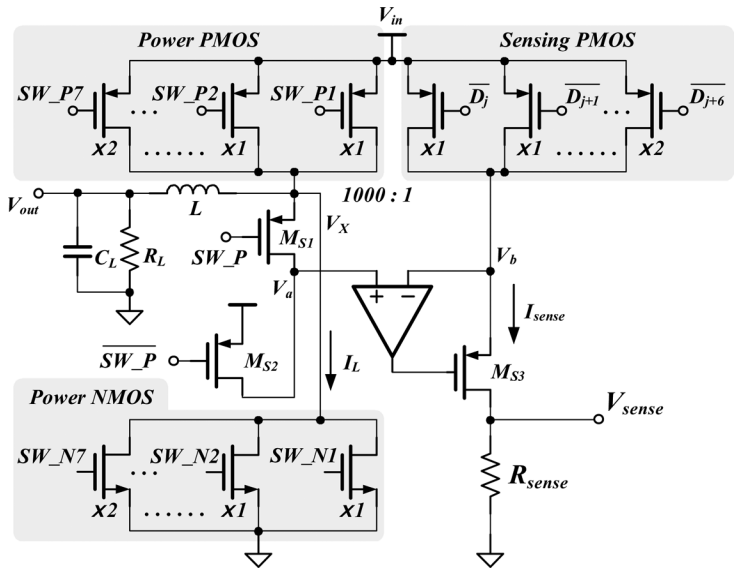

Fig. 3. Modified current sensing technique in SENSEFET topology [14] for the implementation of dynamic width and dead-time adjustment.

A/D converter is sent to mode decoder for selecting optimum modulation mode and to dither circuit for deciding the dithering skipping pulses.

The mode decoder generates two mode-selected bits, which are signals *VPWM* and *VPFM*. Table I shows the codes for determining the modulation mode. The concept of the dithering skipping pulses for DSM mode is illustrated in Fig. 6. The decreasing load current increases the size of dithering skipping (DS) period as shown from Fig. 6(a)–(c). The size of *DS period* is inversely proportional to the load current. The latter section will demonstrate this phenomenon. Thus, a *DS period* gradually contains more *DS modules* when the load current continuously decreases. In order to reduce output voltage ripples, the dithering skip technique is implemented in the *DS module*. The function of a *DS module* makes the DC-DC converter skip one switching pulse among three sequential switching cycles. Certainly, much power can be retrenched by reducing the switching consumption of power MOSFET because of the gradual decrease of load current. Therefore, an *ultra-powerless* pin is turned on to skip more pulses.

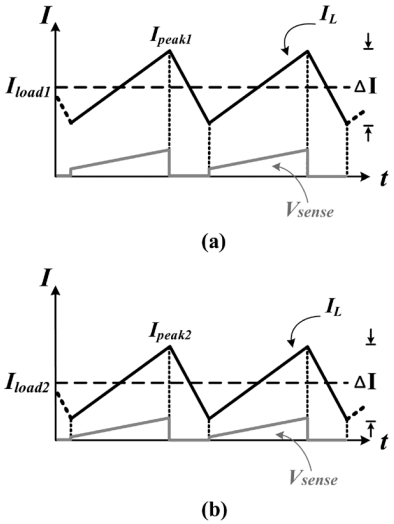

Fig. 4. Waveforms of sensing voltage $V_{\rm sense}$ and output load current $I_{\rm load}$. $(I_{\rm load1} > I_{\rm load2})$.

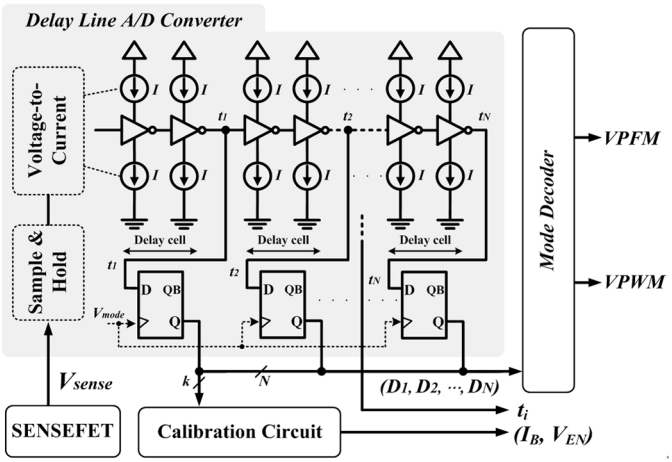

Fig. 5. Block diagrams of load sensor and mode decoder.

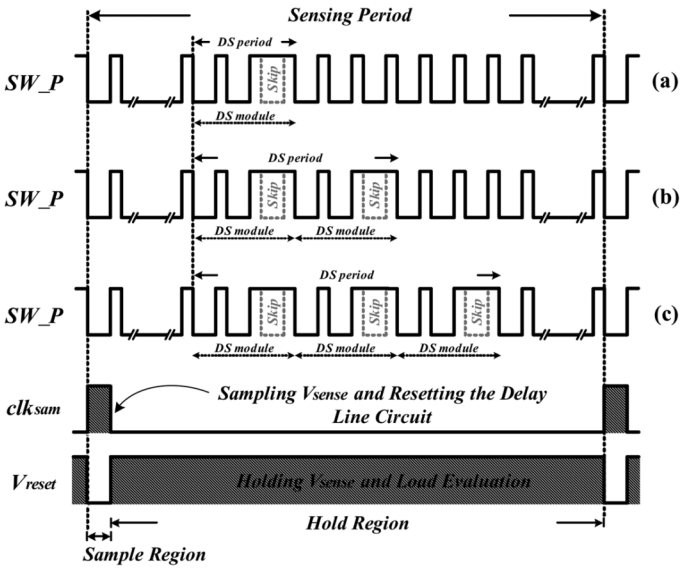

Fig. 6. Timing diagrams for dithering skip modulation.

TABLE I
CONTROLLER MODE

	VPWM	VPFM
PWM mode	*1*	*0*
DSM mode	*0*	*0*
PFM mode	*0*	*1*

III. CIRCUIT IMPLEMENTATIONS OF TRI-MODE CONTROL

A. Tri-Mode Controller

According to the operation codes in Table I, the tri-mode controller composed of three modulators is shown in Fig. 7. Depending on the load condition, the tri-mode controller selects one optimum mode from these three modulator modes to generate the switching signal $V_{\rm switch}$ for current-mode deadtime (CDT) controller. Then, *SW_P* and *SW_N* signals are used for triggering power pMOS and nMOS transistors, respectively. When (*VPWM, VPFM*) is equal to (1, 0), the conventional current-mode with feedback control is adopted in PWM mode. The comparator named as *comp1* is used for hysteretic control in PFM mode. If *VPFM* signal is logic "0", the comparators *comp1* and *comp3* are disable and their output values are set to logic "1". The other comparator *comp2* is utilized to be zero current detector (ZCD) to turn off power nMOS in order to prevent negative inductor current. Similarly, the converter is switched to DSM mode when the code (*VPWM, VPFM*) is equal to (0, 0). In the meanwhile the dithering skip circuit is ready to skip some pulses of PWM mode to save much power consumption. Owing to the dithering technique, output voltage ripples can be smaller than that of PSM mode or burst mode [5]–[7]. Certainly, the power consumption can be reduced by the skipping pulses and the skipping pulses do not dramatically affect the output voltage because of dithering technique.

As we know, if the load condition is continuing to reduce, the efficiency of DSM mode will be worse than PFM mode. Thus, the load sensor will send a code (*VPWM, VPFM*) equal to (0, 1) and the tri-mode controller is switched to PFM mode. The high efficiency can be obtained again by this simple modulation when load current is light. The load sensor is turned off to save much power consumption in PFM mode. However, it is a problem for coming back to DSM or PWM modes when load current changes from light to heavy. Owing to PFM mode is operated in the discontinuous conduction mode (DCM), the peak value of $V_{\rm sense}$ can not be indicative of the average load current. Thus, the delay-line A/D converter will be reset and adopt the comparator named as *comp3* to end the PFM mode when the load current is heavy. A lower threshold voltage is set to determine whether the PFM mode control can supply the output loading or not. Once the driving capability of the converter in PFM mode is not enough to supply the output load current, there is a large dropping voltage at output node. When the feedback voltage $V_{\rm fb}$ is lower than the pre-defined threshold voltage, the tri-mode controller finishes PFM mode and switches to PWM mode instead of DSM mode in order to provide much energy and reduce the output voltage ripple. The pre-defined threshold voltage is a voltage level with an offset voltage V_a lower than the reference voltage $V_{\rm ref}$.

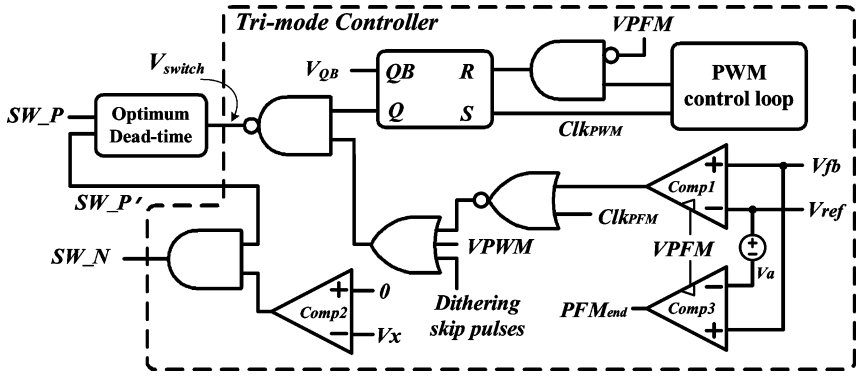

Fig. 7. Tri-mode controller composed of PWM, PFM, and DSM modes.

B. Current-Mode Delay-Line A/D Converter With Temperature Independent Characteristic

Resorting to a high-resolution A/D converter is not economic for the implementation of the load sensor. The reason is that a high-resolution A/D converter consumes much power and chip area for energy efficiency of DC-DC converters. Thus, a simple delay-line A/D converter is a better solution for DC-DC converters. The principle of the voltage-mode delay-line A/D converter [17] is based on the propagation delay of a logic gate is inversely proportional to the gate supply voltage. Owing to the load condition can be represented by the peak value $V_{\rm sense}$, a sample-and-hold circuit can hold this peak value. Therefore, the peak value $V_{\rm sense}$ can be used as supply voltage of delay-line chain in order to convert this voltage level to a digital word. This digital word represents loading condition of DC-DC converters and varies with the peak value of $V_{\rm sense}$ when load current varies.

However, the temperature dependence is an encumbrance for the accuracy of the voltage-mode delay-line A/D converter proposed in [17]. As we know, the increasing temperature makes the mobility and threshold voltage decrease. Thus, the driving current of each delay cell of the voltage-mode delay-line chain will be affected seriously to make the conversion digital word varying with temperature. Besides, the peak value of $V_{\rm sense}$ voltage level is needed to be converted to the voltage level of succeeding logic circuit. In the meanwhile an extra voltage level shifter is needed for the conversion. Higher sensing speed needs more driving current consumption for the voltage level shifter. In other words, the voltage-mode delay-line A/D converter is not suitable for load sensor.

In this paper, a current-mode delay-line A/D converter [18] is adopted to improve the temperature dependent drawback as shown in Fig. 8(a). It is composed of a sample-and-hold circuit, a temperature-independent V-I converter, a current-mode delay-line chain, and a calibration circuit. The detailed schematic of the current-mode delay-line chain is shown in Fig. 8(b). The calibration circuit is used for dead-time controller and illustrated in a later section.

The load sensor works only in PWM and DSM modes not in PFM mode for power reduction in PFM mode. At the beginning of the sensing period, a sampling clock $clk_{\rm sam}$ starts the sample region. In order to eliminate unnecessary mode switching and save the power consumption, the sensing clock $clk_{\rm sam}$ is periodically generated for several times of switching cycles. Besides, the sampling clock $clk_{\rm sam}$ is inverted to generate the active-low resetting pulse $V_{\rm reset}$. Thus, the logic function of $V_{\rm reset}$ in the sample region is written as

$$V_{\rm reset} = \overline{(VPFM + Clk_{\rm sam})}. \tag{4}$$

If $V_{\rm reset}$ is equal to logic "0", the delay-line circuit is reset. At the same time, the capacitor C_1 samples the $V_{\rm sense}$ voltage and V-I converter converts the $V_{\rm sense}$ voltage to a temperature independent current source.

In Fig. 8(a), if $g_{m2}R_s$ is greater than one, the voltages $V_{\rm sense}$ can be converted to I_{M2} written as

$$I_{M2} = \frac{V_{\rm sense} + V_{SG1}}{R_s} = \left(\frac{I_L}{1000} \times \frac{R_{\rm sense}}{R_s}\right) + \frac{V_{SG1}}{R_s}. \tag{5}$$

Similarly, I_{M4} is generated by connecting the gate of M_3 to ground for eliminating the extra signal V_{SG1} of (5). Subtracting I_{M4} from I_{M2}, the output current of the V-I converter I_{M7} is written as

$$I_{M7} = I_{M2} - I_{M4} = \frac{I_L}{1000} \times \frac{R_{\rm sense}}{R_s}, \quad \text{where } I_{M4} = \frac{V_{SG3}}{R_s} \tag{6}$$

Owing to the temperature independence of $R_{\rm sense}/R_s$, the V-I converter provides a temperature-independent current to the delay-line chain.

The hold region starts at the negative falling edge of the sampling clock $clk_{\rm sam}$ and holds the peak value $V_{\rm sense}$ to trigger the current-mode delay-line chain. In Fig. 8(b), each delay cell contributes delay time T_d and the driving current I_D are written as

$$T_d = \frac{2C_{\rm tot}V_{\rm DD}}{I_D}, \quad \text{where } C_{\rm tot} = \frac{5}{2}C_{\rm ox}\left(W_pL_p + W_nL_n\right). \tag{7}$$

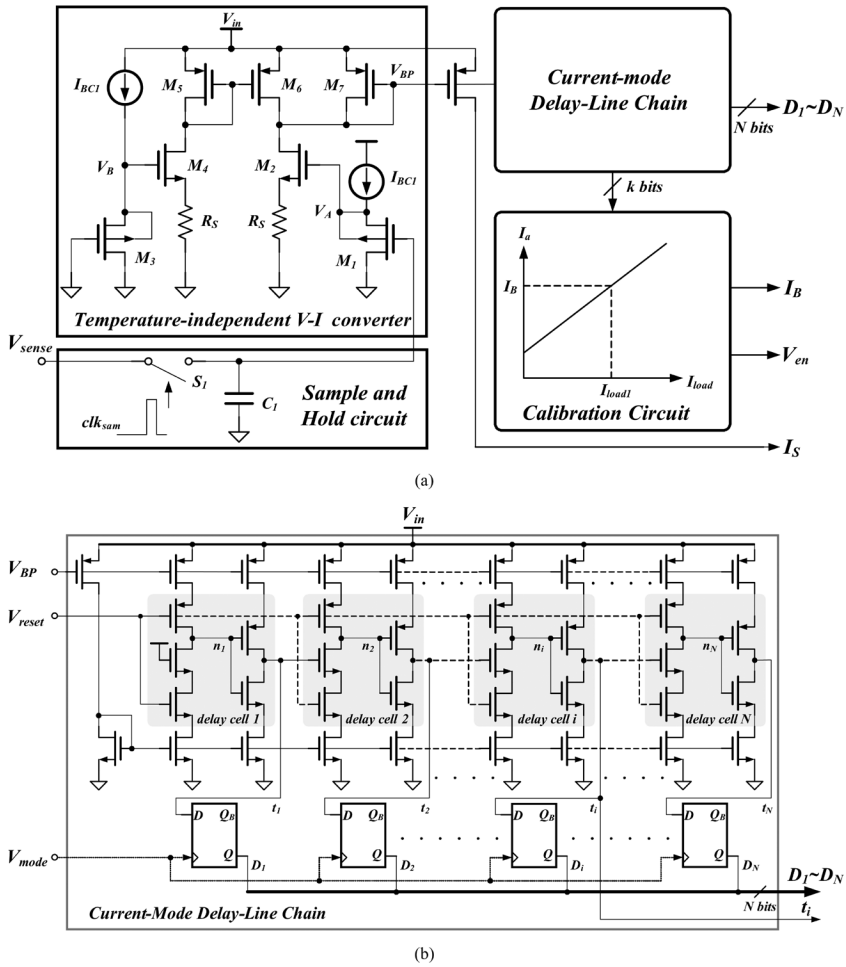

Fig. 8. (a) Current-mode delay-line A/D converter of the load sensor. (b) Schematic of the current-mode delay-line chain.

In (7), $C_{\rm tot}$ is the equivalent output capacitance of each delay cell. $L_{n(p)}$ and $W_{n(p)}$ are the channel length and width for N(P)-type MOSFETs of each delay cell, respectively. Larger load current comes with larger value of peak $V_{\rm sense}$ converted by the SENSEFET circuit. At the same time, the temperature independent current source is raised by V-I converter to decrease the propagation delay time T_d of each delay cell. The relationship between delay time T_d and inductor current I_L is shown as the following equations. Clearly, the propagation delay time T_d is inversely proportional to load current without any temperature dependent characteristic.

$$T_d = \frac{2C_{\rm tot}V_{\rm DD}}{I_D} = 2C_{\rm tot}V_{\rm DD} \times \frac{1000}{I_L} \times \frac{R_s}{R_{\rm sense}} = \frac{k}{I_L},$$
$$\text{where } k = 2000C_{\rm tot}V_{\rm DD}\frac{R_s}{R_{\rm sense}} \tag{8}$$

An example of the timing diagram generated by the delay-line chain is shown in Fig. 9. In order to get a digital word, a periodic pulse $V_{\rm mode}$ is used to trigger the register in the load sensor and then latch the outputs of the delay-line chain. Thus, the digital word can be generated, and the linear conversion of analog load current to 5-bit digital word is shown in Fig. 10. For instance, if the case is $(D_1 \sim D_5) = (11100)$, it means the load current is between I_{L4} and I_{L3}. Besides, if the resolution is not enough for design consideration, extra delay cells can be added to the delay-line chain. In other words, the signals $(t_1 \sim t_n)$ are not needed to select from consecutive delay cells. Furthermore, *DS period* of DSM mode is determined by two signals, $V_{\rm mode}$ and t_i, as shown in Fig. 9. A fixed positive rising edge of *DS period* starts the operation of the dithering skip code at the positive rising edge of $V_{\rm mode}$. The negative falling edge of *DS period* synchronizes with one of the outputs of the delay-line chain t_i, which ends the operation of the dithering skip code. The choice of t_i is a tradeoff between the efficiency and output voltage ripple. Hence, output load current determines the length of *DS period* because the propagation delay time of t_i is inversely proportional to the load current.

C. Decoder and Dithering Skip Pulses Generator

The succeeding decoder in Fig. 11 after current-mode delay-line A/D converter uses this digital word $(D_1, D_2, \ldots, D_N)$ to switch the tri-mode controller to an optimum modulation mode. Three digital mode bits (M_1, M_2, M_3) are selected from the digital word $(D_1, D_2, \ldots, D_N)$. The selection rule of digital mode bits defines the sizes of three mode region. Thus, the selection rule is determined by the tradeoff between efficiency and output voltage ripple according to the applications. In Fig. 11,

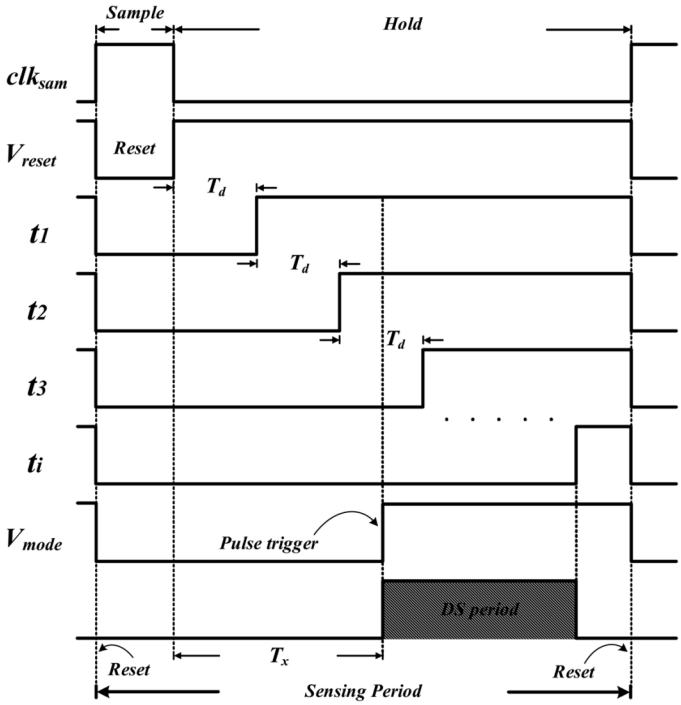

Fig. 9. Timing waveforms of delay-line chain.

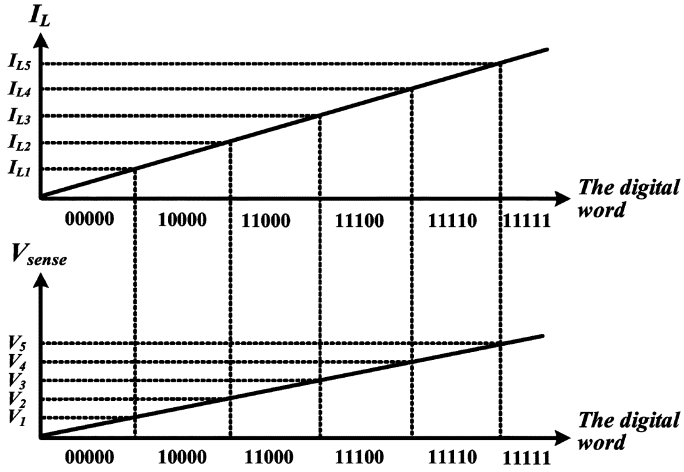

Fig. 10. Load current and sensing voltage $V_{\rm sense}$ versus the digital word.

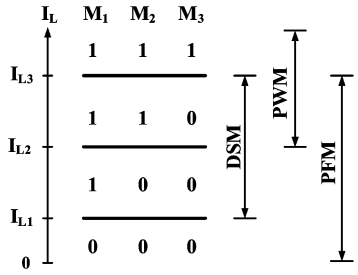

Fig. 11. Diagram of the mode decoder.

the Boolean functions of mode signals *VPWM* and *VPFM* are written as

$$VPWM_i = \overline{VPFM_i} \times M_2 \tag{9}$$

$$VPFM_i = PFM_{\rm end}\left(\overline{M_1} + (PFM)_{i-1}\right). \tag{10}$$

$VPWM_i$ and $VPFM_i$ stand for current condition of load current while $VPWM_{i-1}$ and $VPFM_{i-1}$ stand for previous state of load current. It is important to have a hysteretic region between PWM and DSM modes to eliminate unnecessary mode switching. Therefore, if PWM mode changes to DSM mode, the load current must be lower than I_{L2}. Similarly, load current must be higher than I_{L3} to let control mode back to PWM mode. Furthermore, a sudden heavy load current in PFM mode switches the modulation mode back to PWM mode not to DSM mode because smaller output ripples can be obtained in PWM mode.

Fig. 12 shows the generation of the dithering skip pulse when DC-DC converter operates in DSM mode. $DFF_{1,2}$ and $DFF_{3,4}$ are D-type flip-flops triggered by negative falling edge and positive falling edge, respectively. Dithering-skip-pulses generator generates many *DS modules* according the size of the *DS period*. Each *DS module* contains three pulses, which is composed of two *ON* signals and one *OFF* signal by a switching signal V_{QB} that is from SR latch of tri-mode controller. If the *ultra-power-less* is active high "1", each *DS module* is composed of one *ON* signal and two *OFF* signals to reduce much switching power loss.

D. Dynamic Adjustment Width Control Technique

A large and fixed size power MOSFET is used for DC-DC converter as shown in Fig. 13(b) and (d) in conventional DC-DC converters with hybrid modes. However, much switching power loss dissipates on the turn-on and turn-off power MOS transistors at light or very light load condition. In order to minimize the switching power loss, a low-voltage-swing MOS transistor gate drive technique [19] is proposed to improve the efficiency by scaling down supply voltage of gate drivers. However, the performance of power reduction by scaling down supply voltage of gate drivers is not better than by dynamically adjusting optimum width of power MOS transistors [20]. Scaling down the width of power MOS transistors can save much power dissipation in switching loss at light or very light load current. On the contrary, scaling up the width of power MOS transistors can save much power dissipation in conduction loss at heavy load current. Consequently, based on dynamic adjustment width control technique [13], an OWC technique is proposed to decide the optimum size of power pMOS to adapt to load current variation. The formula of optimum size is

$$W_{p\_\rm optimum} = \sqrt{\frac{T_s\left(\frac{D}{K_p} + \frac{b(1-D)}{K_n}\right)\left(I_{\rm load}^2 + \frac{\Delta I_{\rm load}^2}{3}\right)}{C_{\rm total}(V_{\rm DD} - V_t)V_{\rm DD}^2\left(1+\frac{1}{b}\right)\left(1+\frac{ap^N-1}{ap^N(ap-1)}\right)}} \tag{11}$$

where ap and N are the tapering factor and the series number of the drivers driving power pMOS. The b parameter is the pMOS to nMOS transistor width ratio within each inverter. D is the

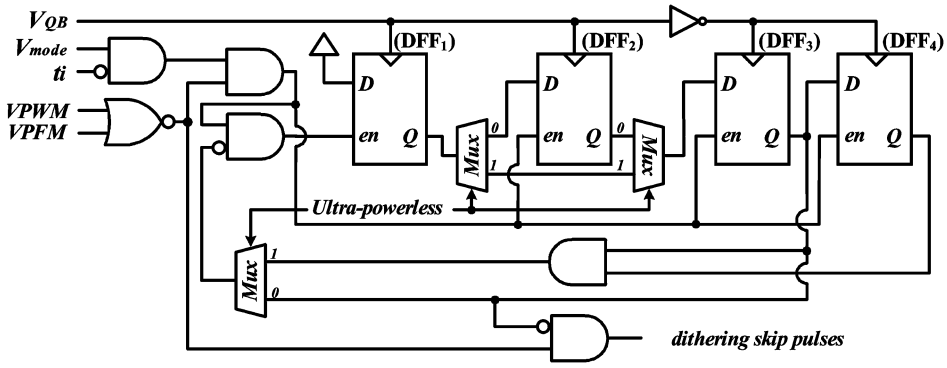

Fig. 12. Dithering skip pulses generator.

duty cycle and T_s is the switching period. Because the value of $(\Delta I_{\rm load}^2)/3$ is smaller than $I_{\rm load}^2$, $W_{p,{\rm optimum}}$ is directly proportional to $I_{\rm load}$. The curve A of Fig. 14 shows the optimum power MOSFET size over the entire load range. By dividing the load region into seven sections and basing on the middle value of each section, the OWC technique partitions the large power pMOS/nMOS into small units as shown in Fig. 13(c) and (e). Combining with the output digital word $(D_j \sim D_{j+6})$ of load sensor, the optimum width can be dynamically chosen as curve B of Fig. 14.

Besides, we do not need a large driver to charge or discharge the gate of the power MOSFET. Because the new proposed width controller partitions the large power MOSFET into small units, then each small power MOSFET unit has its own small tapering factor $a_{1\sim4}$. In our design, $a = 10.68$, $a_1 = (a^3/12)^{1/3} = 4.66$, $a_2 = (a^3/6)^{1/3} = 5.88$, $a' = 8.65$, $a_3 = [(a')^3/12]^{1/3} = 3.77$, and $a_4 = [(a')^3/6]^{1/3} = 4.76$. As a result, the width of power MOSFET varies with load current, the size of driver for charging or discharging the gate of power MOSFET also varies with the optimum width. Owing to the variation of power MOSFET width, the efficiency curve can raise to a high value when the load is from medium load to very light load condition. Therefore, the high efficiency can be extended to a lower load current range about 0.1 mA in PFM operation.

E. Current-Mode Dead-Time Controller

Previous techniques for improved synchronous rectifier commutation are: fixed dead-times, adaptive dead-times, direct ideal diode emulation for dead-times control, ideal diode emulation using delay-lock loop (DLL) for dead-times control, and sensorless optimization of dead-times [21]–[23]. The fixed dead-times control has the worst power efficiency because of the dead-times must be long enough to account for process/temperature and operating point variations. Actually, optimum dead-times should be varied with the load current. In design aspect, too long dead-times control conducts body diode shown as the waveform V_x in Fig. 15. On the contrary, too short dead-time control makes power nMOS transistors turn on too early and leak the energy stored at capacitor C_x to ground, not to load. Although, adaptive dead-time control adjusts the dead-time according to the variation of load, it is a suboptimal solution because of the slow response time of the comparators. Thus, based on incremental or reductive adjustment of dead-times between two sequential switching periods, using DLL for emulation of the ideal diode reduces the response time of zero drain-source voltage/current detection according to load variation. However, extensive usage of analog components to control dead-times of both edges deteriorates the power efficiency gained from the reduction of switching loss.

An interesting sensorless optimization of dead-times [23] is proposed to eliminate the request of sensing load and the bulky analog implementation. Even though it does not sense any node signals related to load variation, the optimization process is swamped in complex digital implementation and a long searching period for dead-times controller to minimize the steady-state duty cycle command. Most importantly, the prerequisite is that load and input voltage are constant during the execution of the dead-times search. There exists a tradeoff between cost and response time to load variation. Therefore, based on load sensor in tri-mode converters, the dead-times of both edges can be easily and dynamically adjusted to further improve the power conversion efficiency. Besides, in order to avoid getting a suboptimal dead-times, a calibration procedure is proposed to eliminate the possibility of a suboptimal solution in response to load variations.

In order to get optimum dead-times and reduce ground bounce effect, the optimum dead-time controller (ODC) is proposed and shown in Fig. 13(a). It converts pulse-width modulation (PWM) signal $V_{\rm switch}$ to two nonoverlapping signals *(SW_P, SW_P')* for driving power pMOS and nMOS transistors. The right side inverter chain adds delay to signal *SW_P'* from logic "1" to logic "0" and the left side inverter chain adds delay to signal *SW_P* from logic "0" to logic "1". Thus, we regulate the biasing current of left inverter chain, I_a, to dynamically control dead-times according to load variation. The predefined current I_B stands for biasing current of the nonoverlapping circuit for optimum dead-times at some predefined load current condition $I_{\rm load1}$ as shown in Fig. 8(a). The value of I_{B1} is smaller than that of I_B and equal to the value of I_S when the load current is equal to $I_{\rm load1}$.

Once load current is greater (or lower) than $I_{\rm load1}$, the current I_S is larger (or smaller) than I_{B1} because I_S is direct proportional to load current generated by current-mode delay-line

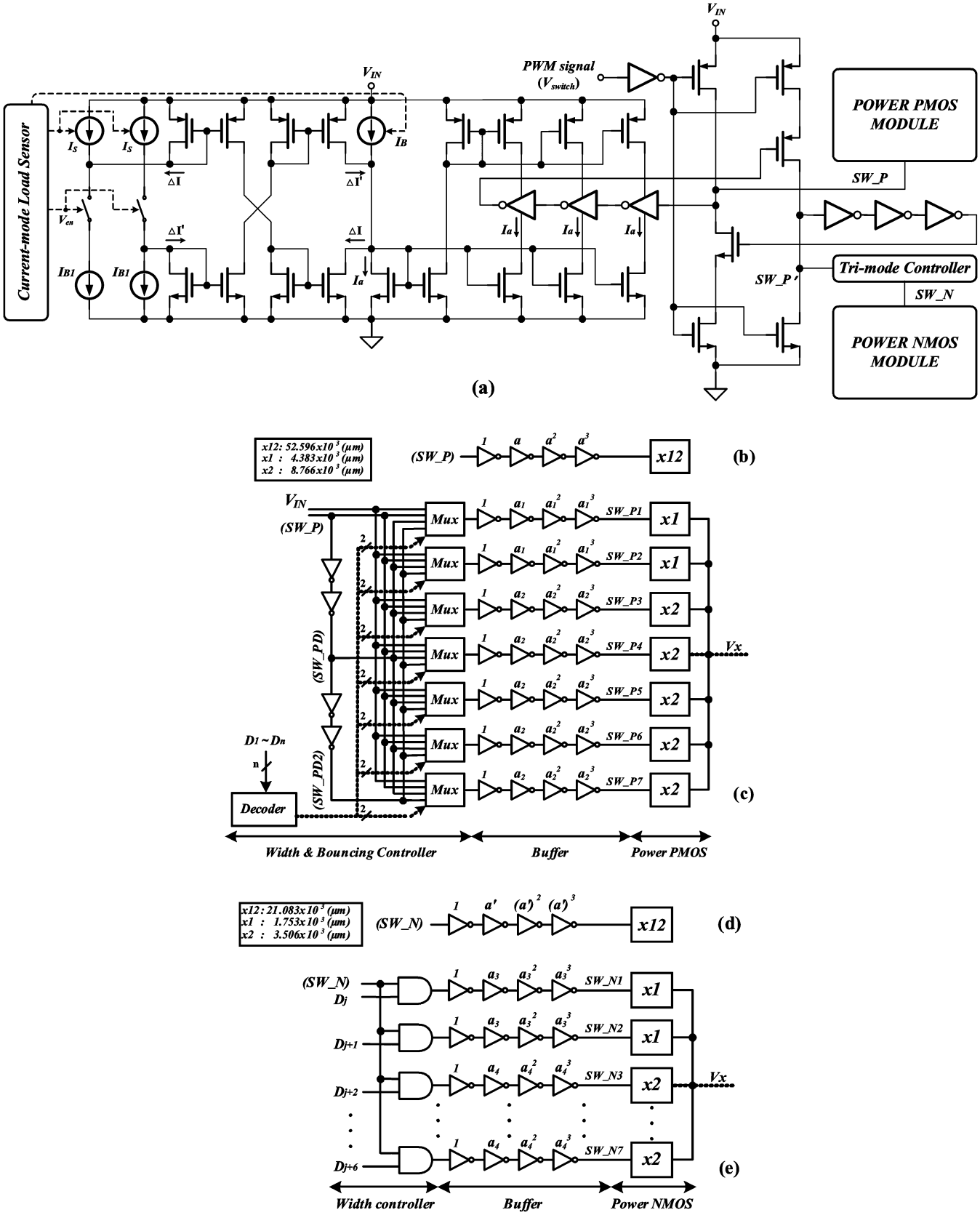

Fig. 13. (a). Schematic of optimum dead-time controller. (b) Traditional power pMOS module. (c) Power pMOS module for ODC technique. (d) Traditional power nMOS module. (e) Power nMOS module for ODC technique.

A/D converter. Therefore, the variation current $\Delta I'$ (or ΔI) is added (or subtracted) to I_B. Then, the driving current I_a is increased (or decreased) to reduce (or extend) the dead-times in response to load variation. In order not to affect the operation of

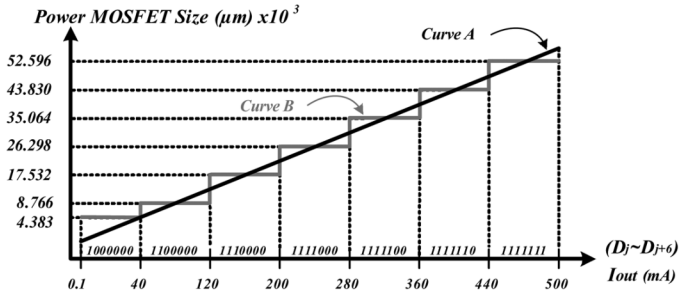

Fig. 14. Optimum size of P-type power MOSFET versus load current.

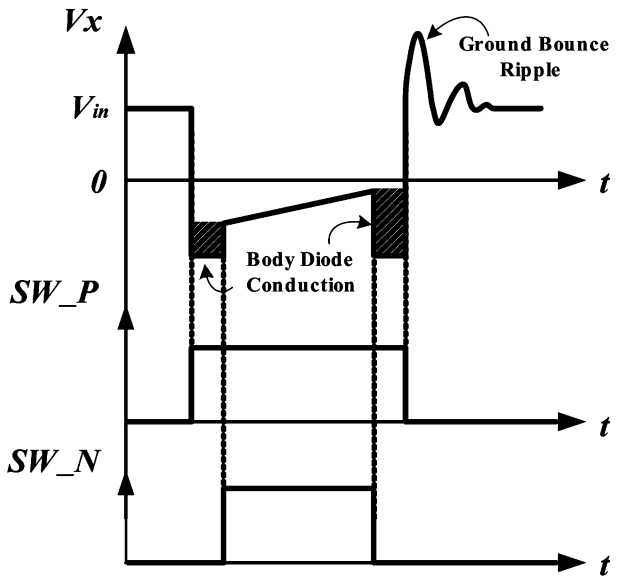

Fig. 15. Dead-time and ground bounce problems.

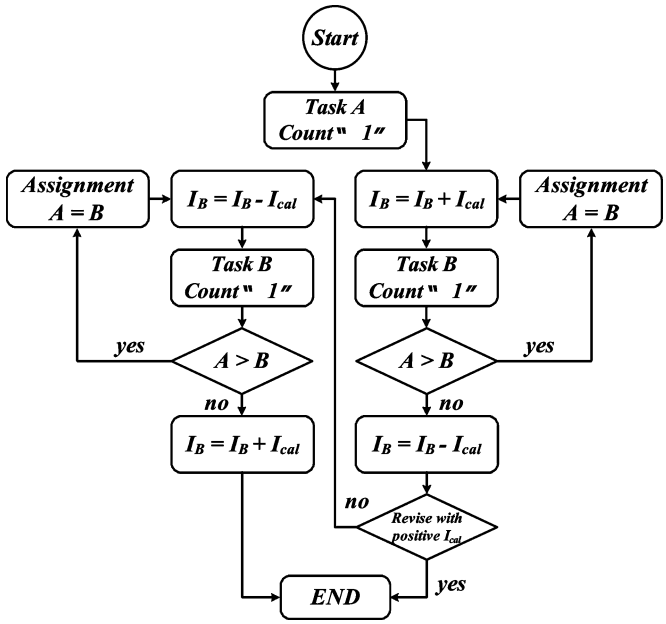

Fig. 16. Calibration flow chart for optimum biasing current I_B.

TABLE II
SPECIFICATIONS OF BUCK CONVERTER

Technology	*TSMC 0.35-μm process*
Input Voltage	*3.3 V*
Output Voltage	*1.65 V*
Output Current Range	*0.1 mA – 500 mA*
Pulse-Width Modulation Mode	
Load Region	*500 mA ~ 80mA*
Switching frequency	*1 MHz*
Output Ripple Voltage	*< 10 mV*
Dithering skip Modulation Mode	
Load Region	*120 mA ~ 40mA*
Output Ripple Voltage	*< 35 mV*
Pulse-Frequency Modulation Mode	
Load Region	*120 mA ~ 0.1 mA*
Switching frequency	*1 MHz*
Output Ripple Voltage	*< 20 mV*

TABLE III
COMPONENT VALUES

L	*4.7 μH*	R_{sense}	*1 kΩ*
C_L	*4.7 μF*	R_s	*500 kΩ*
R_{ESR}	*30 mΩ*		

soft-start, we use a control signal V_{EN} to turn off the dynamic delay-times. Hence, the dynamic adjustment of dead-time starts after the operation of soft-start. However, the values of I_B and I_{B1} may be suboptimal values because of environmental and process variation. Therefore, at the beginning of the converters, the calibration procedure can be used to correct the values of I_B as shown in Fig. 16. A suboptimal biasing current I_B makes the duty cycle larger than that of an optimum biasing current I_B. The reason is that the increment of duty cycle due to incorrect dead-times cause energy loss [23] increases the value of $V_{\rm sense}$. The larger value of $V_{\rm sense}$ increases the number of logic "1" of load digital word $(D_1 \sim D_N)$. Thus, the purpose of calibration procedure is to minimize the number of logic "1". In other words, it minimizes duty cycle and power loss by finding the optimum dead-times and correcting the values of I_B. After the calibration procedure, the load sensor can dynamically adjust the biasing current of the nonoverlapping circuit in response to load variation.

Besides, turning on the power MOSFET in proper sequences alleviates the ground bounce effects [24]. In Fig. 13(c), the twelve distributed power pMOS are divided into three groups and their trigger signals of buffer are named as *SW_P*, *SW_PD* and *SW_PD2*, respectively. When first power pMOS group conducts, V_x voltage level is close to $V_{\rm IN}$ gradually. The drain-source voltage of power pMOS is low enough that the delay signals *SW_PD* and *SW_PD2* are just triggered to turn on the remainder power MOSFET. It reduces the inductive current ripples generated by ground bounce.

Generally speaking, the rising rate of V_x signal varies with different load situation. In other words, at heavy load (or light load) condition, load current slows down (or speeds up) the

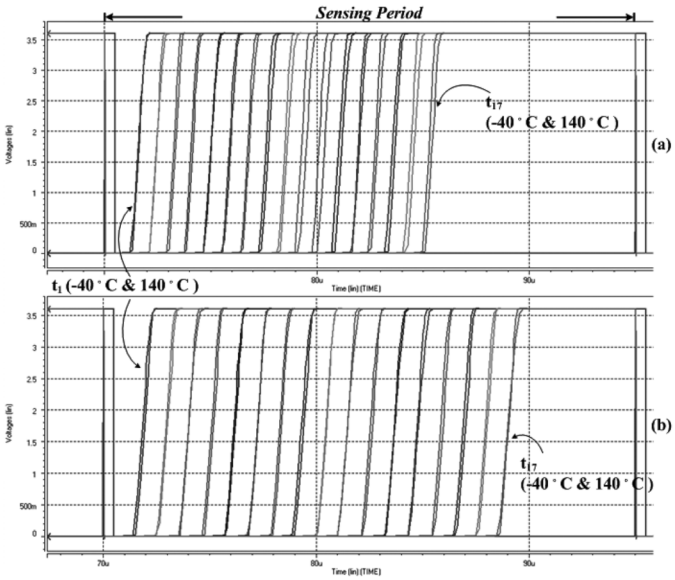

Fig. 17. Waveforms of delay-line chain with temperature variations ($-40\ ^\circ\text{C} \sim 140\ ^\circ\text{C}$). (a) Load current $= 120$ mA. (b) Load current $= 40$ mA.

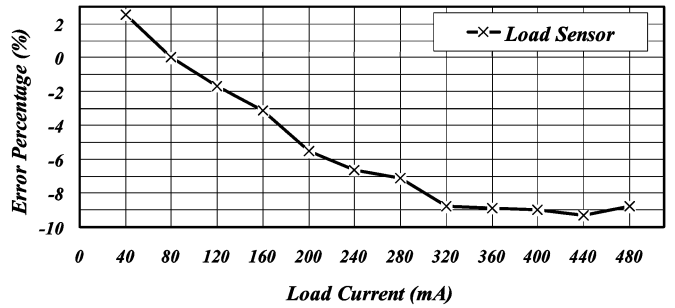

Fig. 18. Error percentage of current-mode delay-line load sensor.

rising rate of V_x. In order to have the same performance of reduced ground bounce results, the first power pMOS group must be dynamically adjusted to maintain a constant rising rate of V_x. Therefore, the load digital word $(D_1 \sim D_N)$ not only chooses the optimum width of power MOSFET, but also decides the turn-on sequences of twelve distributed power pMOS. As a result, the effect of ground bounce is slashed by our proposed ODC technique.

IV. Experimental Results

The proposed tri-mode control DC-DC converter with a load sensor has been implemented in TSMC double-poly four-metal 0.35 μm CMOS technology. The threshold voltages of nMOSFET and pMOSFET are 0.55 V and 0.65 V, respectively. Specifications of DC-DC buck converter are listed in Table II and the component values are shown in Table III.

As illustrated in Fig. 11, the I_{L3}, I_{L2}, I_{L1} are set to 120 mA, 80 mA, and 40 mA in the design. With temperature variation from $-40\ ^\circ$C to 140 °C, Fig. 17(a) and (b) illustrate

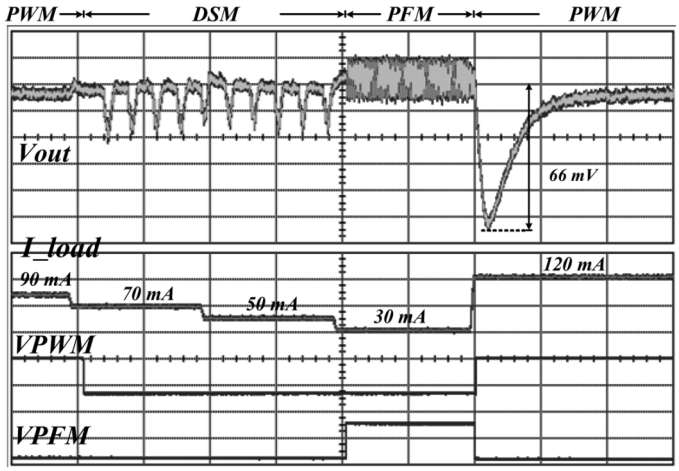

Fig. 19. Mode transition waveforms of the proposed tri-mode DC-DC buck converter. (V_{out}: 10 mV/Div).

outputs of seventeen delay cells in delay-line chain when DC-DC converter operates in 120 mA and 40 mA, respectively. Temperature-independence outputs from t1 to t17 are selected to latch as digital word $(D_1, D_2, \ldots, D_N)$. Obviously, the temperature dependence of delay-line chain is small enough to convert output load current to an accurate digital word $(D_1, D_2, \ldots, D_N)$. It means that our decision of digital word does not vary too much with temperature variation. As we expected, temperature variation does not influence the transition point from PWM mode to DSM mode. Fig. 18 is the error percentage of proposed current-mode delay-line load sensor. The worst case is -9.3% when load current is 440 mA. However, it doe not influence the decision of dithering skipping pulses in DSM mode because modulation mode is not switched from PWM to DSM at load current about 440 mA. The error percentage should be low in DSM mode. Thus, for the load current range from 120 mA to 40 mA, the error percentage is kept within $\pm 2.5\%$.

The mode transitions are shown in Fig. 19. The operating mode changes from PWM mode to DSM when load current changes from 90 mA to 70 mA at the left side in Fig. 19. There are some pulses skipped by dithering skip-control circuit. Thus, when load current decreases from 70 mA to 50 mA, the dithering skip-pulses increase. Once load current decreases below 40 mA, the operation mode switches to PFM mode. In order to prevent the dropout voltage from being too large, the operating mode switches from PFM mode to PWM mode, not DSM mode. Thus, the dropout voltage of output voltage is about 66 mV in the case of load variation about 90 mA.

In DSM mode, experimental results are shown in Fig. 20. In Fig. 20(a), the output ripple of the converter is 30.7m V and the number of *DS module* is one when the loading is about 120 mA. With the gradual decrease of load current from 80 mA to 40 mA, the number of *DS module* is increased from two in Fig. 20(b) to three in Fig. 20(c). Also, output ripples can be kept below 31 mV (29.3 mV at load current 80 mA and 16.5 mV at load current 40 mA). Therefore, much power can be retrenched by reducing

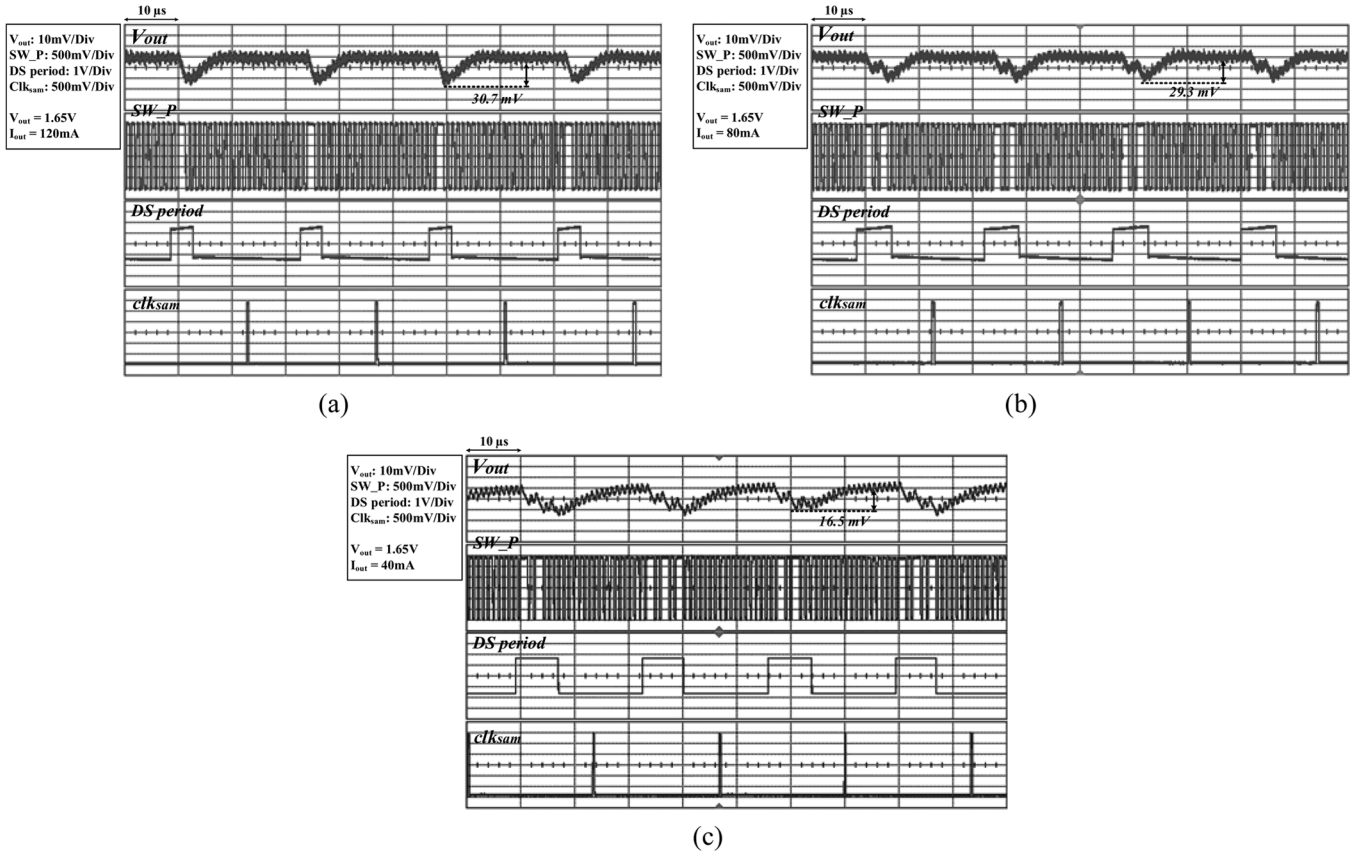

Fig. 20. Waveforms of proposed DSM DC-DC buck converter. (a) Load current $=$ 120 mA. (b)Load current $=$ 80 mA. (c) Load current $=$ 40 mA.

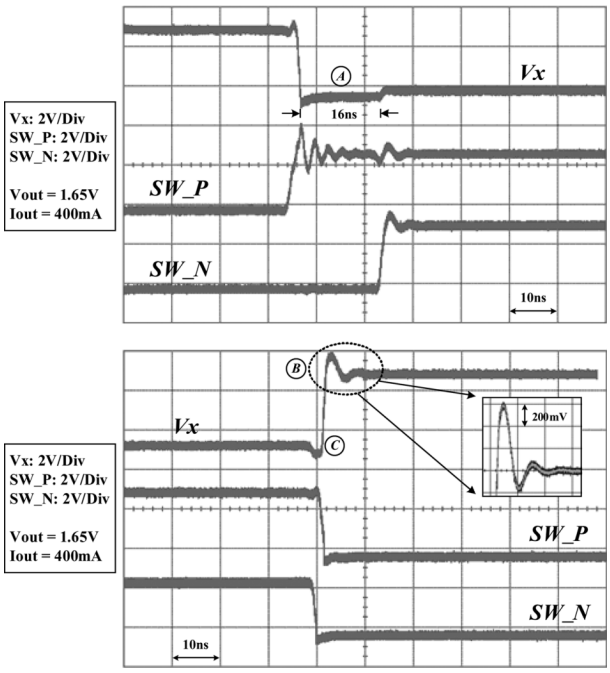

Fig. 21. Measurement results of conventional buck converter with fixed dead-time control ($I_{\rm out} = 400$ mA).

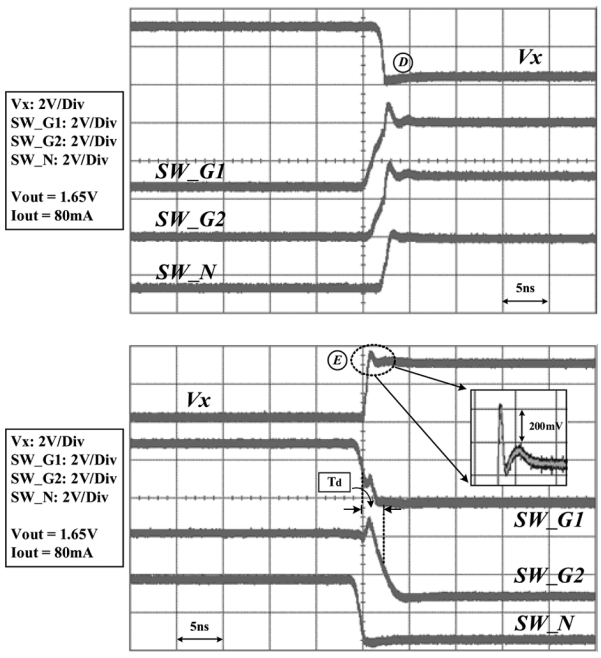

Fig. 22. Measurement results of tri-mode buck converter with ODC technique. ($I_{\rm out} = 80$ mA).

the switching consumption of the power MOSFET when load current changes from medium to light.

Fig. 21 shows waveforms of V_x and power MOS control signal *SW_P* and *SW_N* in the conventional buck converter

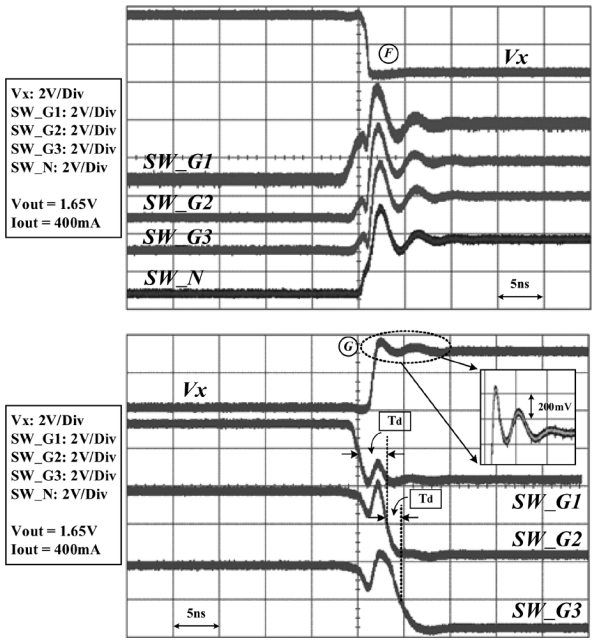

Fig. 23. Measurement results of tri-mode buck converter with ODC technique. ($I_{\rm out} = 400$ mA).

with fixed dead-times structure. Obviously, there are the phenomenons of body diode conduction and big ground bounce ripples in region A, C and B. As the foregoing, the phenomenon causes the power loss and reduces the efficiency. Figs. 22 and 23 are the waveforms of tri-mode buck converter improved by ODC technique with load current 80 mA and 400 mA, respectively. $SW\_G1 \sim SW\_G3$ are the triggering signals for three power pMOS groups. By the proposed ODC, the phenomenons of body diode conduction are almost eliminated in region D and F. The values of the ground bounce ripple in region E and G are only half that of conventional design. Because the number of first power MOSFET groups is modified according to load variation, the ground bounce ripples are 430 mV in 80 mA load current and 450 mV in 400 mA load current. The rising rate of V_x is kept constant by our proposed technique. The overall power efficiency improvement of dead-time and ground bounce is about 1%∼5%.

Fig. 24 shows the improvement of power efficiency by our proposed technique. In PWM mode of tri-mode converter, the power efficiency is higher than that of the converter with only PWM control because of the OWC and ODC controllers. The ODC controller can reduce the switching power loss while the OWC controller can reduce conduction loss a little because the size of power MOSFET is limited within a reasonable value. The improvement is not very large owing to the reduction of switching and conduction loss is very small compared to large output power consumption. Moreover, the efficiency difference between PWM control and tri-mode control becomes large when the operation mode switches to DSM mode. The efficiency drop between PWM control and PFM control is improved about 5.6%. The maximum power efficiency gained from DSM mode is about 8% when we use the dithering skip-control. When load current decreases below 40 mA, mode decoder selects the PFM mode to reduce the switching loss. However, we can find the efficiency improvement between the tri-mode converter in PFM mode and the converter with only PFM controller. The improvement increases from 3% to 7% in case of decreasing load current. As we know, it is obvious the benefit is gained from OWC and ODC controllers because OWC and ODC controllers can save much switching power loss.

Furthermore, compared the proposed dynamic adjustment width control with conventional design, the improved ratio about the power consumptions of driver and power MOSFET is shown as curve A of Fig. 24. Consequently, when the load current changes from heavy to very light load, the improved ratio of power consumption becomes higher and higher and the maximum value is achieved 90% at $I_{\rm load} = 0.3$ mA. With the insertion of DSM mode, dynamic adjustment width controller and optimum dead-time controller, the efficiency is above 90% achieved over a wide load current range from 0.3 mA to 500 mA. Basically, much improvement in power efficiency is achieved and high efficiency is maintained to a very light load, about 0.1 mA. The power efficiency of light load is raised to about 90%. The chip micrograph is shown in Fig. 25. The active silicon area is about 3.2 mm^2.

V. Conclusion

In this paper, a tri-mode DC-DC converter with temperature-independent LS, OWC, and ODC techniques achieves a maximum efficiency about 95% over an ultra-wide-load range from 0.1 mA to 500 mA. For SoC applications that is switched to sleeping mode at very light load condition or to high-speed mode at heavy load condition, a tri-mode DC-DC converter can automatically switch to optimum modulation mode, width of power MOS transistors, and power MOSFET turn-on and turn-off delays by a novel load sensor. Owing to the DSM technique, high efficiency can be maintained from heavy to light load current without efficiency drop between PWM and PFM modes. Furthermore, optimum width of power MOS transistors by the OWC technique and dead-times/ground bounce control by ODC technique not only raise efficiency from medium to light load current but also extend high efficiency to very light load current. Experimental results show high efficiency can be achieved by the tri-mode operation about 90% over a wide load current range from 3 mA to 500 mA. Because of effective mitigation of the switching loss contributed by optimum power MOSFET width and reduction of conduction loss contributed by optimum dead-times, the novel width and dead-time controllers improve efficiency to about 95% at heavy load condition and maintain the highly efficient performance to very light load current about 0.1 mA. The invention is very suitable for SoC applications.

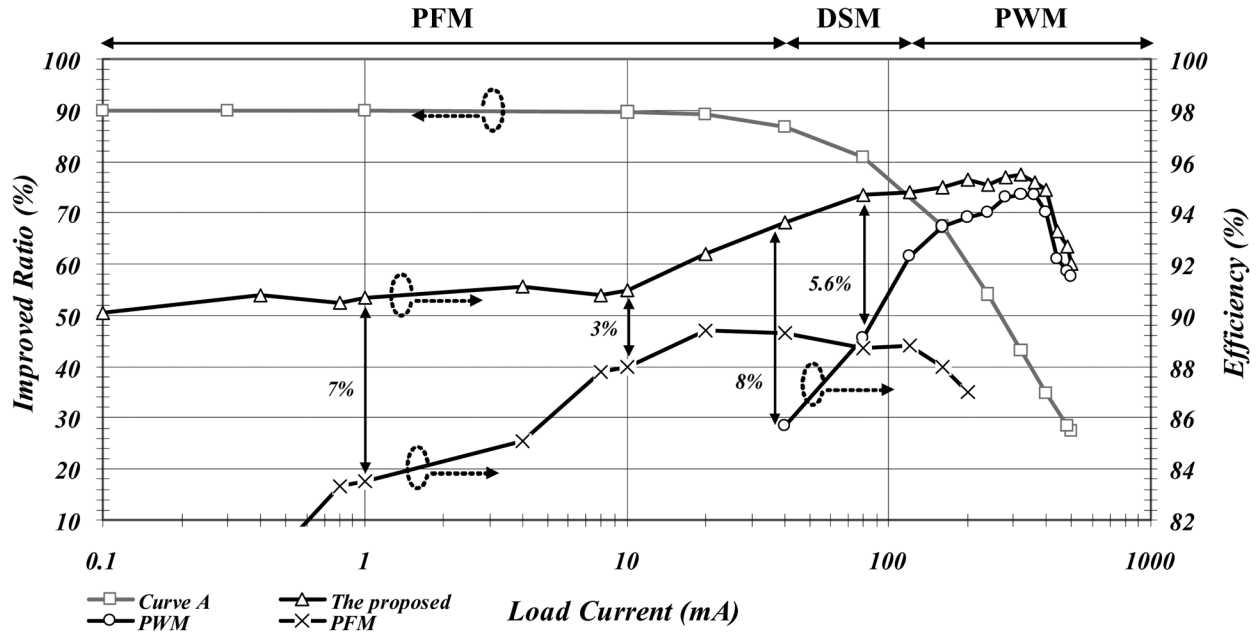

Fig. 24. Measured tri-mode converter efficiency and improved ratio of power consumption in driver and power MOSFET (load current changes from 0.1 mA to 500 mA).

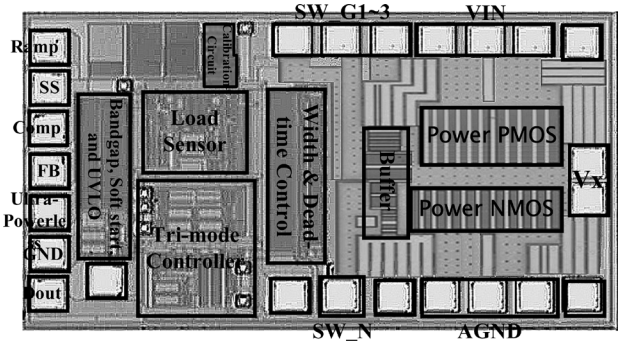

Fig. 25. Chip micrograph.

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