

Fast-Transient DC–DC Converter With On-Chip Compensated Error Amplifier

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Abstract—A fast-transient dc–dc converter with on-chip compensated error amplifier is presented in this paper. The error amplifier uses three transistors and one voltage follower to implement the on-chip current-mode Miller capacitor. Not only on-chip compensated error amplifier is implemented without off-chip components and I/O pins, but also fast-transient response is achieved. Moreover, we accurately decrease the transient response time without suffering from the oscillation issue. Implemented in a 0.35- μm CMOS process, experimental results demonstrate the stability of converters with a little area overhead about 5% larger than that of conventional design. In case of load variations, there is about four times reduction on the dropout voltage compared to that of conventional design. Furthermore, transient speed by our proposed technique is about five times faster than that of conventional control, while the total quiescent current is only increased about 3%.

Index Terms—Current-mode dc–dc converter, fast-transient response, on-chip compensation.

I. INTRODUCTION

AMONG the numerous requirements included in the ability to build high-performance system-on-chip (SOC) systems, the imperative demand is to supply a dynamic voltage in terms of the processing throughputs. It means that the dynamic voltage scaling (DVS) technique is the most popular power management technique for reducing power loss of SOC systems. Therefore, the design consideration for dc–dc converters with fast-transient response is necessary to provide good dynamic performance and simultaneously ensure the regulator's stability. In other words, fast-transient response techniques must make sure low supply voltage ripple and maintain a reliable supply voltage to SOC systems.

Switching frequency of dc–dc converters limit the bandwidth of switching dc–dc converters within 10%–20% of switching frequency. Thus, it is hard for us to design a switching dc–dc converter with high bandwidth. Besides, owing to the demand of large compensation capacitor C_C connected at the output of conventional error amplifier as shown in Fig. 1, the slewing

problem seriously affect the response time of switching dc–dc converters. Thus, the limited bandwidth and slewing problem deteriorate the load response of switching converters.

Therefore, most popular techniques [1], [2] are based on nonlinear control to source or sink recovery current within the limited bandwidth. However, these techniques are based on positive feedback control and have the possibility of oscillation. Pseudocontinuous conduction mode (Pseudo-CCM) buck converters [3] contain only one low-frequency single pole in the closed-loop transfer function. With PI compensation, the bandwidth can be extended but still limited within 10%–20% switching frequency. Thus, large time constant due to PI compensator still slows transient response time.

One popular fast-transient technique named as adaptive voltage position (AVP) [4] controlling technique modifies the reference voltage of error amplifier to obtain good transient response because of continuously maintaining constant output impedance of converters. As we know, it reduces the transient response time and output voltage ripple at the sacrifice of efficiency and load regulation. In addition to speed up the transient response of error amplifier, the skill of fast-response double buck converters (FRDBs) [5] is presented to reduce the recovery time of output voltage with an auxiliary converter. This technique increases the driving ability at the output of the dc–dc converters by nonlinear controlling techniques in case of large voltage variation. However, it needs two external inductors to implement double buck converters.

Recently, the end-point prediction [6] demonstrated fast-transient response when the reference voltage changes. In case of load variation, this technique doesn't have the ability to have fast-transient response because it suffers from large compensation capacitor at the output node of error amplifier. It means that it did not solve the slewing problem due to large compensation capacitor when load current changes.

In Fig. 1, a novel error amplifier with on-chip reconfigurable compensator substitutes for the conventional error amplifier to achieve fast-transient response in case of load variations. In other words, the proposed error amplifier not only contains on-chip but also achieves fast-transient response. In Section II, we describe the design of the proposed error amplifier. Experimental results are shown in Section III. Finally, we make a conclusion in Section IV.

II. DESIGN OF PROPOSED CIRCUITS

A. On-Chip Compensated Error Amplifier With Fast-Transient Controller

The schematic of proposed error amplifier is shown in Fig. 2. The current source is composed of transistors $M_{B1} \sim M_{B9}$ for biasing a cascade operational transconductance amplifier (OTA), which is a single-stage amplifier with a high gain and one dominant pole. The on-chip compensator is composed of

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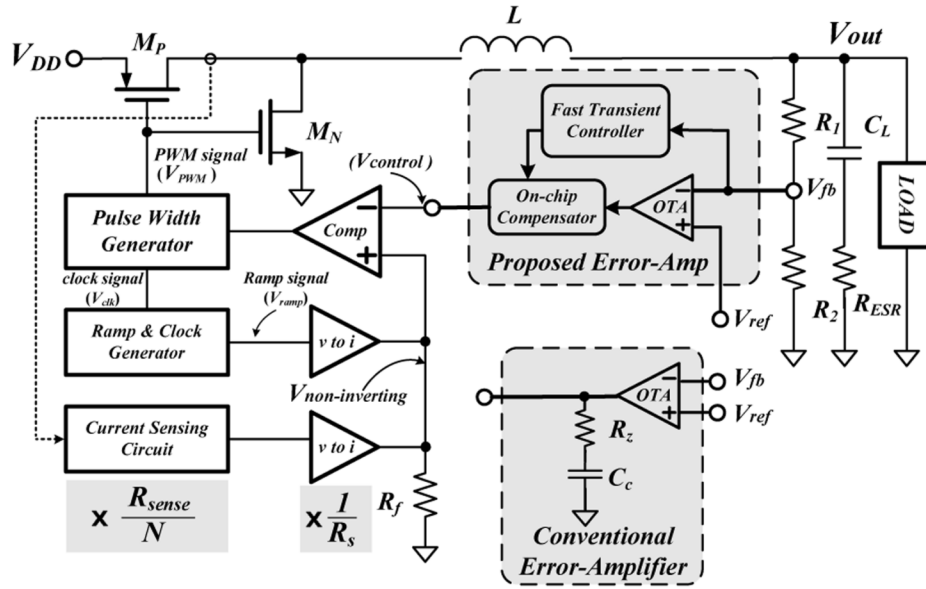


Fig. 1. On-chip compensated error amplifier with fast-transient technique substitutes for the conventional error amplifier in a buck converter.

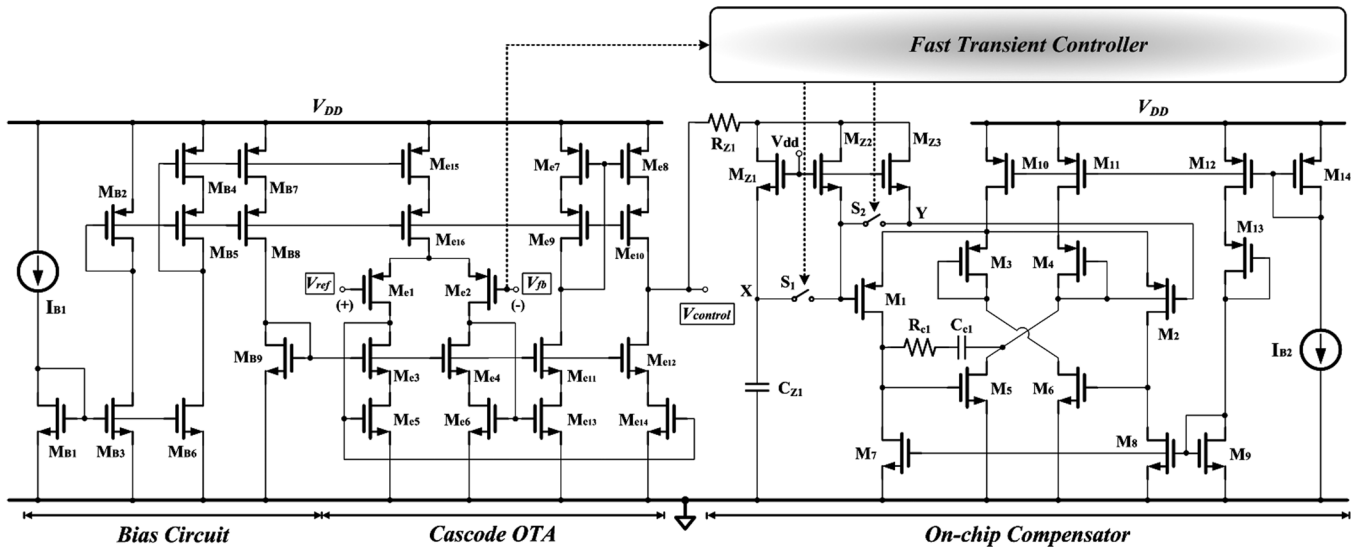


Fig. 2. Schematic of proposed fast-transient compensated error amplifier.

three transistors $M_{Z1\sim3}$, on-chip components (R_{z1}, C_{z1}) and a voltage follower $M_{1\sim14}$ [7]. According to theorem of current-mode Miller capacitance, an equivalent current source connected to the two terminals of the small capacitor has a current k times that of flowing through the small capacitor. In Fig. 2, voltage follower forces the voltage of *node Y* when switch S_1 is off and switch S_2 is on. Three transistors M_{Z1}, M_{Z2} , and M_{Z3} , which operate in linear-region and constitute two parallel on-resistances, have the same large gate–source voltage and small drain–source voltage. One on-resistance is decided by transistor M_{Z1} and the other on-resistance is decided by the parallel transistors $M_{Z2\sim3}$. The values of these two parallel on-resistances are inversely proportional to their respective aspect ratios and shown as

$$r_{ds} \approx \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{tn})}. \quad (1)$$

In order to generate a current that is k times larger than the current flowing through a small capacitor C_{z1} , the sum of the aspect ratio of M_{Z2} and M_{Z3} is set k times that of M_{Z1} . Hence, the equivalent driving current flowing through capacitor C_{z1} is boosted by a factor of $(k + 1)$. In other words, the equivalent capacitance is multiplied by a factor of $(k + 1)$ and is equivalent to a large off-chip capacitor.

The output capacitor of the error amplifier needs to be charged or discharged as fast as possible for sudden load variations. Thus, when switch S_1 is on and switch S_2 is off the equivalent current is divided into two parts. One part current $I_{M_{Z2}}$ is utilized to charge or discharge the small capacitor C_{z1} . The other part current $I_{M_{Z3}}$ is utilized to compensate the dc–dc converters.

The detector and fast-transient control circuit in Fig. 3 is used to react to load current suddenly changing from low to high, or vice versa. In order to accurately detect the load variation, the fast-transient control circuit needs two one-shot circuits to get optimum transient response time. The operation of the output voltage detector (OVD) is described as following: $M_{S1\sim3}$ and

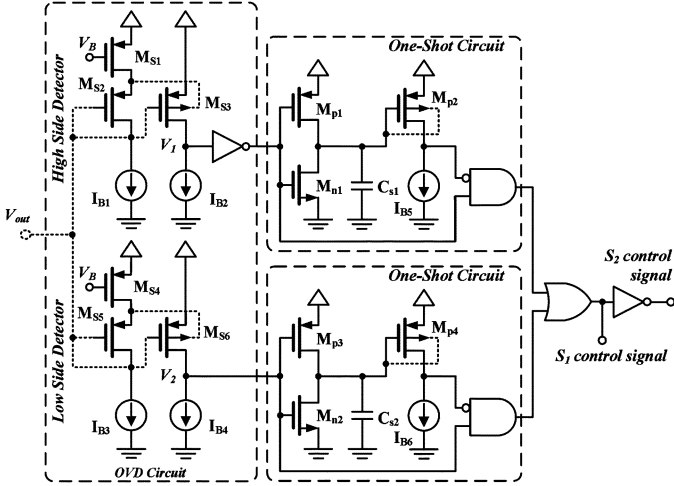


Fig. 3. Detective and control circuit for fast-transient response.

$I_{B1,2}$ are in response to detect the condition that V_{out} is larger than the desired voltage when load current suddenly changes from heavy to light. $M_{S4\sim6}$ and $I_{B3,4}$ are used to detect the load current from light to heavy. In steady state operation, the current $I_{MS3}(I_{MS6})$ is larger (smaller) than the $I_{B2}(I_{B4})$ due to the aspect ratio of transistor M_{S3} is larger than that of transistor M_{S6} . The value of node $V_1(V_2)$ stay at a high (low) voltage level if the variation of output voltage V_{out} is not large enough to trigger OVD circuit to generate one-shot pulse.

Once load current decreases (increases) rapidly and cause V_{out} to pull high (drop down), then it results in decreasing (increasing) gate-source voltage and increasing (decreasing) threshold voltage for transistor $M_{S3}(M_{S6})$ because of the modulation voltage between body and source. According to current equation of MOS transistor operating in saturation region, current $I_{MS3}(I_{MS6})$ drastically shrinks to a smaller (larger) value than that of current $I_{B2}(I_{B4})$. Consequently, voltage $V_1(V_2)$ is pulled down (up) to trigger a one-shot pulse for switching the normal operation mode to the fast-transient mode. Proper adjustment of bulk-source voltage V_{BS} can eliminate the possibility of leakage current between source and bulk nodes. When one-shot circuit switches the normal operation mode to the fast-transient mode for a short time, the proposed error amplifier in Fig. 2 has a large current to charge or discharge the small output capacitor C_{z1} ; meanwhile, the transconductance of the proposed error amplifier is increased from $g_{m,n}$ to $g_{m,f}$.

The transconductance in the normal operation mode $g_{m,n}$ is shown as the following equation when the tail current of the error amplifier is I_D :

$$g_{m,n} = \sqrt{2\mu_p C_{ox} \left(\frac{W}{L}\right)_{Me1,2} I_D} \times \frac{\left(\frac{W}{L}\right)_{Me14}}{(k+1)\left(\frac{W}{L}\right)_{Me5}}. \quad (2)$$

The transconductance in the fast-transient mode is increased from $g_{m,n}$ to $g_{m,f}$, which is shown as

$$g_{m,f} = g_{m,n} + g_{m,n} \times mk = g_{m,n}(1 + mk) \quad (3)$$

where m is the ratio of I_{Mz2} to I_{Mz3} and k is the factor of Miller multiplication. The steeper the slope $g_{m,f}$ is, the less the recovery time of the on-chip error amplifier is. The appropriate values of m and k are set to 0.5 and 100 for this on-chip compensated error amplifier. Larger value of the product mk

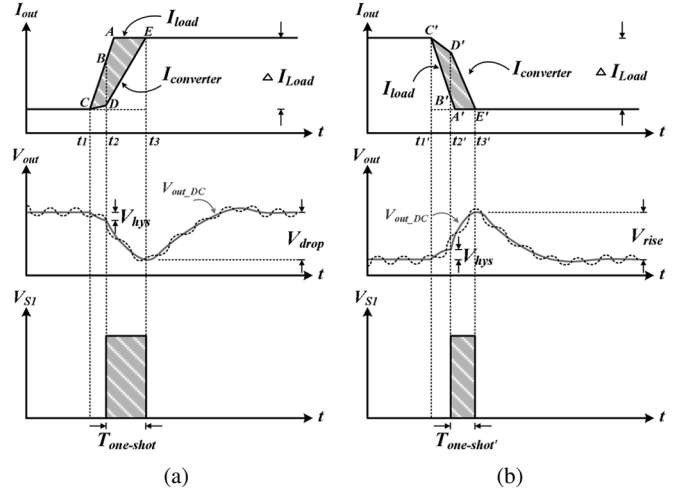


Fig. 4. Timing analysis of signal waveforms: (a) with a positive and sudden load current variation, and (b) with a negative and sudden load current variation.

may make the system unstable and oscillation may occur at the output. Thus, a conservative value is selected for our implementation.

B. Timing Analysis of Fast-Transient Control

An appropriate $T_{one-shot}$ time [8] can speed up the transient response and reduce the output voltage ripple significantly. Fig. 4 shows the waveforms of the transient response when load current I_{load} has a sudden load current change ΔI_{Load} . Within the bandwidth smaller than 20% switching frequency, the averaged model [9] is used to analyze the characteristics of transient response. For a sudden large load, the insufficient charge between the current $I_{converter}$ and I_{load} from time t_1 to t_3 is supplied by the output capacitor C_L . The current $I_{converter}$ increases with a slow slope dI_{DC}/dt in normal operation. Once the fast-transient controller is triggered, it increases the slope of $I_{converter}$ from dI_{DC}/dt to dI_{ED}/dt . The slopes dI_{DC}/dt and dI_{ED}/dt are proportional to the transconductances $g_{m,n}$ and $g_{m,f}$ of the error amplifier, respectively. The optimum duration time of $T_{one-shot}$ is determined when the value of $I_{converter}$ is slightly larger than that of the load current because the energy is sufficient to supply the load and V_{out} stops dropping after time t_3 . The duty of switching signal is rapidly increased by the fast-transient controller. The new proposed technique can have better performance than that of slew-rate enhancement (SRE) [1] because the output capacitor C_{z1} of the error amplifier is a small capacitor, which needs short charging/discharging time [10].

The fast-transient controller is started to speed up the increasing rate of $I_{converter}$ at time t_2 . From time t_2 to t_3 , the non-inverting input terminator of comparator in Fig. 1 is expected to rise to a stable voltage, which can be decided by the current-sensing circuit and $V-I$ converter [11]. When the output is stable, the voltage variation of the noninverting input terminator of comparator is given by

$$\Delta V_{noninverting} = \frac{\Delta I_{Load}}{N} \times \frac{R_{sense} R_f}{R_s} \quad (4)$$

where N is current sensing ratio, R_{sense} is the current sensing resistor, R_f is the resistor for converting current to voltage, and R_s is the resistor in the $V-I$ converter [11].

Once the fast-transient controller triggers a one-shot pulse, the error amplifier only needs to raise the voltage of the inverting input terminator to $\Delta V_{\text{control}}$ described as (5). The second term in (5) stands for the voltage drop corresponding to V_{hys} before starting the fast-transient operation. $|T(j\omega)|$ is the magnitude of error amplifier's transfer function in normal operation mode

$$\Delta V_{\text{control}} = \Delta V_{\text{non-inverting}} - \frac{V_{\text{hys}} |T(j\omega)| R_2}{R_1 + R_2}. \quad (5)$$

The small capacitor C_{z1} is charged by an average current I_{fast} for a period of $T_{\text{one-shot}}$ when the fast-transient controller increases the transconductance from $g_{m,n}$ to $g_{m,f}$. The increasing charge of the output capacitor C_{z1} and average current I_{fast} are given as

$$C_{z1} \times V_{\text{control}} = T_{\text{one-shot}} \times I_{\text{fast}} \quad (6)$$

$$I_{\text{fast}} = \frac{1}{2} (V_{\text{drop}} + V_{\text{hys}}) \frac{R_2}{R_1 + R_2} g_{m,f}. \quad (7)$$

According to (3), the period of $T_{\text{one-shot}}$ for fast-transient operation can be derived as

$$T_{\text{one-shot}} = \frac{2C_{z1} \Delta V_{\text{control}} (R_1 + R_2)}{g_{m,n} (1 + mk) (V_{\text{drop}} + V_{\text{hys}}) R_2}$$

$$T'_{\text{one-shot}} = \frac{2C_{z1} \Delta V_{\text{control}} (R_1 + R_2)}{g_{m,n} (1 + mk) (V_{\text{rise}} + V_{\text{hys}}) R_2}. \quad (8)$$

$T'_{\text{one-shot}}$ is the case of large negative load as shown in Fig. 4(b) for fast-transient operation. Before time t_1 , the output voltage level is slightly lower than the desired voltage because the dc-dc converter is working in the heavy load. Thus, it needs to wait more time than the case of Fig. 4(a) for triggering the fast-transient controller. In other words, $T'_{\text{one-shot}}$ is smaller than $T_{\text{one-shot}}$.

C. Analytic Pole-Zero Pair of the On-Chip Compensated Error Amplifier

The equivalent resistances of two parallel resistances generated by three transistors $M_{Z1 \sim 3}$ working in triode region are modeled as two resistances R and KR . R is the equivalent resistance of transistors M_{Z1} , and KR is the equivalent resistance of parallel transistors M_{Z2} and M_{Z3} . A careful effort on symmetrical layouts of $M_{Z1 \sim 3}$ can improve the mismatching problem.

Due to the switch frequency of the dc-dc buck converter is designed at 500 kHz, the unity gain frequency is designed below 20% switching frequency. Thus, we model the voltage follower as a transfer function with only one dominant pole at ω_{P1} . The transconductance of this voltage follower is g_{m0} . As a result, the transfer function of the voltage follower is shown as (9)

$$G_m(s) \approx \frac{g_{m0}}{1 + \left(\frac{s}{\omega_{P1}}\right)}. \quad (9)$$

Furthermore, the output equivalent impedance of voltage follower can be derived as

$$Z_{\text{out}} = \left(\frac{R_{C1} + r_{o1}}{1 + g_{m5} r_{o1}} + \frac{1}{sC_{C1}(1 + g_{m5} r_{o1})} \right) \parallel r_{o2} \quad (10)$$

where C_{C1} and R_{C1} are the Miller compensation capacitor and resistor, respectively. g_{m5} is the transconductance of the second stage in the voltage follower. Besides, the output impedance of

TABLE I
SPECIFICATIONS OF BUCK CONVERTER

Technology		TSMC 0.35- μm process			
Input Voltage		3.3 V			
Output Voltage		2.0 V			
Switching frequency		500 kHz			
Output Current Range		< 400 mA			
Output Ripple Voltage		< 10 mV			
Output recovery time		< 25 μs			
L	4.7 μH	R_l	300 $\text{k}\Omega$	R_{sense}	400 Ω
C_L	10 μF	R_2	100 $\text{k}\Omega$	R_s	50 $\text{k}\Omega$
R_{BSR}	30 $\text{m}\Omega$	R_{z1}	1 $\text{M}\Omega$	R_f	95 $\text{k}\Omega$
V_{ref}	0.5 V	C_{z1}	20 pF	K	100
M	0.5	N	1000		

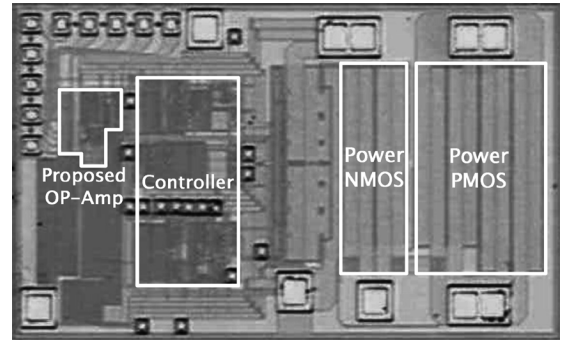


Fig. 5. Micrograph of the on-chip compensated error amplifier for fast-transient response dc-dc buck converter.

first stage and second stage of this operational amplifier are r_{O1} and r_{O2} .

The transfer function of on-chip compensator is written as

$$T(s) \approx -g_m R_o \frac{1 + sKC_{z1}R_{z1}}{1 + sKC_{z1}(R_{z1} + R_o)}. \quad (11)$$

Because the value of R_o is such larger than R_{z1} , the value of low-frequency pole is lower than that of the low-frequency zero by this proposed on-chip compensator and they are described as

$$\text{Zero} \approx \frac{1}{KC_{z1}R_{z1}} \text{ and Pole} \approx \frac{1}{KC_{z1}R_o}. \quad (12)$$

Obviously, the proposed on-chip current-mode Miller capacitor can work correctly as a large off-chip capacitor. The analytic results show the correctness of the equivalent low-frequency pole-zero pair and implementation of the proportional-integral (PI) compensation in dc-dc converters.

III. EXPERIMENTAL RESULTS

The fast-transient response dc-dc converter with on-chip compensated error amplifier is implemented with TSMC 0.35- μm process. Specifications of the dc-dc converter are listed in Table I. The micrograph of proposed circuit is shown in Fig. 5.

For demonstrating the fast-transient response, the load current changes from 100 to 400 mA and back to 100 mA with rising time and falling time of 4 μs . In Fig. 6, curve (a) illustrates the conventional error amplifier with external compensation resistor and capacitor. This curve needs about 100 μs

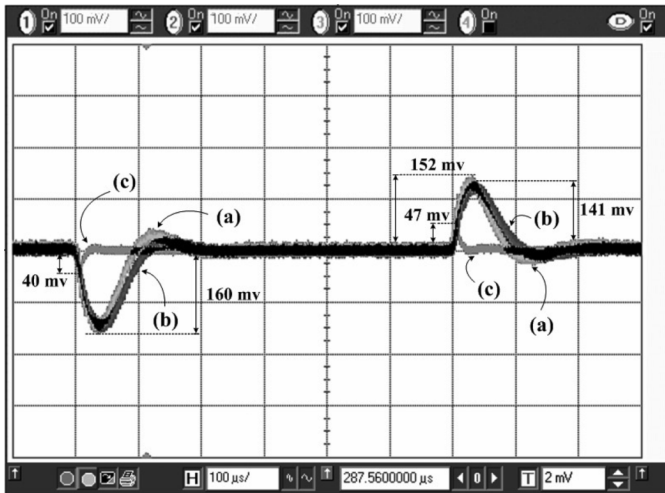


Fig. 6. Load transient response with load current step between 100 and 400 mA. (a) Dropout voltage is 160 mV and overshoot voltage is 152 mV by conventional error amplifier. (b) Dropout voltage is 160 mV and overshoot voltage is 141 mV by on-chip compensated error amplifier without fast-transient controller. (c) Dropout voltage is 40 mV and overshoot voltage is 47 mV by on-chip compensated error amplifier with fast-transient controller.

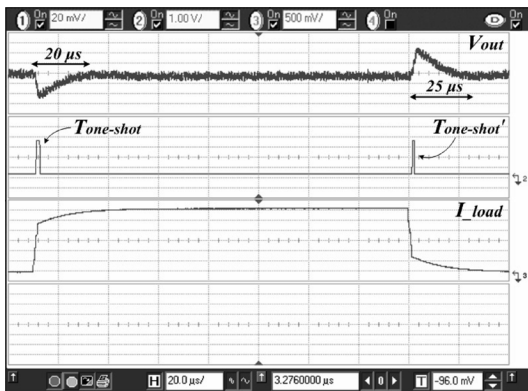


Fig. 7. Enlarged waveforms of transient response with proposed error amplifier.

to stabilize the large load current variation from low to high, or vice versa. Curve (b) is the result of the on-chip compensated error amplifier without fast-transient controller. Owing to the same compensated pole-zero pair, the transient response is nearly the same as that of curve (a). Curve (c) shows the result of the on-chip compensated error amplifier with fast-transient mechanism. It has the minimum recovery time and the enlarged waveforms are shown in Fig. 7. The proposed amplifier only needs less than 25 μs to recover the output voltage to a stable voltage level when load current changes. The reason why the output voltage level of error amplifier can be recovered rapidly is benefited from an auxiliary current that is mk times the value of original current.

Moreover, experimental results also prove the correctness of timing analysis of fast-transient control. By (8), $T_{\text{one-shot}}$ and $T_{\text{one-shot}'}$ are 2.65 μs and 2.23 μs , respectively. From Fig. 7, $T_{\text{one-shot}}$ and $T_{\text{one-shot}'}$ are 2.85 and 2.28 μs , respectively. The error percentage for load suddenly changing from low to high and high to low are only 7.23% and 2.54%, respectively. These values slightly deviate from analytic values because of process, temperature and supply voltage variations. Thus, in order to avoid the converter from oscillating, we use conservative value of one-shot timing values to make sure the stability of the system.

IV. CONCLUSION

A novel dc-dc converter with on-chip compensated error amplifier and fast-transient mechanism is presented in this paper. The error amplifier uses an on-chip reconfigurable Miller capacitor to improve the transient response at an accurate one-shot time. Experimental results demonstrate the transient speed by our proposed technique is faster than conventional control by about five times, and there is about four times reduction on the dropout voltage compared to that of conventional design. With the proposed error amplifier, the transient response of dc-dc converters is improved significantly.

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