A traffic shaper for supporting CBR and VBR services in ATM networks

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Abstract

The proposed ATM traffic shaper consists of a regulator and a scheduler. It can shape multiple incoming CBR and VBR cell streams simultaneously. The impact of cell emission conflicts is considered and resolved by using an earliest-due-date (EDD) scheduler. In addition, for VBR services, there exists a feedback signal from the EDD scheduler to the regulator. It guarantees that the shaped VBR streams always conform to the GCRA-based traffic descriptor when the cells depart for the ATM output link. Both the cell delay bounds and the call admission control (CAC) conditions for assuring shaper performance are derived. With our CAC mechanism, this traffic shaper can operate with no jitter violation for CBR cells and provide a predictable overall delay bound for VBR cells, and the derived bounds of the proposed traffic shaper are tight for both CBR and VBR. © 2000 Elsevier Science B.V. All rights reserved.

Keywords: Traffic shaper; CBR; VBR; ATM; EDD; Traffic descriptor

1. Introduction

Since traffic management became an important topic in the ATM research arena, many traffic shapers or cell spacing devices have been proposed to reduce the burstiness of the traffic streams [1–11]. The concept of a traffic shaper or cell spacer is to store the input cells in a buffer and then output them at eligible times. Usually, the best eligible time for cell emission is directly related to the desired output traffic pattern. Such desired traffic patterns may be in many forms in various designs. In [1–3], traffic shapers or cell spacers are designed according to the so-called virtual-scheduling algorithm to reduce the cell delay variation due to queueing in multiplexing nodes. In [4], Brochin employs a cell spacing device to prevent any two successive cells from being transmitted within a very short interval. In [5], traffic

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shapers are used to output cells at a rate lower than the peak input rate. Traffic shaping is implemented by a sliding window mechanism followed by a peak bit rate reduction mechanism in [6]. In [7,8], the concept of a multiple level shaping algorithm is introduced. In the latter design, the cell emission rate is determined by the buffer occupancy level of the shaper so that overall performance can be improved. Another similar traffic shaper design which resembles RC circuit behavior is proposed in [9]. In [10], a rate-controlled static-priority (RCSP) server which consists of two components: a rate-controller and a static-priority scheduler, is proposed to correct the distortion of traffic pattern introduced by the previous network nodes. Furthermore, in order to shape cell streams to strictly follow the GCRA traffic descriptor [12], a VBR traffic shaper is proposed and analyzed in [11].

In most of these papers, e.g. [1,5,8,10], the assumed models include multiple traffic streams passing through separate spacing devices and a second-stage multiplexer before cell emission. If two cells from different connections are assigned the same eligible time to enter the multiplexer to be emitted, then the cell emission conflict occurs. Since the impact of the multiplexer on the output traffic is usually not taken into account, the output cell streams may not conform to the desired traffic descriptor due to cell conflicts within the multiplexer, regardless of the fact that the cell streams observed at the output of spacing devices do conform. For example, such emission conflicts can lead to unnecessary peak cell rate violations or undesirable cell delay jitter when cells are transmitted to the ATM output link. It reveals that the multiplexer should be modeled as a component of the traffic shaper such that the impact of cell output conflicts can be resolved. In [13], Shiomoto and Yamanaka proposed a cell spacer architecture that can resolve the cell emission conflicts and support multiple traffic classes. In this design, the cell spacer can only regulate the peak cell rate successfully, but other traffic descriptors such as the sustainable cell rate and the burst tolerance (or maximum burst size) are not considered. In [11], we proposed a design that employs such discipline so that multiple VBR streams can be shaped and their peak cell rate, sustainable cell rate, and burst tolerance are kept in conformance simultaneously for each connection. Nevertheless, we find the design of an ideal ATM traffic shaper is yet to be completed, because all ATM services need to be supported. For example, none of the aforementioned shaper designs are specifically targeted to support the increasingly important CBR services, which are expected to play a key role in many voice-over-ATM applications. In order to support CBR applications with strict timing requirement, such as circuit emulation, the cell delay jitter can be a more important traffic parameter than those GCRA-based parameters defined by the ATM Forum [12], and is also difficult for traffic shaping. How to handle these two types of traffic streams, CBR and VBR, which have totally different traffic characteristics in one traffic shaper, has thus become a challenging issue.

In this paper, we propose an ATM traffic shaper which can shape multiple CBR and VBR traffic streams simultaneously to be conforming, with respect to each connection's own traffic descriptor, when their cells enter the ATM output link. The conformance requirement for CBR cell streams is to have all cell delay jitter to be within predefined constraints, while the conformance requirement for VBR cell streams follows the GCRA traffic descriptor. The CBR traffic streams are granted higher priority for cell emissions in the shaper than the VBR streams. We will then derive the call admission control (CAC) conditions to guarantee the shaper performance and analyze the overall shaping delay bound later.

The organization of this paper is as follows. In Section 2, the traffic model is defined. In Section 3, we describe the design of the proposed traffic shaper. In Section 4, the delay bounds and the CAC conditions of the proposed traffic shaper are derived. In Section 5, the proposed traffic shaper is demonstrated by numerical examples. Next, we delineate the implementation issues in Section 6, and finally in Section 7, we present our conclusions.

2. Traffic model

We define two traffic descriptors to describe the different characteristics of VBR and CBR traffic, respectively.

VBR traffic descriptor. The concept of a GCRA-based traffic contract described in the ATM Forum UNI Specification [12] is used to define the traffic descriptor (X^v, T^v, τ^v) for each VBR connection. Here, X^v indicates the minimum cell interarrival time, which corresponds to the peak cell rate parameter, and T^v represents the minimum average cell interarrival time. Note that the inverse of T^v is equivalent to the sustainable cell rate. The burst tolerance τ^v is the maximal amount of time by which the actual cell arrival is allowed to be earlier than the cell arrival time theoretically predicted, under the assumption that any two consecutive cells are separated by the interval T^v. The latter burst tolerance parameter τ^v is identical to that defined in Forum's GCRA definition [12]. In other words, the traffic descriptor (X^v, T^v, τ^v) indicates the following traffic characteristics of a cell stream: regarding the sustainable cell rate, the cell stream conforms to GCRA (T^v, τ^v); when the peak cell rate is concerned, the cell interarrival time is strictly larger or equal to X^v, i.e., conforms to GCRA $(X^v, 0)$. Since the proposed traffic shaper can shape traffic streams to conform to the GCRA-based traffic descriptors, we call it a GCRA-based traffic shaper. Note that this VBR traffic descriptor assumes no strict timing requirement for its applications.

CBR traffic descriptor. For each CBR connection, the traffic descriptor (T^c, τ^c) is employed. T^c is the inverse of the constant cell rate. τ^c is the maximum tolerable jitter which is defined as follows:

$$\tau^c \equiv \max_{\forall m \neq n} \{|A(m) - A(n) - (m - n)T^c|\}, \tag{1}$$

where $A(m)$ is the arrival time of the mth cell. Eq. (1) indicates that a CBR cell can never arrive earlier or later than its predicted arrival time by τ^c. Notably, such traffic descriptors should satisfy the need of constant rate applications with strict timing requirement.

In the rest of this paper, the number of active CBR connections and the number of active VBR connections are denoted as K_c and K_v, respectively. The input traffic descriptor and the desired output traffic descriptor of the ith CBR connection are represented as $(\tilde{T}_i^c, \tilde{\tau}_i^c)$ and (T_i^c, τ_i^c), respectively, where $\tilde{T}_i^c = T_i^c$ should hold for $i = 1, \ldots, K_c$ in order to maintain the provisioned constant cell rate. The input traffic descriptor and the desired output traffic descriptor of the jth VBR connection are specifically specified as $(\tilde{X}_j^v, \tilde{T}_j^v, \tilde{\tau}_j^v)$ and (X_j^v, T_j^v, τ_j^v), respectively, where $\tilde{T}_j^v \geq T_j^v$ for $j = 1, \ldots, K_v$. Alternatively, we also call the jth CBR (VBR) connection as the CBR-j (VBR-j) connection.

3. ATM traffic shaper

3.1. Traffic shaper model

In this section, we propose a new traffic shaper model which consists of two components: a regulator and a scheduler, as shown in Fig. 1. The regulator consists of multiple CBR and VBR departure controllers. Each departure controller stores and forwards the cells of one connection (VP or VC) according to its individual output traffic descriptor. The operation of the traffic shaper follows a discrete time-axis, on which the normalized cell transmission time is used as a time slot. If a cell arrives early, the regulator will stop it in the buffer. The cell then enters the scheduler at its eligible time. The scheduler is
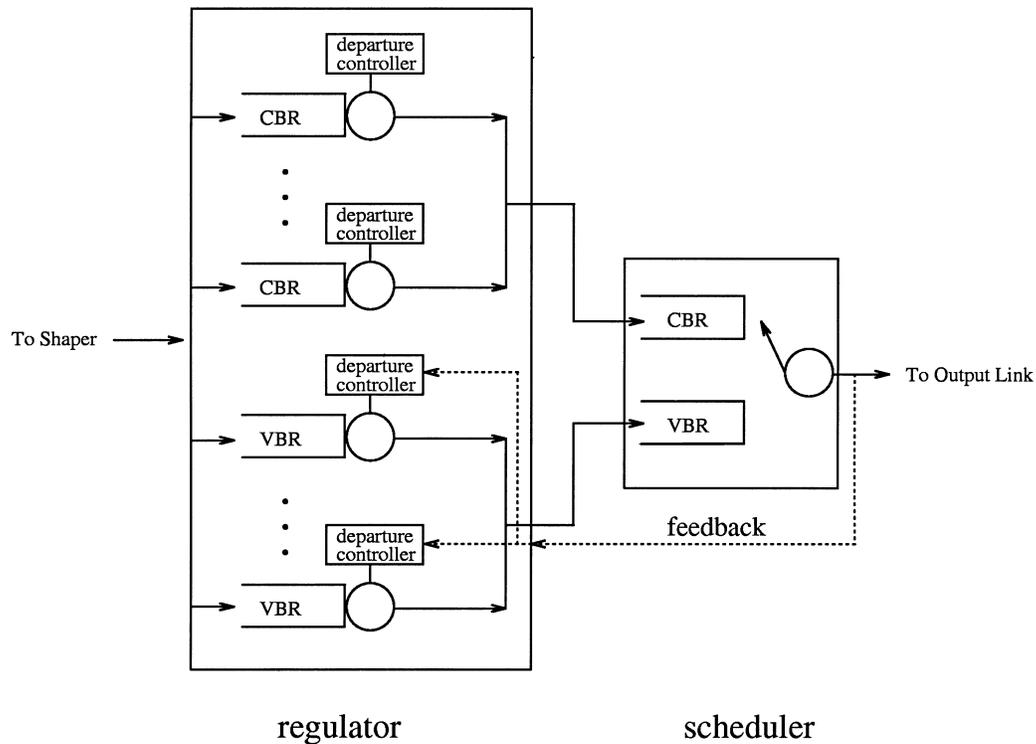
Fig. 1. The model of the ATM traffic shaper.

responsible for resolving emission conflicts among cells from different connections. It consists of two earliest-due-date (EDD) queues [14], one for CBR and one for VBR cells, respectively. In addition, non-preemptive priority is granted to CBR cells. Hence, VBR cells have lower service priority. The scheduler processing time is one slot so that the sojourn time at the scheduler for any cell is at least one slot.

In order to prevent the VBR cell emissions from violating the peak cell rate constraint even under emission conflicts, there exists a feedback signal from the scheduler to the GCRA mechanism within the regulator. The calculation of the eligible time of the next cell emission on the same VBR connection is always done after the receipt of the feedback signal triggered by the current emission. This approach assures that the calculated eligible time for next VBR cell emission always satisfies the GCRA-based traffic descriptor. As a result, there will be at most one cell in the scheduler for each VBR connection at any time.

Meanwhile, no peak cell rate parameters are specified in the CBR traffic descriptors and constant cell rates must be maintained for all CBR services. Hence, we do not stop the operation of CBR departure controllers in the regulator under cell emission conflicts as in the VBR case, and no feedback signal is required between the scheduler and the CBR departure controllers. Regarding the delay jitter constraint specified in the CBR traffic descriptor, it can be met by employing a CAC mechanism. Under such a design, the number of cells for each CBR connection in the scheduler may be larger than 1, but the total number of cells at the scheduler should still be smaller under this CAC mechanism.

The proposed traffic shaper model resembles that presented in [10]. However, the proposed traffic shaper ensures that the output cell streams of the *scheduler* always conform to their respective traffic descriptors, while the RCSP server in [10] does not. In addition, the proposed traffic shaper in this paper can shape the traffic stream to conform to a better traffic descriptor, while the RCSP server can only preserve the original traffic pattern. Thus, we think that a RCSP server is not powerful to operate as a traffic shaper.

3.2. Algorithm in the regulator

In order to describe the shaping algorithm in the regulator in detail, some control variables for shaped connections are defined as follows. For the jth CBR or VBR connection, the kth cell arrives at the shaper (or regulator) at time $A_j(k)$ and is buffered until the eligible time $ET_j(k)$ before it enters the scheduler. It is then given an initial due-date $IDD_j(k)$ when it enters the scheduler. The target time for this cell to leave the scheduler is called the theoretical departure time $TDT_j(k)$. However, the time epoch when it leaves the scheduler could be different. We call the latter epoch the actual departure time, and denote it as $ADT_j(k)$. Note that the variables $A_j(k)$, $ET_j(k)$, and $ADT_j(k)$ are integers, while $TDT_j(k)$ and $IDD_j(k)$ may not be. During the operation of the traffic shaper, these variables are calculated by the following iterative forms.

Case A (Iterative form for VBR-j connection).

$$TDT_j(k) = \max\{ADT_j(k-1), TDT_j(k-1)\} + T_j^{\text{v}}, \tag{2}$$

$$ET_j(k) = \max\{ADT_j(k-1) + \lceil X_j^{\text{v}} \rceil - 1, \lceil TDT_j(k) - \tau_j^{\text{v}} \rceil - 1, A_j(k)\}, \tag{3}$$

$$IDD_j(k) = \max\{TDT_j(k) - ET_j(k), \delta_j^{\text{v}}\}, \tag{4}$$

with initial values $TDT_j(1) = A_j(1)$, $ET_j(1) = A_j(1)$, and $IDD_j(1) = \delta_j^{\text{v}}$, where δ_j^{v} is the minimal initial due-date, given by $\delta_j^{\text{v}} = \min\{T_j^{\text{v}} - \lceil X_j^{\text{v}} \rceil + 1, \tau_j^{\text{v}}\}$.

To illustrate detailed operation, we first consider a specific VBR connection, say VBR-j. When the kth cell arrives at the regulator, $TDT_j(k)$ is not determined until the feedback signal triggered by the departure of the $(k-1)$th cell is received. $TDT_j(k)$ is then set to $\max\{ADT_j(k-1), TDT_j(k-1)\} + T_j^{\text{v}}$ so that it meets the output sustainable cell rate constraint of VBR-j. In order to guarantee that the output cell stream will conform to $(X_j^{\text{v}}, T_j^{\text{v}}, \tau_j^{\text{v}})$, the kth cell cannot enter the scheduler earlier than either the time epoch $ADT_j(k-1) + \lceil X_j^{\text{v}} \rceil - 1$ or $\lceil TDT_j(k) - \tau_j^{\text{v}} \rceil - 1$; otherwise, it might violate the peak cell rate constraint or the burst tolerance constraint, respectively. By taking account of the fact that a cell can never enter the scheduler before it arrives at the regulator, eligible time can be expressed as Eq. (3). Actually, Eq. (3) implies that a cell is allowed to enter the scheduler as early as possible. Thus, such an implementation strategy can be called the *most greedy method* (MGM). Under ideal operation conditions, the maximal throughput of all connections should be maintained with the use of the traffic shaper. This requires that no cell losses occur in the scheduler and all cells are emitted before their theoretical departure times. The first requirement can be easily met by allocating M buffers for VBR cells at the scheduler, where M is the maximal number of VBR connections that the shaper supports. To satisfy the second requirement, appropriate initial due-dates must be assigned. The difference between $TDT_j(k)$ and $ET_j(k)$ is used as the preliminary initial due-date whenever the shaper is non-empty with

respect to VBR-j. From (2) and (3), it can be shown that $TDT_j(k) - ET_j(k)$ is never smaller than δ_j^v unless $ET_j(k) = A_j(k)$. The proof is left to the reader. The final initial due-date, as given by Eq. (4), is set to be the maximum of the preliminary initial due-date $TDT_j(k) - ET_j(k)$ and the minimal initial due-date δ_j^v. The latter δ_j^v is used to fairly resolve cell emission conflicts, reduce scheduling delay bounds, and to improve the shaper utilization under the CAC mechanism. We set $\delta_j^v = \min\{T_j^v - \lceil X_j^v \rceil + 1, \tau_j^v\}$ so that overdue events for other VBR connections caused by immediate emission of cells with $ET_j(k) = A_j(k)$ can be minimized. From (2) to (4), it can be shown that $IDD_j(k)$ satisfies $\tau_j^v + 1 \geq IDD_j(k) \geq \delta_j^v$.

Case B (Iterative form for CBR-j connection).

$$TDT_j(k) = TDT_j(k-1) + T_j^c, \tag{5}$$

$$ET_j(k) = \max\{\lceil TDT_j(k) - \tau_j^c \rceil - 1, A_j(k)\}, \tag{6}$$

$$IDD_j(k) = TDT_j(k) - ET_j(k), \tag{7}$$

with initial values $TDT_j(1) = A_j(1) + p_j + \tau_j^c + 1$, $ET_j(1) = A_j(1) + p_j$, and $IDD_j(1) = \tau_j^c + 1$, where p_j is an integer which satisfies $\tilde{\tau}_j^c \geq p_j \geq \max\{0, \tilde{\tau}_j^c - \tau_j^c\}$.

From Eqs. (5) to (7), one can show that the minimum initial due-date cannot be less than $\delta_j^c = \min\{\tau_j^c, p_j - \tilde{\tau}_j^c + \tau_j^c + 1\}$, and $IDD_j(k)$ satisfies $\tau_j^c + 1 \geq IDD_j(k) \geq \delta_j^c$. The shaping algorithm for a CBR connection is very similar to that of a VBR connection. Since the theoretical departure time should be equally separated by the constant interval T_j^c for the jth CBR connection, one obtains Eq. (5). Moreover, no peak rate parameter is defined for CBR connections, so $ET_j(k)$ is given by Eq. (6). The design parameter p_j is used to meet the delay jitter constraint and guarantee that the minimal initial due-date is not less than 1. How p_j should be selected is an engineering issue and is elaborated in Section 5.

3.3. Algorithm in the scheduler

After the kth cell of the jth CBR or VBR connection enters the buffer of the scheduler, its *instantaneous due-date* at time t, denoted as $DD_j(k, t)$, is calculated as follows:

$$DD_j(k, ET_j(k)) = IDD_j(k), \tag{8}$$

$$DD_j(k, t+1) = \max\{DD_j(k, t) - 1, 0\} \quad \text{for } t \geq ET_j(k). \tag{9}$$

If $DD_j(k, t) = 0$, it maintains the value zero from t on. We say that a cell is *overdue* if its due-date is zero and still resides at the scheduler.

In the scheduler, the EDD service discipline is employed in each queue (CBR and VBR) to minimize the number of overdue events [14]. The cell with the smallest due-date is emitted first. If multiple cells have equal due-date, they are emitted in FIFO order. Fig. 2 shows one sample-path of the control variables associated with a specific VBR connection.
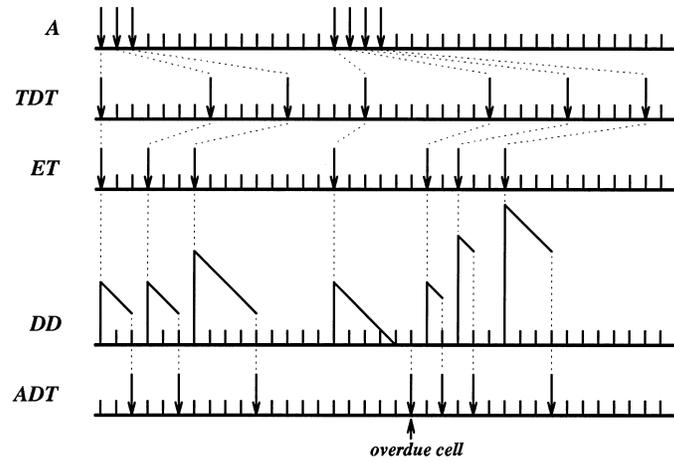
Fig. 2. Sample-path of a specific VBR connection with traffic descriptor $(X, T, \tau) = (2, 5, 8)$.

4. Performance analysis

The performance analysis consists of three parts. We first derive the scheduling delay bounds for both CBR and VBR services. The scheduling delay bounds are then used to determine the call admissible conditions, which meet the delay jitter constraint for CBR and assure predictable overall delay bound for VBR. Finally, the overall delay bounds are derived.

4.1. Scheduling delay bound analysis

For convenience in the following delay bound analysis, we defined some related work load functions in Lemmas 1–3. The proofs of Lemmas 1–3 are given in Appendix A.

Lemma 1. *If there exists CBR-j cells in the scheduler at time t and the latest cell to enter the scheduler before time t has instantaneous due-date s at time t, then the number of CBR-j cells which enter the scheduler during the interval $[t - \Delta, t]$ is bounded by $N_j^c(\Delta, s)$, where*

$$N_j^c(\Delta, s) = \begin{cases} 1 + \left\lfloor \dfrac{\Delta + s - \delta_j^c}{T_j^c} \right\rfloor & \text{for } \Delta + s \geq \delta_j^c, \Delta \geq 0, \\ 0 & \text{otherwise.} \end{cases} \tag{10}$$

Lemma 2. *If there exists a cell belonging to VBR-j in the scheduler at time t with instantaneous due-date s, then the number of VBR-j cells which enter the scheduler during the interval $[t - \Delta, t]$ is bounded by $N_j^v(\Delta, s)$, where*

$$N_j^v(\Delta, s) = \begin{cases} 1 + \left\lfloor \dfrac{\Delta + s - 1}{T_j^v} \right\rfloor & \text{for } \Delta + s \geq \delta_j^v, \Delta \geq 0, \\ 0 & \text{otherwise.} \end{cases} \tag{11}$$

Lemma 3. *The number of CBR cells emitted from the scheduler during $(t - \Delta, t]$ is bounded by $S_c(\Delta)$, where*

$$S_c(\Delta) = \max_{0 \leq v \leq h_c} \left\{ \sum_{i=1}^{K_c} N_i^c(v + \Delta, \tau_i^c) - v \right\}, \tag{12}$$

and h_c is the maximum CBR busy period.

The functions $N_j^c(\Delta, s)$ and $N_j^v(\Delta, s)$ are related to the input traffic load, while $S_c(\Delta)$ describes the output traffic load during any period Δ.

Theorem 1. *Consider a target cell from CBR-j with initial due-date y. Then the scheduling delay bound, $d_j^c(y)$, of the target cell in the scheduler is given as follows:*

$$d_j^c(y) = \max_{\Delta \geq 0} \left\{ \min \left\{ u \middle| \sum_{i=1}^{K_c} N_i^c(u + \Delta, s_i^c) \leq u + \Delta, u \geq 1 \right\} \right\}, \tag{13}$$

where $s_i^c = \min\{y - u, \tau_i^c\}$.

Proof. Consider the target cell which enters the scheduler with initial due-date y at time t. Assume the CBR busy period of the scheduler that contains time t started at some earlier time $(t - \Delta)$ and the target cell is emitted at time $(t + u)$, where $\Delta \geq 0$ and $u \geq 1$. Since the scheduler processing time is one slot, the last CBR-i cell which can contribute to the busy period $[t - \Delta, t + u]$ should not enter the scheduler later than time $(t + u - 1)$. Assume that the last CBR-i ($i \neq j$) cell that can be emitted before the target cell enters the scheduler at time $(t + v)$ with initial due-date s. Since $\delta_i^c \leq s \leq \min\{y - v, \tau_i^c + 1\}$ must hold under the initial due-date constraint and the EDD service discipline, we have $v \leq \min\{y - \delta_i^c, u - 1\}$. Then by Lemma 1, during $[t - \Delta, t + v]$ the maximum number of CBR-i cells which can be emitted before the target cell, is bounded by $N_i^c(v + \Delta, s)$. It can be shown that $N_i^c(v + \Delta, s) \leq N_i^c(u + \Delta, \min\{y - u, \tau_i^c\})$ by Eq. (10). Moreover, during $[t - \Delta, t]$ the maximum number of CBR-j cells entering the scheduler is bounded by $N_j^c(\Delta, y)$. For $\delta_j^c \leq y \leq \tau_j^c + 1$, it is obvious that $N_j^c(\Delta, y) = N_j^c(u + \Delta, \min\{y - u, \tau_j^c\})$. Since during $[t - \Delta, t + u]$ the scheduler is busy in serving CBR cells, the delay of the target cell is not larger than the minimum u that satisfies

$$\sum_{i=1}^{K_c} N_i^c(u + \Delta, s_i^c) \leq u + \Delta \quad \text{for any } \Delta \geq 0, u \geq 1, \tag{14}$$

where $s_i^c = \min\{y - u, \tau_i^c\}$. Thus, one can obtain the delay bound (13). $\square$

Theorem 2. *Consider a target cell from VBR-j with initial due-date y. Then the scheduling delay bound, $d_j^v(y)$, of the target cell in the scheduler is given as follows:*

$$d_j^v(y) = \max_{\Delta \geq 0} \{ \min\{ u | L_c(u, \Delta) + L_v(u, \Delta, y) \leq u + \Delta, u \geq 1 \}\}, \tag{15}$$

where

$$L_c(u, \Delta) = \sum_{i=1}^{K_c} N_i^c(u + \Delta, \tau_i^c),$$

$$L_v(u, \Delta, y) = \min \left\{ K_v + \Delta + v^\star - [L_c(u, \Delta) - S_c(u - 1 - v^\star)]^+, \sum_{i=1}^{K_v} N_i^v(u + \Delta, s_i^v) \right\},$$

with $v^\star = \min\{y - \min_{1 \le i \le K_v}\{\delta_i^v\}, u - 1\}$, $s_i^v = \min\{y - u, \tau_i^v\}$ *and* $[x]^+ = x$ *if* $x > 0$, $[x]^+ = 0$ *otherwise.*

Proof. Consider the target cell which enters the scheduler with initial due-date y at time t. Assume the combined CBR and VBR busy period of the scheduler that contains time t started at some earlier time $(t - \Delta)$ and the target cell is emitted at time $(t + u)$, where $\Delta \ge 0$ and $u \ge 1$. Since the scheduler processing time is one slot, the CBR cells which contribute to the busy period $[t - \Delta, t + u]$ should not enter the scheduler later than time $(t + u - 1)$, i.e., only those CBR cells entering the scheduler during the interval $[t - \Delta, t + u - 1]$ can be emitted before the target cell. Thus, by Lemma 1 the maximum number of CBR cells that can be emitted before the target cell is equal to $\sum_{i=1}^{K_c} N_i^c(u + \Delta - 1, \tau_i^c + 1)$, which is not larger than

$$L_c(u, \Delta) = \sum_{i=1}^{K_c} N_i^c(u + \Delta, \tau_i^c). \tag{16}$$

On the other hand, assume that the last VBR-i ($i \ne j$) cell that can be emitted before the target cell, enters the scheduler at time $(t + v)$ with initial due-date s. Since $\delta_i^v \le s \le \min\{y - v, \tau_i^v + 1\}$ should be satisfied under the initial due-date constraint and the EDD service discipline, we have $v \le \min\{y - \delta_i^v, u - 1\}$. This means that the last VBR-i cell that can be emitted before the target cell should not enter the scheduler later than time $t + \min\{y - \delta_i^v, u - 1\}$. By Lemma 2, the number of VBR-i cells which enter the scheduler during $[t - \Delta, t + v]$, and can be emitted before the target cell is bounded by $N_i^v(v + \Delta, s)$, which is not larger than $N_i^v(u + \Delta, s_i^v)$, where $s_i^v = \min\{y - u, \tau_i^v\}$. In addition, the number of VBR-j cells entering the scheduler during $[t - \Delta, t]$ is bounded by $N_j^v(\Delta, y)$, which is equal to $N_j^v(u + \Delta, s_j^v)$. Since all the VBR-i (for all $i \ne j$) cells entering the scheduler during $[t - \Delta, t + v]$ and the VBR-j cells entering the scheduler during $[t - \Delta, t]$ can contribute to the busy period $[t - \Delta, t + u]$, the maximum number of VBR cells which can contribute to the busy period $[t - \Delta, t + u]$ is bounded by $\sum_{i=1}^{K_v} N_i^v(u + \Delta, s_i^v)$. However, since there exists a feedback signal between the regulator and the scheduler, and recall that all VBR cells which can contribute to the busy period $[t - \Delta, t + u]$ should not enter the scheduler later than time $(t + v^\star)$, where $v^\star = \min\{y - \min_{1 \le i \le K_v}\{\delta_i^v\}, u - 1\}$, the number of VBR cells existing in the scheduler cannot be larger than K_v at time $(t + v^\star)$. It follows that the number of VBR cells which can contribute to the busy period $[t - \Delta, t + u]$ cannot possibly be larger than $S_v(\Delta + v^\star) + K_v$, where $S_v(\Delta + v^\star)$ is the maximum number of VBR cells emitted during $[t - \Delta, t + v^\star]$ given that the number of CBR cells entering the scheduler during $[t - \Delta, t + u - 1]$ is $L_c(u, \Delta)$.

By Lemma 3, one can observe that

$$S_v(\Delta + v^\star) = \Delta + v^\star - [L_c(u, \Delta) - S_c(u - 1 - v^\star)]^+.$$

Therefore, the maximum number of VBR cells which can contribute to the busy period $[t - \Delta, t + u]$ is bounded by

$$L_v(u, \Delta, y) = \min \left\{ K_v + \Delta + v^\star - [L_c(u, \Delta) - S_c(u - 1 - v^\star)]^+, \sum_{i=1}^{K_v} N_i^v(u + \Delta, s_i^v) \right\}. \quad (17)$$

Since both $L_c(u, \Delta)$ and $L_v(u, \Delta, y)$ contribute to the busy period $[t - \Delta, t + u]$, the delay of the target cell should not be larger than the minimum u that satisfies

$$L_c(u, \Delta) + L_v(u, \Delta, y) \leq u + \Delta \quad \text{for any} \ \Delta \geq 0, \ u \geq 1. \quad (18)$$

It follows that the delay bound, $d_j^v(y)$, of the target cell can be rewritten as (15). □

Under the stable condition $\sum_{i=1}^{K_c}(1/T_i^c) + \sum_{i=1}^{K_v}(1/T_i^v) < 1$, the maximum CBR busy period, h_c, and the maximum combined CBR and VBR busy period, h_{c+v}, of the scheduler are bounded. This shows that the upper limits of the search intervals of Δ in (13) and (15) need not exceed h_c and h_{c+v}, respectively.

4.2. Call admission control

When cell overdue events are completely avoided, our shaper can operate without accumulating cells from burst to burst in the regulator. In this case, we can guarantee both the throughput for all VBR connections and the constrained delay jitter for CBR. The following theorems provide the conditions necessary to avoid cell overdue events. One should note that if a cell is overdue, then its *ADT* is larger than its *TDT*. However, for VBR cells, *ADT* > *TDT* does not always imply an overdue event.

Theorem 3. *If $d_j^c(\delta_j^c) \leq \delta_j^c$, then no cells of CBR-j are overdue and thus all output cells of CBR-j satisfy the jitter constraint τ_j^c.*

Proof. Consider an arbitrary cell from CBR-j and let its initial due-date be y. If $d_j^c(y) \leq y$, for all $y \geq \delta_j^c$, this cell shall not experience an overdue event. To show the sufficient condition, by Eq. (13) one can express $d_j^c(y) - y$ as

$$d_j^c(y) - y$$

$$= \max_{\Delta \geq 0} \left\{ \min \left\{ u - y \ \middle| \ \sum_{i=1}^{K_c} N_i^c(u + \Delta, s_i^c) \leq u + \Delta, u \geq 1 \right\} \right\}$$

$$= \max_{\Delta' \geq y - \delta_j^c} \left\{ \min \left\{ u' - \delta_j^c \ \middle| \ \sum_{i=1}^{K_c} N_i^c(u' + \Delta', \min\{\delta_j^c - u', \tau_i^c\}) \leq u' + \Delta', u' \geq 1 - y + \delta_j^c \right\} \right\}$$

$$= \max_{\Delta \geq y - \delta_j^c} \left\{ \min \left\{ u - \delta_j^c \ \middle| \ \sum_{i=1}^{K_c} N_i^c(u + \Delta, q_i^c) \leq u + \Delta, u \geq 1 - y + \delta_j^c \right\} \right\}, \quad (19)$$

where $u' = u - y + \delta_j^c$, $\Delta' = \Delta + y - \delta_j^c$, and $q_i^c = \min\{\delta_j^c - u, \tau_i^c\}$. For $y \geq \delta_j^c$, one can write

$$d_j^c(y) - y \leq \max_{\Delta \geq 0} \left\{ \min \left\{ u - \delta_j^c \left| \sum_{i=1}^{K_c} N_i^c(u + \Delta, q_i^c) \leq u + \Delta, u \geq 1 \right. \right\} \right\} = d_j^c(\delta_j^c) - \delta_j^c. \tag{20}$$

Thus, $d_j^c(y) \leq y$ for all $y \geq \delta_j^c$ is implied by $d_j^c(\delta_j^c) \leq \delta_j^c$. We then conclude $d_j^c(\delta_j^c) \leq \delta_j^c$ implies no cell overdue for CBR-j.

For CBR cells, by Eq. (7) no cell overdue implies $ADT_j(k) \leq TDT_j(k)$ for all k. Subsequently, we show that the jitter constraint is not violated. Since $ET_j(k) + 1 \leq ADT_j(k) \leq TDT_j(k)$, one can observe that $ADT_j(m) - ADT_j(n)$ satisfies

$$[ET_j(m) + 1] - TDT_j(n) \leq ADT_j(m) - ADT_j(n) \leq TDT_j(m) - [ET_j(n) + 1] \tag{21}$$

for all $m \neq n$. First, $TDT_j(m) - [ET_j(n) + 1]$ can be rewritten as

$$TDT_j(m) - [ET_j(n) + 1] = TDT_j(m) - \max\{\lceil TDT_j(n) - \tau_j^c \rceil, A_j(n) + 1\}$$
$$\leq TDT_j(m) - \lceil TDT_j^c(n) - \tau_j^c \rceil \leq (m - n)T_j^c + \tau_j^c. \tag{22}$$

Secondly, $[ET_j(m) + 1] - TDT_j(n)$ can be expressed as

$$[ET_j(m) + 1] - TDT_j(n) = \max\{\lceil TDT_j(m) - \tau_j^c \rceil, A_j(m) + 1\} - TDT_j(n)$$
$$\geq \lceil TDT_j(m) - \tau_j^c \rceil - TDT_j(n) \geq (m - n)T_j^c - \tau_j^c. \tag{23}$$

Combining (21)–(23), we conclude that

$$(m - n)T_j^c - \tau_j^c \leq ADT_j(m) - ADT_j(n) \leq (m - n)T_j^c + \tau_j^c. \tag{24}$$

That is,

$$|ADT_j(m) - ADT_j(n) - (m - n)T_j^c| \leq \tau_j^c \tag{25}$$

for all $m \neq n$. By definition, for CBR-j the jitter constraint is not violated when $d_j^c(\delta_j^c) \leq \delta_j^c$. $\qquad\square$

Theorem 4. *If $d_j^v(\delta_j^v) \leq \delta_j^v$, then no cell of VBR-j will be overdue.*

A similar procedure as the proof of Theorem 3 can be employed to show Theorem 4, and thus we omit it here. The CAC procedure to avoid any overdue event operates as follows. When a new CBR connection, say CBR-n, requests to be supported by the shaper, $d_j^c(\delta_j^c)$ and $d_j^v(\delta_j^v)$ are computed for all existing CBR and VBR connections and CBR-n. If all $d_j^c(\delta_j^c) \leq \delta_j^c$ and $d_j^v(\delta_j^v) \leq \delta_j^v$ are satisfied, the new request is granted. Otherwise, it is rejected. Similarly, when a new VBR connection, say VBR-m, requests to be supported by the shaper, $d_j^v(\delta_j^v)$ are computed for all existing VBR connections and VBR-m. If all $d_j^v(\delta_j^v) \leq \delta_j^v$ are satisfied, the new request is granted. Otherwise, it is rejected.

4.3. Overall delay bound analysis

The overall cell delay of the proposed traffic shaper is defined to be the sum of the delay in the regulator and the scheduler. The overall delay bounds for CBR and VBR cells are given by the following two theorems.

Theorem 5. *The overall cell delay of CBR-j within the traffic shaper is bounded by D_j^c, where*

$$D_j^c \leq p_j + \tilde{\tau}_j^c + 1 + d_j^c(\tau_j^c + 1). \tag{26}$$

Proof. From (1), one can obtain

$$A_j(n) \geq A_j(1) + (n - 1)T_j^c - \tilde{\tau}_j^c. \tag{27}$$

By (5) and the initial value $TDT_j(1) = A_j(1) + p_j + \tau_j^c + 1$, it is obvious that

$$TDT_j(n) = A_j(1) + p_j + \tau_j^c + 1 + (n - 1)T_j^c. \tag{28}$$

By using (6), (27) and (28), we have

$$ET_j(n) - A_j(n) \leq p_j + \tilde{\tau}_j^c + 1. \tag{29}$$

For CBR-j, $ADT_j(n) \leq ET_j(n) + d_j^c(y)$ for all n, where y is the initial due-date of the nth cell and $\delta_j^c \leq y \leq \tau_j^c + 1$. By definition, we have

$$D_j^c = \max_{n \in N}\{ADT_j(n) - A_j(n)\} \leq \max_{n \in N}\{ET_j(n) - A_j(n) + d_j^c(y)\}. \tag{30}$$

Combining (29) and (30), we obtain

$$D_j^c \leq p_j + \tilde{\tau}_j^c + 1 + d_j^c(\tau_j^c + 1). \qquad \square \tag{31}$$

From (31), it is obvious that the overall cell delay bound in the shaper is affected directly by the design parameter p_j, the input jitter $\tilde{\tau}_j^c$ and the desired output jitter τ_j^c.

Theorem 6. *If VBR-j is guaranteed to be free of cell overdue events, the overall cell delay of VBR-j within the traffic shaper is bounded by D_j^v, where*

$$D_j^v \leq d_j^v(\delta_j^v) + \left\lfloor \frac{\tilde{\tau}_j^v}{\tilde{T}_j^v - \tilde{X}_j^v} \right\rfloor (T_j^v - \tilde{X}_j^v). \tag{32}$$

If $T_j^v = \tilde{T}_j^v$, then

$$D_j^v \leq d_j^v(\delta_j^v) + \tilde{\tau}_j^v. \tag{33}$$

The proof of the theorem can be found in [11], and it is omitted here. In the theorem, the sufficient condition is implied by the call admissible condition for VBR in Section 4.2. Hence, as long as the CAC procedure to avoid cell overdue is applied, then the overall delay for VBR cells is always bounded. Meanwhile, with bounded overall cell delay, the buffer requirement to guarantee no cell loss in the traffic shaper can be easily derived.

5. Numerical results

In this section, we provide examples to illustrate the advantages of the proposed ATM traffic shaper. The ATM link data rate is set to be 149.76 Mbps. During simulation, input cell streams to the regulator are
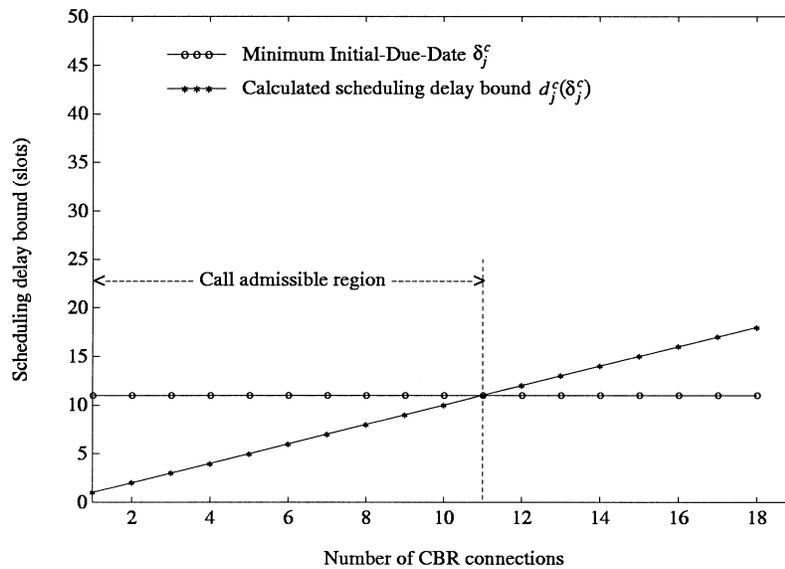
Fig. 3. Scheduling delay bound versus the number of CBR connections, with emulated DS2 circuits.

generated by the following rule. The kth cell arrival is first generated by a pseudo-arrival time $TAT(k) - x$, where $x = \tilde{\tau}$ (the input jitter or burst tolerance parameter) with probability r and $x = 0$ with probability $(1 - r)$. The recurrence equation $TAT(k) = TAT(k - 1) + \tilde{T}$ determines the kth theoretical arrival time for $k \geq 1$, while $TAT(0)$ can be arbitrarily set. The actual cell arrival time for simulation, $A(k)$, is determined by

$$A(k) = \max\{\lceil TAT(k) - x \rceil, A(k - 1) + 1\}$$

for CBR connections, and

$$A(k) = \max\{\lceil TAT(k) - x \rceil, A(k - 1) + \lceil \tilde{X}^{\mathrm{v}} \rceil\}$$

for VBR connections. Note that $A(k)$ is always an integer. One can observe that the generated input arrival cell stream conforms to the traffic descriptor $(\tilde{T}^{\mathrm{c}}, \tilde{\tau}^{\mathrm{c}})$ or $(\tilde{X}^{\mathrm{v}}, \tilde{T}^{\mathrm{v}}, \tilde{\tau}^{\mathrm{v}})$.

In the first example, only CBR connections are supported. The traffic descriptor and the design parameter of each CBR connection are given as follows: $(\tilde{T}_j^{\mathrm{c}}, \tilde{\tau}_j^{\mathrm{c}}) = (21.0392, 100)$, $(T_j^{\mathrm{c}}, \tau_j^{\mathrm{c}}) = (21.0392, 50)$, $p_j = 60$ for all j. Note that $T_j^{\mathrm{c}} = 21.0392$ corresponds to the required throughput of an unstructured DS2 emulated circuit. Fig. 3 shows the curves of the minimum initial due-date δ_j^{c} and the scheduling delay bound $d_j^{\mathrm{c}}(\delta_j^{\mathrm{c}})$ versus the number of CBR connections. According to the CAC condition $d_j^{\mathrm{c}}(\delta_j^{\mathrm{c}}) \leq \delta_j^{\mathrm{c}}$ in Theorem 3, at $p_j = 60$ only up to 11 CBR connections can be admitted if jitter violation for CBR cells is to be avoided. Fig. 4 indicates the maximum overall delay for CBR cells. Simulation and analytical results are both given. It reveals that the analytical bound is excellent. In Fig. 5, we use simulation to compare the proposed traffic shaper with an EDD scheduler against the shaper design for CBR traffic with an FIFO multiplexer and identical regulator, using non-conforming cell ratio as a performance metric. Here, each non-conforming cell is also a jitter violation cell for CBR. Fig. 5 shows that jitter violation events do not occur until the number of CBR connections is beyond the call admissible region. The EDD
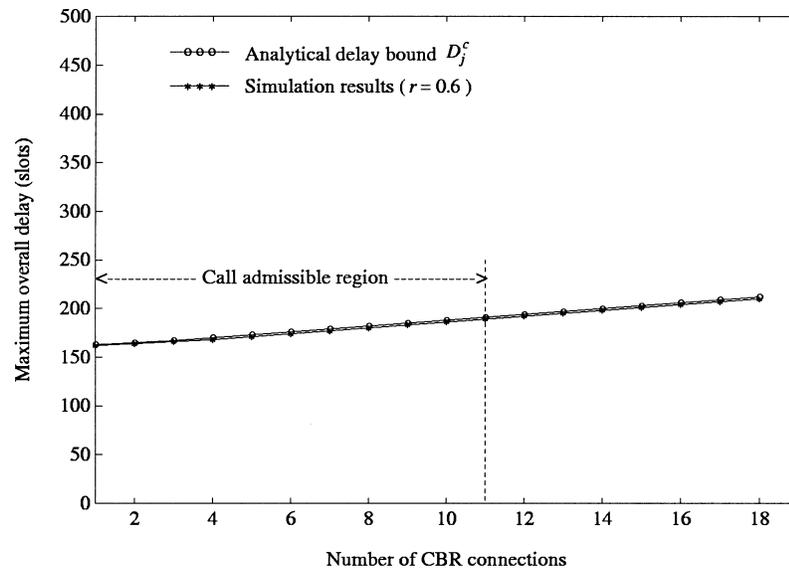
Fig. 4. Maximal overall delay versus the number of CBR connections, with emulated DS2 circuits.

scheduler also results in smaller non-conforming cell ratio than the FIFO multiplexer even under heavy traffic loads. The latter result agrees with that in [14]. Fig. 6 illustrates how the maximum number of admitted CBR connections is affected by the design parameter p_j. Obviously, when one increases the parameter p_j, which is a key part of the minimum initial due-date δ_j^c, the bandwidth utilization can be improved. However, the maximum overall delay performance can be degraded if p_j increases to a very
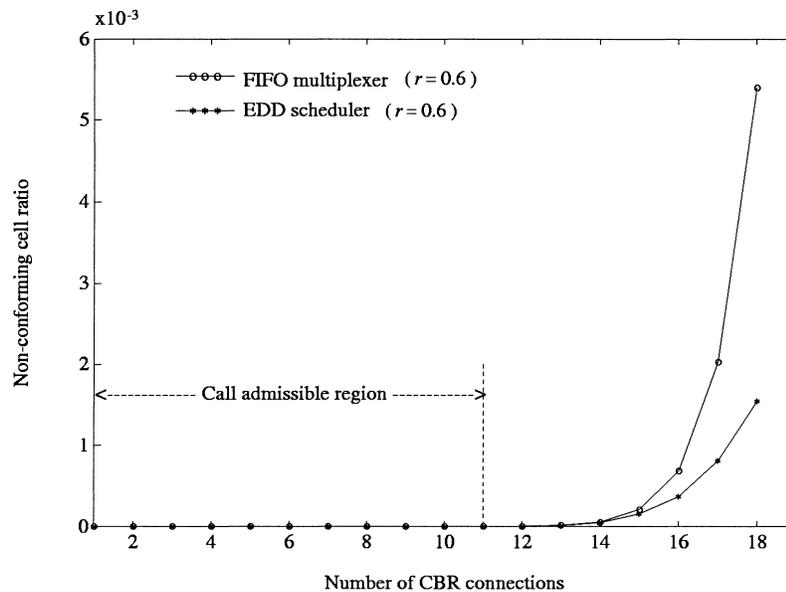
Fig. 5. Non-conforming cell ratio versus the number of CBR connections, with emulated DS2 circuits.
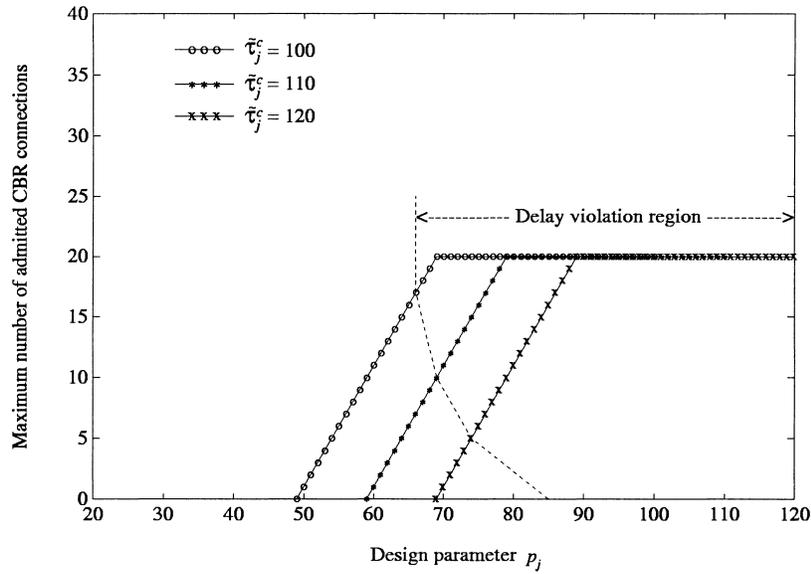
Fig. 6. Maximal number of admitted CBR connections (DS2) versus the design parameter p_j, with overall delay constraint $D_j^c \leq 210$ slots and burst tolerance $\tilde{\tau}_j^c =$ 100, 110, 120 slots.

high level. The engineering rule for determining p_j is thus to choose p_j as close to $\tilde{\tau}_j^c$ as possible, provided that none of the delay constraints D_j^c is violated, i.e., $p_j = \min\{\tilde{\tau}_j^c, D_j^c - \tilde{\tau}_j^c - 1 - d_j^c(\tau_j^c + 1)\}$.

In the second example, there are eight homogeneous CBR connections with traffic descriptors $(\tilde{T}_j^c, \tilde{\tau}_j^c) = (21.0392, 21)$, $(T_j^c, \tau_j^c) = (21.0392, 10)$, $p_j = 21$, and several homogeneous VBR connections with traffic descriptors $(\tilde{X}_j^v, \tilde{T}_j^v, \tilde{\tau}_j^v) = (3, 86.2323, 1600)$, $(X_j^v, T_j^v, \tau_j^v) = (20, 86.2323, 200)$ for all j. Note that the sustainable cell rate of the VBR connections is equivalent to the data rate of a DS1. Using the CAC condition $d_j^v(\delta_j^v) \leq \delta_j^v$ in Theorem 4, the call admissible region is calculated as shown in Fig. 7. From Fig. 8, one can observe that the analytical bound for the maximal overall delay is very close to the simulation results. In Figs. 9–11, we compare the proposed traffic shaper with feedback signal against two other traffic shaper designs: one with an EDD scheduler and one with a regular FIFO multiplexer; both are without feedback signal. The regulators of all three shaper designs are similar. For the traffic shapers without feedback signal, no information about $ADT_j(k-1)$ is available. Therefore, their algorithms in the regulator still follow (2)–(4), except that $ADT_j(k-1)$ in (2) and (3) is replaced by $ET_j(k-1) + 1$. In Fig. 9, computer simulations confirm that the output cell streams of the proposed traffic shaper do not contain any non-conforming cells. However, the output cell streams of the two traffic shapers without feedback signal do contain non-conforming cells, due to emission conflicts in the scheduler. Note that for each active VBR connection, there can be at most one cell at the scheduler. As we have expected, in Fig. 10 the maximum queue size in the EDD scheduler with feedback signal is controlled to be equal to the number of active VBR connections. While for the other traffic shapers without feedback signal, the maximum queue size can be much larger than the number of VBR connections.

The probability density functions (p.d.f.) of interdeparture time for all the above three shaper designs are given in Fig. 11. For the shaper with an EDD scheduler and feedback signal, the interdeparture time distribution is well controlled to be in the neighborhood of T_j^v. However, the designs without feedback
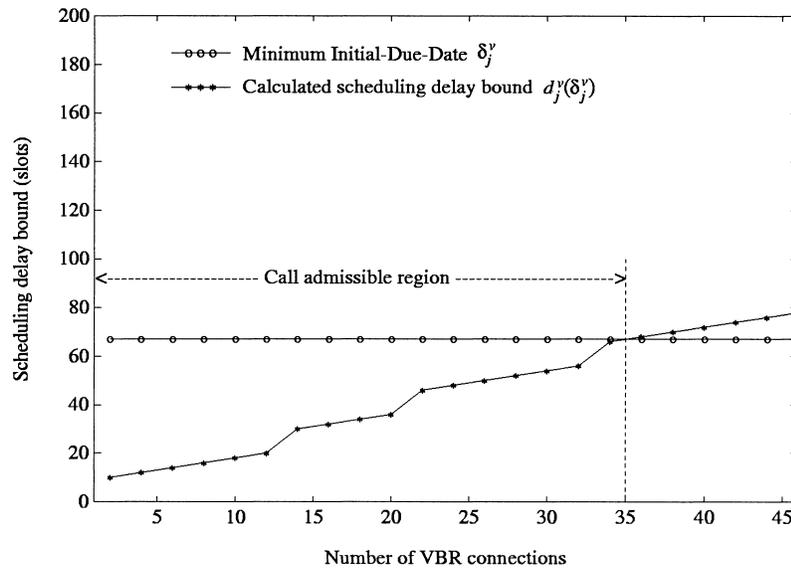
Fig. 7. Scheduling delay bound versus the number of VBR connections, each with DS1 equivalent sustainable cell rate. Background traffic consists of eight DS2 emulated circuits.

signal may lead to non-conforming cells in the output cell streams. Either based on the non-conforming cell ratio or by observing the p.d.f of interdeparture time, one can conclude that the shaper with an FIFO multiplexer and no feedback signal is the least favorable design. One can also conclude that the variance of the interdeparture time for the shaper with an EDD scheduler and feedback signal is much smaller than
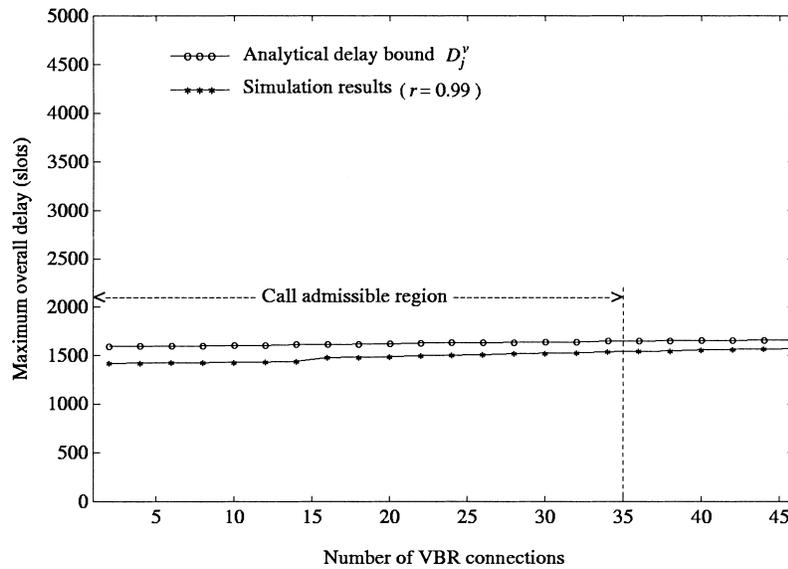

Fig. 8. Maximal overall delay versus the number of VBR connections, each with DS1 equivalent sustainable cell rate. Background traffic consists of eight DS2 emulated circuits.
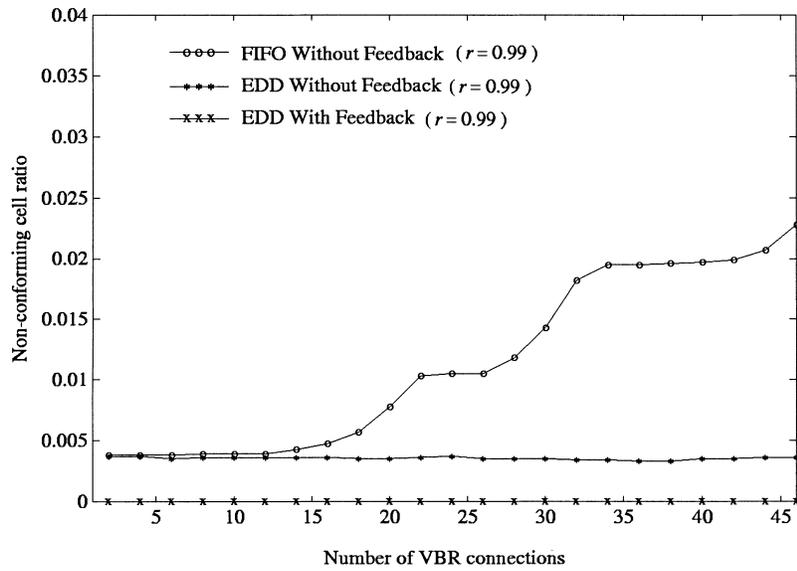
Fig. 9. Observed non-conforming cell ratio versus the number of VBR connections, with three different shaper designs: EDD with feedback, EDD without feedback and FIFO without feedback.
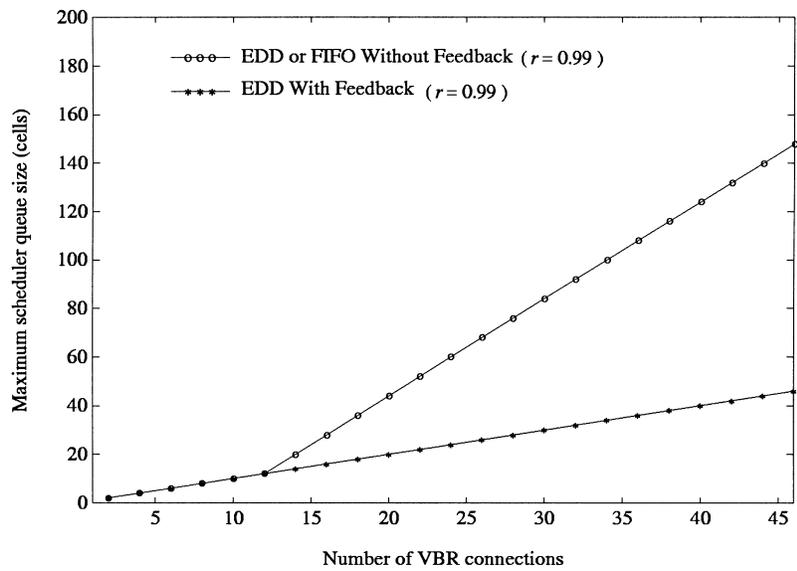

Fig. 10. Observed maximum scheduler queue size versus the number of VBR connections, with three different shaper designs: EDD with feedback, EDD without feedback and FIFO without feedback.
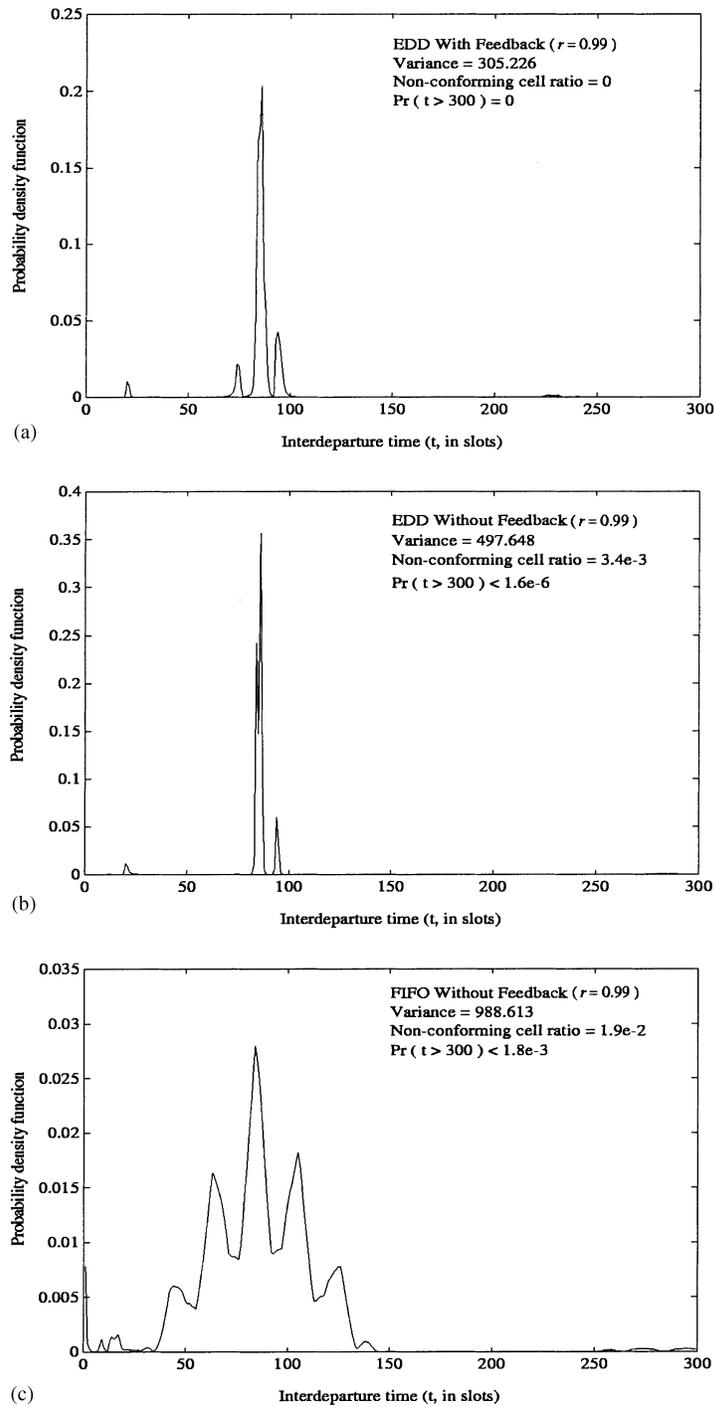
Fig. 11. Probability density functions of interdeparture time for a specific VBR connection from the shaper with (a) EDD with feedback (b) EDD without feedback and (c) FIFO without feedback. Total traffic load contributed by eight DS2 emulated circuits and 34 VBR connections is 77.5%.

those of the other two. All these results reveal that the performance of a shaper with an EDD scheduler and feedback signal is outstanding.

6. Implementation issues

The major features of the proposed traffic shaper model include the EDD schedulers and the feedback control mechanism. In order to implement the proposed traffic shaper, the queued cells in the EDD schedulers must be sorted according to their due-dates. According to [14,15], this requires a search or sort operation whenever a new cell enters the scheduler. Since the due-dates vary with time and may complicate the implementation of EDD scheduler, the *deadline* $DL_j(k)$, which is a constant and defined as $DL_j(k) = ET_j(k) + IDD_j(k)$, can replace the due-date as the sorting metric. That is, the cell with the smallest deadline is emitted first. One should note that sorting the deadlines is equivalent to sorting the due-dates, since the due-date represents the remaining time to the deadline.

In addition, a modification to the simple EDD algorithm in [14] or [15] is required due to the addition of the feedback control mechanism. The modification is simply described as follows. At the departure of the $(k-1)$th VBR-j cell, the values of $TDT_j(k)$, $ET_j(k)$, $IDD_j(k)$ and the deadline $DL_j(k)$ must first be determined in the regulator. Then the sorting algorithm for choosing the next cell within the EDD scheduler to be emitted can be executed. It means that the sorting algorithm and the computation of $TDT_j(k)$, $ET_j(k)$, $IDD_j(k)$ and $DL_j(k)$ should be completed within one cell slot time. Since the time complexity of computing $TDT_j(k)$, $ET_j(k)$, $IDD_j(k)$ and $DL_j(k)$ is much smaller than that of the sorting algorithm, there will be no difficulty to implement the proposed shaper model based on the simple EDD operation in [14] or [15].

Notably, the implementation complexity of EDD algorithm can only be related to the total number of connections but not the number of cells. If the implementation complexity of EDD algorithm in [14] or [15] is still considered not acceptable when large number of connections need to be supported, other alternative scheduling algorithms, such as *rotating-priority-queues* (RPQ) [16] which approximates EDD scheduling without sorting queued cells, can be employed in the scheduler, and we expect the resulting performance for any EDD-like scheduler should be similar.

7. Conclusions

In this paper, a new ATM traffic shaper has been proposed for supporting both CBR and VBR traffic. This shaper has considered and resolved the emission conflict problem that other designs [1–10] did not. With an EDD scheduler, the jitter violation ratio for CBR and the scheduling overdue events for VBR, due to cell emission conflicts, can be reduced significantly. By using a feedback signal between the regulator and the scheduler for VBR services, we can guarantee the output VBR cell streams to always conform to the desired traffic descriptors, under any traffic conditions, and the output queue size can be significantly decreased. We believe similar designs can be employed for simplifying the traffic control circuit in many other ATM devices.

For this traffic shaper, the delay bounds for both CBR and VBR, and the CAC mechanisms are also presented. For CBR services, the overall delay bound, including the delay in the regulator and the sched-

uler, is derived for any traffic condition. For VBR services, the overall delay bound is derived under the call admissible condition. The numerical results illustrate that the analytical delay bounds are tight. The resulting utilization with the CAC mechanism is still reasonable. Hence, the proposed traffic shaper design is excellent for supporting both real time CBR and non-real time VBR.

It is known that VBR services include both real time VBR (rtVBR) and non-real time VBR (nrtVBR). To extend the functionality of the proposed shaper to support CBR, rtVBR and nrtVBR, there should be three EDD queues in the scheduler, one for each traffic class. The same scheduler and feedback mechanism can be applied to both rtVBR and nrtVBR. The CBR cells are still assigned to have the highest service priority, while nrtVBR cells have the lowest service priority. The analytical approaches presented in this paper can be directly applied to CBR and rtVBR, respectively. With appropriate CAC, the jitter constraints for CBR can also be met. Meanwhile, rtVBR and nrtVBR output streams should still conform to the desired output traffic descriptors under the proposed mechanism. Only the performance and CAC condition for nrtVBR must be derived, but a similar analytical procedure can be employed. One can refer to [17] for details.

The proposed traffic shaper can also be used for supporting ABR services if one adds ABR departure controllers in the regulator and an EDD queue for ABR cells in the scheduler. As long as one assigns the ABR cells the lowest priority for cell emission in the scheduler, the performance bounds for both CBR and VBR cells in Section 4 should still hold. The performance bound for ABR services could then be obtained via a procedure similar to what we have presented in Section 4. However, the behavior of an ABR mechanism under the traffic shaper should be a target for future study.

Appendix A

Proof of Lemma 1. Assume that there are n CBR-j cells, indexed from $(k + 1)$ to $(k + n)$ for some k, to enter the scheduler during the interval $[t - \Delta, t]$. Let the $(k + n)$th cell have instantaneous due-date s at time t. Then $t - \Delta \le ET_j(k + l) \le t$ should always hold for all l, where $1 \le l \le n$. By Eq. (9), $ET_j(k + n) = t + s - IDD_j(k + n)$. Hence, one can either derive $\Delta + s \ge IDD_j(k + n) \ge \delta_j^c$ for $n \ge 1$, or n must be 0. Now, we consider the case $n \ge 1$ and $\Delta + s \ge \delta_j^c$, from (7) we have

$$
\begin{aligned}
ET_j(k + n) - ET_j(k + 1) &= [TDT_j(k + n) - IDD_j(k + n)] - [TDT_j(k + 1) - IDD_j(k + 1)] \\
&= (n - 1)T_j^c + IDD_j(k + 1) - IDD_j(k + n) \\
&\ge (n - 1)T_j^c + \delta_j^c - IDD_j(k + n).
\end{aligned}
\tag{A.1}
$$

Since $ET_j(k + n) = t + s - IDD_j(k + n)$, we have $ET_j(k + 1) \le t - (n - 1)T_j^c + s - \delta_j^c$. It follows that

$$
t - \Delta \le t - (n - 1)T_j^c + s - \delta_j^c.
\tag{A.2}
$$

Thus, for $\Delta \ge 0$ and $\Delta + s \ge \delta_j^c$, n should satisfy

$$
n \le 1 + \left\lfloor \frac{\Delta + s - \delta_j^c}{T_j^c} \right\rfloor.
\tag{A.3}
$$

Hence, one obtains (10). □

Proof of Lemma 2. Based on the same approach as what we used in the proof of Lemmas 1 and 2 can be proved. From (4) one has

$$ET_j(k + n) \geq TDT_j(k + n) - IDD_j(k + n). \tag{A.4}$$

Since the scheduling delay is at least one slot, we also have $ET_j(k + 1) \leq ADT_j(k + 1) - 1$ for all k. Therefore, one can obtain

$$\begin{aligned} ET_j(k + n) - ET_j(k + 1) &\geq [TDT_j(k + n) - IDD_j(k + n)] - [ADT_j(k + 1) - 1] \\ &\geq (n - 1)T_j^v - IDD_j(k + n) + 1. \end{aligned} \tag{A.5}$$

Under the non-trivial case $\Delta + s \geq \delta_j^v$, with $ET_j(k + n) = t + s - IDD_j(k + n)$, we have

$$t - \Delta \leq ET_j(k + 1) \leq t - (n - 1)T_j^v + s - 1. \tag{A.6}$$

Thus, for $\Delta \geq 0$ and $\Delta + s \geq \delta_j^v$, n should satisfy

$$n \leq 1 + \left\lfloor \frac{\Delta + s - 1}{T_j^v} \right\rfloor. \tag{A.7}$$

Eq. (11) then follows. $\qquad\square$

Proof of Lemma 3. First, consider the case that there exist CBR cells in the scheduler at time $(t - \Delta)$. Then one can assume the CBR busy period of the scheduler that contains time $(t - \Delta)$ starts at time $(t - \Delta - v)$, where $0 \leq v \leq h_c$. Since the scheduler processing time is one slot in the scheduler, all the CBR cells emitted during $[t - \Delta - v, t]$ should have entered the scheduler during $[t - \Delta - v, t - 1]$. By Lemma 1, one can obtain that the number of CBR cells emitted during $(t - \Delta, t]$ is bounded by the maximum value of

$$\sum_{i=1}^{K_c} N_i^c(v + \Delta - 1, \tau_i^c + 1) - v \quad \text{for } 0 \leq v \leq h_c, \tag{A.8}$$

which is equivalent to (12).

Secondly, consider the case that there are no CBR cells at time $(t - \Delta)$. Then one can assume that the earliest CBR busy period during $[t - \Delta, t]$ starts at time $(t - u)$, where $u < \Delta$. Thus, the maximum number of CBR cells emitted during $(t - \Delta, t]$ is bounded by $\sum_{i=1}^{K_c} N_i^c(u - 1, \tau_i^c + 1) \leq \sum_{i=1}^{K_c} N_i^c(\Delta - 1, \tau_i^c + 1)$. One can observe that $\sum_{i=1}^{K_c} N_i^c(\Delta - 1, \tau_i^c + 1)$ is equal to (A.8) by setting $v = 0$. Hence, Lemma 3 is proved. $\qquad\square$

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