A Three-Stage One-Sided Rearrangeable Polygonal Switching Network

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Abstract—This paper proposes a three-stage rearrangeable polygonal switching network (PSN) for interconnecting one-sided input-output terminals. In comparing our PSN with a three-stage one-sided Clos switching network of the same size and with the same number of switches, we prove that rearrangeability of a PSN is better than that of a Clos switching network. Also, the switches efficiency of PSN is explored.

Index Terms—Rearrangeable, switching network, polygonal switching network.

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1 INTRODUCTION

IN communication and computer networks, two-sided switching networks consisting of switching elements, such as crosspoints and interconnecting links, have been used to interconnect input and output terminals (ports) located on opposite sides. To interconnect input-output terminals located on the same side, another kind of switching network, called the one-sided switching network, is used instead. For example, Fig. 1 shows a three-stage one-sided Clos network [1], [2] $C(n, m, s)$, which consists of s $CB(n, m)$ crossbars (at the first and third stages) interconnected by m triangular arrays (at the second stage). As we know, this $C(n, m, s)$ Clos network with $m \geq 2n - 1$ is a nonblocking network.

Through the arrangement of switches (or interconnects) in various combinations, different input-output terminals of a one-sided switching network can be connected to each other. Assuming that all *connections* are point-to-point, the enumeration of all pairs of input-output terminals to be connected is called an *assignment*, where an input (or output) terminal can appear in at most one pair of connections. An assignment is *realizable* if there exist in the network disjoint paths connecting all pairs of input-output terminals given in the assignment. A switching network is *rearrangeable* [2], [3], [4], [5], [6], [7] if any given assignment is realizable.

Studies on multistage switching networks are fruitful. Yen and Feng [4] proposed a class of $2 \log_2 N$-stage two-sided networks, which are equivalent to Benes networks. All networks in this class are nonblocking and rearrangeable. The one-stage one-sided rearrangeable switching networks have been discussed by Mitchell and Wild [5]; then, the reduction of crosspoints in the one-stage one-sided crosspoint switching network has been investigated by Varma and Chalasani [6]. Gordon and Srikanthan [7] studied another multistage one-sided switching network with many 2×2 switch elements. Chang et al. [8], [9], [10] proposed universal switch blocks to improve the routability in a Field Programmable Gate Array (FPGA) routing network. However, most of these studies are concerned with either the two-sided rearrangeable switching networks or the one-stage one-sided rearrangeable

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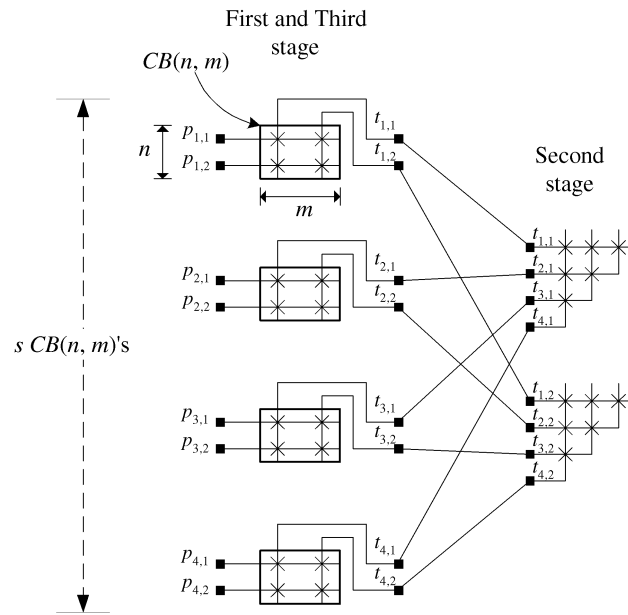
Fig. 1. A three-stage one-sided Clos switching network $C(n, m, s)$ with $n = 2$, $m = 2$, and $s = 4$.

switching networks. In this paper, we propose a new three-stage one-sided rearrangeable network, called the Polygonal Switching Network (PSN) [11], [12] for the bidirectional communication system. We investigate how to use this PSN to construct a rearrangeable switching network and how to minimize the number of switches in PSN. We also compare our PSN with a three-stage one-sided Clos switching network of the same size and with the same number of switches. We show that a $C(n, m, s)$ Clos switching network with $m \leq n$ is not rearrangeable.

The next section gives a description of the proposed PSN and some notation and definitions. Furthermore, we prove that the Clos switching network is not rearrangeable. Section 3 proves the rearrangeability of a PSN and Section 4 shows how to minimize the number of switches in a rearrangeable PSN. Conclusions are reported in Section 5.

2 POLYGONAL SWITCHING NETWORK

A three-stage one-sided polygonal switching network (PSN) consists of s crossbars (CBs) interconnected by an s-sided polygonal switch block (PSB) with $s \geq 3$. Fig. 2 shows an example of PSN with $n = 2$, $m = 2$, and $s = 4$, where the first and third stages are composed of four CBs and the second (internal) stage is a 4-sided PSB.

Each crossbar in a PSN, denoted as $CB_i(n, m)$ for $i = 1, 2, \ldots, s$, is an $n \times m$ block architecture having n external terminals $P_i = \{p_{i,1}, p_{i,2}, \ldots, p_{i,n}\}$ connected to the input-output ports and m internal terminals $T_i = \{t_{i,1}, t_{i,2}, \ldots, t_{i,m}\}$ connected to one side of PSB. Since we have two sets of terminals $\mathcal{P} = P_1 \cup P_2 \cup \cdots \cup P_s$ and $\mathcal{T} = T_1 \cup T_2 \cup \cdots \cup T_s$, a polygonal switching network can then provide $N = s \times n$ external terminals for interconnection. Through these $n \times m$ programmable and electrically noninteracting switches in a crossbar $CB_i(n, m)$, any external terminal in P_i can be connected to a free internal terminal in T_i without any blocking. For example, if switch $SW(p_{i,j}, t_{i,h})$ is programmed to be "ON," then connection $(p_{i,j}, t_{i,h})$ between an external terminal $p_{i,j}$ and an internal terminal $t_{i,h}$ is established.

The polygonal switch block in a PSN, denoted as $PSB(m, s)$, is an s-sided switch block with m (internal) terminals on each side of the block, as shown in Fig. 3a and
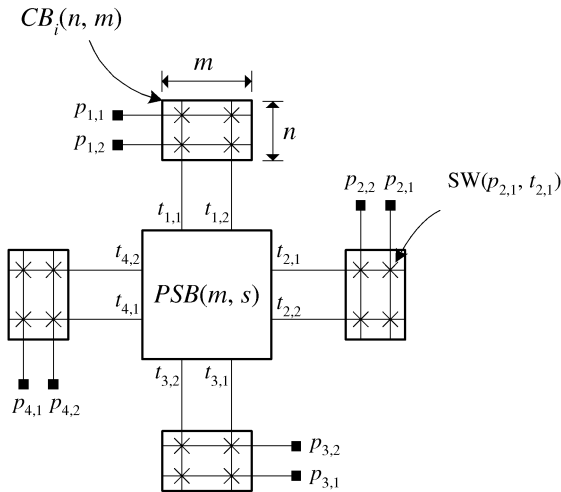
Fig. 2. A polygonal switching network $PSN(n,m,s)$ with $n=2$, $m=2$, and $s=4$.

Fig. 3d. Label the terminals on the ith side of a $PSB(m,s)$ as $T_i = \{t_{i,1}, t_{i,2}, \ldots, t_{i,m}\}$ for $1 \le i \le s$. Since a terminal in one side of the PSB should be connected to a terminal in any of the other $(s-1)$ sides through switches, a $PSB(m,s)$ needs $ms(s-1)/2$ switches. If a switch $SW(t_{i,j}, t_{k,l}), i \ne k$ is programmed to be "ON," then a connection between terminals $t_{i,j}$ and $t_{k,l}$ is established, as shown in Fig. 3a and Fig. 3d. To form a PSN, we need s $CB(n,m)$ crossbars connected to a $PSB(m,s)$. Thus, a $PSN(n,m,s)$ can be completely characterized by three parameters: n, m, and s.

In the following, we study two types of PSB, as shown in Fig. 3a and Fig. 3d. The PSB in Fig. 3a is equivalent to the two isolated triangular arrays in Fig. 3b, which is exactly the second stage of a Clos switching network in Fig. 1. And, this $PSB_C(m,s)$ is composed of m isolated $PSB_C(1,s)$, as shown in Fig. 3c. Fig. 4a shows a polygonal switching network $PSN_C(n,m,s)$ constructed with a $PSB_C(m,s)$, which can be used to implement a Clos switching network $C(n,m,s)$. Fig. 3d shows a universal polygonal

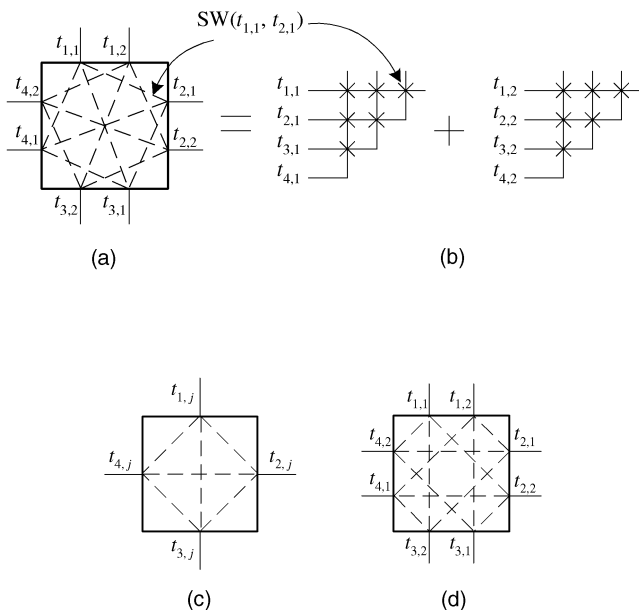Fig. 3. Two types of polygonal switch blocks $PSB(m,s)$ with $m=2$ and $s=4$. (a) A $PSB_C(m,s)$ and (b) its corresponding triangular arrays. (c) A $PSB_C(m,s)$ is equivalent to the m isolated $PSB_C(1,s)$. (d) A $PSB_U(m,s)$.
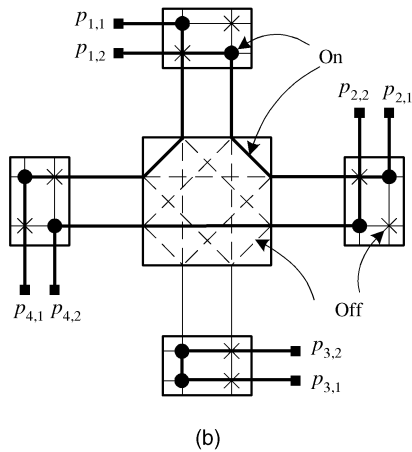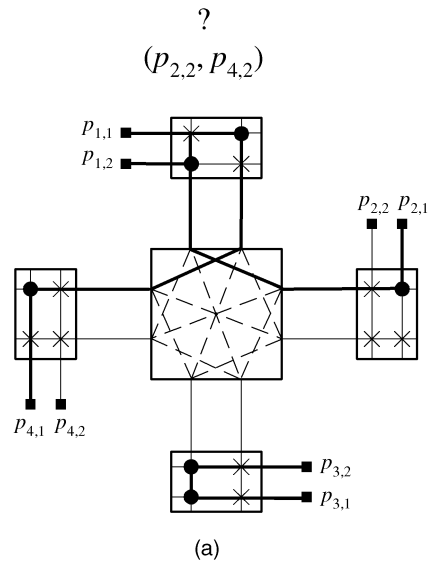

Fig. 4. Two types of polygonal switching networks $PSN(n,m,s)$ with $n=2$, $m=2$, and $s=4$. (a) A $PSN_C(n,m,s)$ implementation of the Clos switching network $C(n,m,s)$ in Fig. 1. (b) A $PSN_U(n,m,s)$.

switch block $PSB_U(m,s)$ proposed by Chang et al. [8], [9], [10]. A $PSN_U(n,m,s)$, consisting of s $CB(n,m)$ crossbars connected to a $PSB_U(m,s)$, is shown in Fig. 4b. Note both $PSN_U(n,m,s)$ and $PSN_C(n,m,s)$ have the same size and the same number of switches.

In a $PSN(n,m,s)$, any *connection pair* $(p_{i,j}, p_{k,l})$ is a point-to-point connection, where $p_{i,j}, p_{k,l} \in \mathcal{P}$. An assignment $AS = \{(p_{i,j}, p_{k,l})\}$ represents a set of connection pairs to be connected, where a terminal can appear in at most one pair. A $PSN(n,m,s)$ is *rearrangeable* if any assignment AS is *realizable* (*routable*). To examine whether a connection pair $(p_{i,j}, p_{k,l}) \in AS$ can be connected through $PSB(m,s)$, let us classify AS into two disjoint sets, $AS = AS_D \cup AS_S$, such that

$$AS_D = \{(p_{i,j}, p_{k,l}) : (p_{i,j}, p_{k,l}) \in AS \text{ and } i \ne k\}$$

and

$$AS_S = \{(p_{i,j}, p_{k,l}) : (p_{i,j}, p_{k,l}) \in AS \text{ and } i = k\},$$

where $p_{i,j}, p_{k,l} \in \mathcal{P}$, $1 \le i, k \le s$, and $1 \le j, l \le m$.

Note that a connection pair $(p_{i,j}, p_{k,l})$ belonging to AS_D is to be connected by passing through blocks $CB_i - PSB - CB_k$, while the
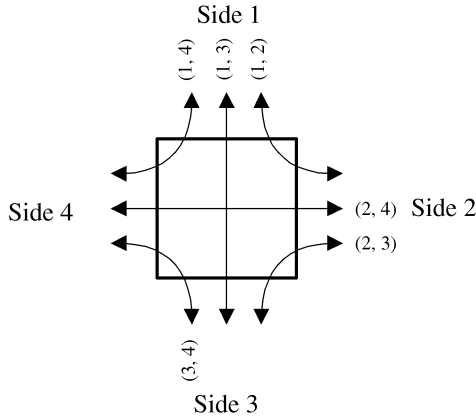
Fig. 5. Six possible types of connections in a four-sided switch block.

pair belonging to AS_S has to be connected through a CB only. In AS_D, each connection is accomplished using two sides of a $PSB(m,s)$; we can thus classify those connections passing through a $PSB(m,s)$ into $s(s-1)/2$ types of connections. Fig. 5 shows the six possible types of connections in a four-sided switch block. A *routing requirement vector (RRV)* $\vec{r}$ [8], [9], [10] for a $PSB(m,s)$ is an $s(s-1)/2$-tuple $(r_{1,2}, r_{1,3}, \ldots, r_{1,s}, r_{2,3}, \ldots, r_{2,s}, \ldots, r_{s-1,s})$, where $r_{i,k}$ represents the number of the connection pairs $(p_{i,j}, p_{k,l})$ required to be connected through $PSB(m,s)$ and $0 \le r_{i,k} \le m$ for $1 \le i < k \le s$. An RRV $\vec{r}$ is said to be *realizable (routable)* on a $PSB(m,s)$ if there exist disjoint paths for $\vec{r}$ on a $PSB(m,s)$. For example, Fig. 6a shows a routing instance with three nets corresponding to the RRV $\vec{r} = (1, 0, 1, 0, 1, 0)$ and we try to route this RRV using two different polygonal switch blocks $PSB_U(2, 4)$ and $PSB_C(2, 4)$. Instances of an RRV $(1, 0, 1, 0, 1, 0)$ routable on a $PSB_U(2, 4)$ are shown in Fig. 6b and Fig. 6c, where the routing solutions are illustrated by thick lines. As shown in Fig. 6d and Fig. 6e, however, there is always one net that cannot be routed on a $PSB_C(2, 4)$. Thus, this RRV $(1, 0, 1, 0, 1, 0)$ is not routable on a $PSB_C(2, 4)$.
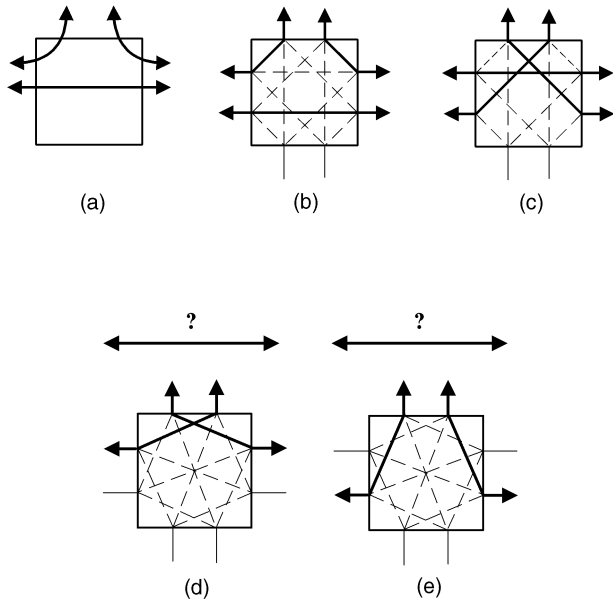

Fig. 6. Examples of routing on two four-sided switch blocks, each of the same size. (a) An RRV instance $(1, 0, 1, 0, 1, 0)$. (b) and (c) This RRV is routable on a $PSB_U(2, 4)$. (d) and (e) This RRV is not routable on a $PSB_C(2, 4)$.
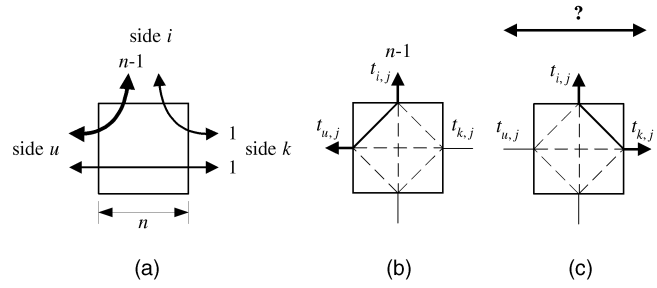

Fig. 7. An instance of RRV not routable on a $PSB_C(n, s)$. (a) An RRV instance $\vec{r} = (0, \ldots, 0, r_{i,k} = 1, 0, \ldots, 0, r_{i,u} = n-1, 0, \ldots, 0, r_{k,u} = 1, 0, \ldots, 0)$. (b) This $r_{i,u} = n-1$ is routable on $(n-1)$ isolated $PSB_C(1, s)$. (c) This $r_{i,k} = 1$ and $r_{k,u} = 1$ are not simultaneously routable on a $PSB_C(1, s)$.

Now, let $AS = \{(p_{1,1}, p_{4,1}), (p_{1,2}, p_{2,1}), (p_{2,2}, p_{4,2}), (p_{3,1}, p_{3,2})\}$ be routed on a $PSN_C(2, 2, 4)$ and a $PSN_U(2, 2, 4)$, as, respectively, shown in Fig. 4a and Fig. 4b. Decomposing $AS = AS_D \cup AS_S$, we have

$$AS_D = \{(p_{1,1}, p_{4,1}), (p_{1,2}, p_{2,1}), (p_{2,2}, p_{4,2})\}$$

and

$$AS_S = \{(p_{3,1}, p_{3,2})\}.$$

The RRV for routing AS_D on a $PSB(2, 4)$ is $\vec{r} = (1, 0, 1, 0, 1, 0)$. We show, in Fig. 4b, a possible routing solution for the given AS on a $PSN_U(2, 2, 4)$ switching network. For instance, Fig. 4a shows that the same AS is not routable on a $PSN_C(2, 2, 4)$ switching network because RRV $\vec{r} = (1, 0, 1, 0, 1, 0)$ contains at least one connection that cannot be routed on a $PSB_C(2, 4)$, as already shown in Fig. 6d and Fig. 6e. In the following, we prove that a $PSN_C(n, m, s)$ with $m \le n$ is not rearrangeable.

Theorem 1. *A $PSN_C(n, m, s)$ polygonal switching network is not rearrangeable for $m \le n$ and $s \ge 3$.*

Proof. Observably, if a $PSN_C(n, m, s)$ with $m = n$ is not rearrangeable, then a $PSN_C(n, m, s)$ with $m < n$ is not rearrangeable. Thus, we need to prove that a $PSN_C(n, n, s)$ is not rearrangeable.

Arbitrarily select three sides i, k, and u of a $PSN_C(n, n, s)$, $1 \le i < k < u \le s$, we form an assignment

$$AS = AS_D$$
$$= \{(p_{i,1}, p_{u,1}), (p_{i,2}, p_{u,2}), \ldots, (p_{i,n-1}, p_{u,n-1}), (p_{i,n}, p_{k,n}), (p_{k,1}, p_{u,n})\}$$

to be connected between the P_i, P_k, and P_u on a $PSN_C(n, n, s)$. The RRV for routing AS_D on a $PSB_C(n, s)$ is $\vec{r} = (0, \ldots, 0, r_{i,k} = 1, 0, \ldots, 0, r_{i,u} = n-1, 0, \ldots, 0, r_{k,u} = 1, 0, \ldots, 0)$ as shown in Fig. 7a. Since a $PSB_C(n, s)$ is equivalent to n isolated $PSB_C(1, s)$s, the first $r_{i,u} = (n-1)$ can be realizable on $(n-1)$ isolated $PSB_C(1, s)$s, as shown in Fig. 7b. But, we cannot find enough disjoint paths to simultaneously realize an $r_{i,k} = 1$ and an $r_{k,u} = 1$ on the last $PSB_C(1, s)$, as shown in Fig. 7c. Thus, this AS cannot be realizable on a $PSN_C(n, n, s)$ because this RRV $\vec{r}$ contains at least one connection that cannot be routed on a $PSB_C(n, s)$. Therefore, the $PSN_C(n, n, s)$ is not rearrangeable. □

3   REARRANGEABILITY OF PSN

A polygonal switch block $PSB(m, s)$ is said to be *universal* [8], [9], [10] if any RRV $\vec{r} = (r_{1,2}, r_{1,3}, \ldots, r_{s-1,s})$ satisfying the dimensional constraint is *realizable* on this $PSB(m, s)$. The dimensional constraint for a $PSB(m, s)$ is that the number of connections interconnecting through each side of $PSB(m, s)$ cannot exceed m

[8], [9], [10]. A generic *universal* switch block has been proposed by Shyu et al. [10]. Furthermore, they presented an algorithm to construct an s-sided universal switch block with m terminals on each side. We use this algorithm to construct a universal $PSB_U(m, s)$ for our $PSN_U(n, m, s)$. Based on the universality of $PSB_U(m, s)$ and the properties of a crossbar $CB(n, m)$, we proceed to prove the rearrangeability of a $PSN_U(n, m, s)$.

Theorem 2. *A $PSN_U(n, m, s)$ polygonal switching network is rearrangeable if and only if $m \geq n$.*

Proof. Observably, if a $PSN_U(n, m, s)$ with $m = n$ is rearrangeable, then a $PSN_U(n, m, s)$ with $m \geq n$ is rearrangeable. Thus, we need to prove that a $PSN_U(n, n, s)$ is rearrangeable.

(If) A $PSN_U(n, n, s)$ is rearrangeable if any assignment $AS = AS_D \cup AS_S$ is realizable. First, we prove that AS_D is realizable on a $PSN_U(n, n, s)$. Since each connection pair $(p_{i,j}, p_{k,l}) \in AS_D$, $i \neq k$, is connected by passing through blocks $CB_i - PSB - CB_k$. Furthermore, we observe that the RRV $\vec{r}$ for AS_D satisfying the dimension constraint is also realizable on a *universal* $PSB_U(n, s)$ since the number of connection pairs interconnecting through each side of $PSB_U(n, s)$ does not exceed n. Therefore, for each $(p_{i,j}, p_{k,l}) \in AS_D$, we can find a connection path $(t_{i,q}, t_{k,n-q+1})$ in a $PSB_U(n, s)$ because its RRV $\vec{r}$ is realizable on a $PSB_U(n, s)$, where $1 \leq q \leq n$. The last thing to do is to program the two switches $SW(p_{i,j}, t_{i,q})$ and $SW(p_{k,l}, t_{k,n-q+1})$ in the $CB_i(n, n)$ and $CB_k(n, n)$, respectively. Then, we have all the connection pairs $(p_{i,j}, p_{k,l}) \in AS_D$ connected by $PSN_U(n, n, s)$. That is, AS_D is realizable on a $PSN_U(n, n, s)$.

Next, we consider the AS_S connections on a $PSN_U(n, n, s)$ after the AS_D ones have been realized on a $PSN_U(n, n, s)$. For each connection pair $(p_{i,j}, p_{i,l}) \in AS_S$, we can find a terminal $t_{i,h} \in T_i$ (truly, at least two terminals) in the $CB_i(n, n)$ which is not in use by AS_D. And, this connection pair $(p_{i,j}, p_{i,l})$ can be connected by programming two switches $SW(p_{i,j}, t_{i,h})$ and $SW(p_{i,l}, t_{i,h})$ in the $CB_i(n, n)$. Therefore, AS_S is realizable through s $CB_i(n, n)$s of a $PSN_U(n, n, s)$.

Hence, any assignment $AS = AS_D \cup AS_S$ is realizable on a $PSN_U(n, n, s)$. That is, a $PSN_U(n, m, s)$ polygonal switching networks with $m \geq n$ is rearrangeable.

(Only If) If, in a $PSN_U(n, m, s)$ with $m < n$, we have an assignment $AS = AS_D = \{(p_{i,1}, p_{k,1}), (p_{i,2}, p_{k,2}), \ldots, (p_{i,n}, p_{k,n})\}$ to be connected between the P_i and P_k on a $PSN_U(n, m, s)$, $i \neq k$. Since each connection pair $(p_{i,j}, p_{k,l}) \in AS$ is connected by passing through blocks $CB_i - PSB - CB_k$. In each $CB_i(n, m)$, we cannot find enough disjoint paths to connect all the n external terminals in P_i to all the m internal terminals in T_i, which in turn are connected to the ith side of a $PSB_U(m, s)$ due to $m < n$. Thus, this AS is not realizable on a $PSN_U(n, m, s)$ with $m < n$. □

4 SWITCHES EFFICIENCY OF PSN

We have shown the rearrangeability of our $PSN_U(n, n, s)$ in Section 3. Now, we start to explore the effect of the parameters s and n in a $PSN_U(n, n, s)$ on the switch-efficiency and we try to find proper s and n values to minimize the number of switches needed in a rearrangeable $PSN_U(n, n, s)$ to interconnect $N = s \times n$ input-output terminals.

Since the number of switches in s $CB(n, n)$ crossbars is equal to $s \times n^2$, the number of switches in a $PSB_U(n, s)$ is equal to $ns(s - 1)/2$. Denote the number of switches in a $PSN_U(n, n, s)$ as $SW(n, n, s)$. By summing the number of switches in all the above blocks, we have:

$$SW(n, n, s) = sn^2 + \frac{ns(s - 1)}{2}. \tag{1}$$

Substituting $n = N/s$ into (1) results in

$$SW(n, n, s) = \frac{N^2}{s} + \frac{Ns}{2} - \frac{N}{2}. \tag{2}$$

This indicates that the function $SW(n, n, s)$ has minimum value at $s = \sqrt{2N}$,

$$SW(n, n, \sqrt{2N}) = \sqrt{2}N^{3/2} - \frac{N}{2}. \tag{3}$$

From (3), we have that a $PSN_U(n, n, s)$ with $s = \sqrt{2N}$ contains the number of switches to a minimum. Furthermore, the $SW(n, n, s)$ is proportional to $N^{3/2}$.

5 CONCLUSIONS

This paper proposed a three-stage one-sided rearrangeable polygonal switching network $PSN_U(n, m, s)$, which consists of s $CB(n, m)$ crossbars interconnected by a universal polygonal switch block $PSB_U(m, s)$ with s sides. We not only provide the designers with a rearrangeable $PSN_U(n, m, s)$, where $m \geq n$ for interconnecting $N = s \times n$ input-output ports, but also show what value of s can be used to minimize the number of switches needed in a network. Besides, this polygonal switching network has been successfully applied to the design of a Field Programmable Interconnection Chip (FPIC) for interconnecting FPGAs in a symmetric multi-FPGA system [11], [12], [13].

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