

# An Auto- $I/Q$ Calibrated CMOS Transceiver for 802.11g

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**Abstract**—The CMOS transceiver IC exploits the superheterodyne architecture to implement a low-cost RF front-end with an auto- $I/Q$  calibration function for IEEE 802.11g. The transceiver supports  $I/Q$  gain and phase mismatch auto tuning mechanisms at both the transmitting and receiving ends, which are able to reduce the phase mismatch to within  $1^\circ$  and gain mismatch to 0.1 dB. Implemented in a  $0.25\ \mu\text{m}$  CMOS process with 2.7 V supply voltage, the transceiver delivers a 5.1 dB receiver cascade noise figure, 7 dBm transmit, and a 1 dB compression point.

**Index Terms**—Auto calibration, DC offset cancellation, gain mismatch, phase mismatch, RF transceiver, 802.11g.

## I. INTRODUCTION

IN THE MARKET of wireless local area networks (WLANs), high data-rate transmission has been the trend. IEEE 802.11g standard works at 2.4 GHz ISM band and supports data rates up to 54 Mb/s using OFDM modulation [1]. To achieve the desired performance upper bound, it is crucial to deliver a close match of  $I$  and  $Q$  signals in both the modulator and the demodulator. Solutions on in-phase and quadrature ( $I/Q$ ) gain and phase mismatch compensation can be classified into three types. The first type uses a fully digital compensation technique. For example, Eberle *et al.* [2] presented a digital compensation architecture for the  $I/Q$  mismatch problem that occurred in a digital receiver. The second type uses baseband plus RF front-end to calibrate the gain and phase mismatch. For example, baseband signal processing techniques have been used to generate a test signal to the RF front-end [3], [4]. Since the output of the RF front-end running this test signal will give information on the  $I/Q$  mismatch, the baseband can sense this output to determine a control code for the front-end circuits to compensate the  $I/Q$  mismatch. But the RF front-end and baseband circuits are often developed independently, and thus, implementing the second type of calibration is not possible. The third type does not require any baseband support. For example, the 802.11a/b/g transceiver presented by Ahola *et al.* [5] achieved an accuracy quadrature phase through careful analysis and design of the  $I/Q$  generation parts of the local oscillator. Another approach of this type has been presented by Hsieh *et al.* [6]; an auto- $I/Q$  calibrated transceiver with no more than 5% additional chip area for the calibration circuitry.

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This paper gives a more detailed description of [6], especially on the auto-calibration mechanism and calibration circuits design.

## II. SYSTEM ARCHITECTURE

Fig. 1 illustrates the overall transceiver architecture. At the receiver front-end, a single-ended input, two-stage low-noise amplifier (LNA) is followed by an image-reject mixer and a polyphase filter. A CMOS analog switch (SW5) is used to drive the off-chip SAW filter. From IF to baseband, the IF signal flows through a CMOS analog switch (SW4) to a two-mode (RX/TX) variable gain amplifier (VGA), followed by an in-phase and quadrature ( $I/Q$ ) down-conversion mixer and a fifth-order Bessel filter. The VGA and the Bessel filter are reused in both the receiving and transmitting paths through SW3, SW4, and SW6 to reduce the total transceiver die area. To remove the demodulator DC offset, a continuous feedback DC offset cancellation loop is designed as shown in Fig. 1: One of the differential RX  $I$  output (RX  $Q$  output) DC signal is extracted by the  $RC$  low pass filter. This extracted DC voltage will be compared with the common mode voltage  $V_{cm}$  of RX  $I$  output (RX  $Q$  output). The resulted DC offset voltage will create an offset current on buffer output; this offset current flows through the resistors' load of mixer and generates a compensated offset voltage.

As shown in Fig. 1, the transmitting path begins with an input buffer, followed by a Bessel low-pass filter (LPF). A traditional Gilbert-cell double-balance mixer, succeeding LPF through SW2, is used to up-convert the baseband signal to IF frequency. The transmitter (TX) output power range is determined by the dual-mode VGA gain that varies from  $-23$  dBm to 2 dBm. The TX shares the same SAW filter with the receiver using on-chip CMOS analog switches SW4 and SW5, which are designed to have a differential output impedance of  $200\ \Omega$ . A differential-to-single Gilbert-cell mixer drives a single-ended, two-stage preamplifier that was designed to have 15 dB gain and 7 dBm output  $P_{1dB}$ .

An integer- $N$  phase-locked loop (PLL) operates with a 1 MHz reference frequency, which is derived from the system reference frequency generated by an external 40 MHz crystal oscillator. Three additional capacitor arrays in parallel with the tank circuits are used to tune the RF VCO frequency from about 1930 to 2210 MHz. The calibration of the center frequency is performed when the channel changes. The quadrature local signals for the image-reject RF mixer are generated by the two-stage polyphase filter. The IF PLL is implemented with an integer- $N$  structure using the same reference frequency as

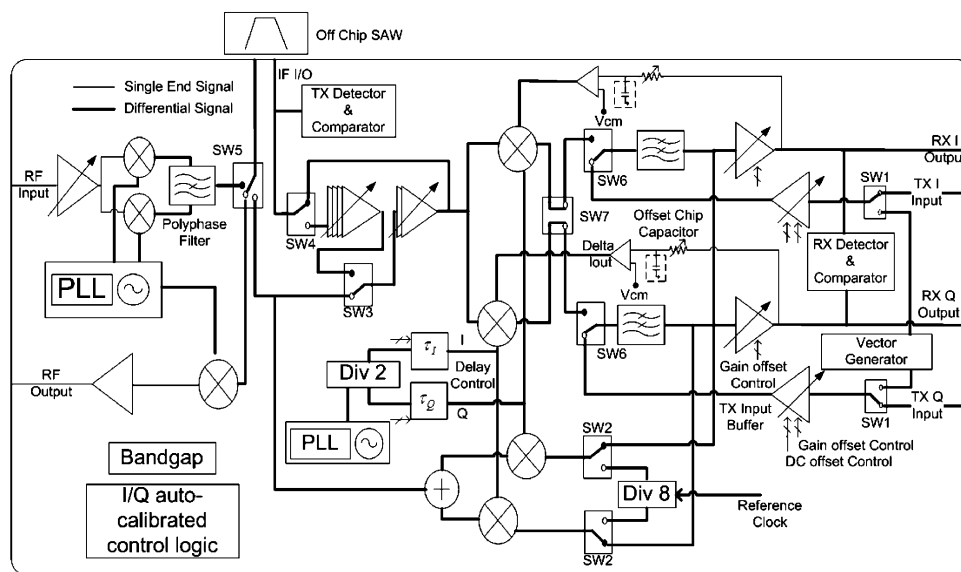


Fig. 1. Transceiver diagram.

the RF PLL. Since the IF VCO oscillation frequency is 748 MHz, it is divided by two to create the 374 MHz quadrature IF local signals. The RF and IF VCO's have phase noises of  $-116$  dBc/Hz and  $-120$  dBc/Hz, respectively, at a 1 MHz offset.

### III. AUTO- $I/Q$ CALIBRATION ALGORITHMS

The auto- $I/Q$  calibration is performed when powered up to correct the process-related imperfections on  $I/Q$  mismatch; when temperature conditions change, the baseband processor can trigger the radio auto- $I/Q$  calibration through the three wire series interface. But the measured results, which are the circuits without recalibrations, show that the degradation of EVM is less than 1.5% on the different temperatures. To reduce the overall current consumption, all the calibration circuits will be turned off after the calibration. The overall calibration flow starts from TX DC-offset cancellation, then to TX  $I/Q$  gain, and finally to TX  $I/Q$  phase. The RX  $I/Q$  gain and RX  $I/Q$  phase calibrations will be performed after all the TX calibrations, because the RX calibrations need to use a test tone from the calibrated TX.

The DC-offset cancellation process needs to be executed first. As shown in Fig. 1, a switch SW1 on both the  $I$  and  $Q$  paths switches the input of TX input buffer from the baseband to the vector generator, and a DC test vector  $(0, V_T)$  or  $(V_T, 0)$  is applied to the TX  $I/Q$  input in different time slots, and different signal power levels caused by the  $I/Q$ -path gain mismatch will appear on the modulator output. The peak detector then is used to sense which test vector will give a higher output power on the modulator. And the comparator output gives information on which path of the modulator has less gain. A 4-bit gain-controlled TX input buffer is designed to compensate for the gain mismatch. The gain of the TX input buffer is then increased step by step on the smaller gain path. When the S/C comparator changes its output polarity, the  $I/Q$  path gain becomes balanced and the gain calibration process stops.

The ideal input DC test vectors  $(0, V_T)$  and  $(V_T, 0)$  become invalid under the existence of DC offset and vector mismatch, and thus we use equivalent test vectors  $(0, V_T)$  and

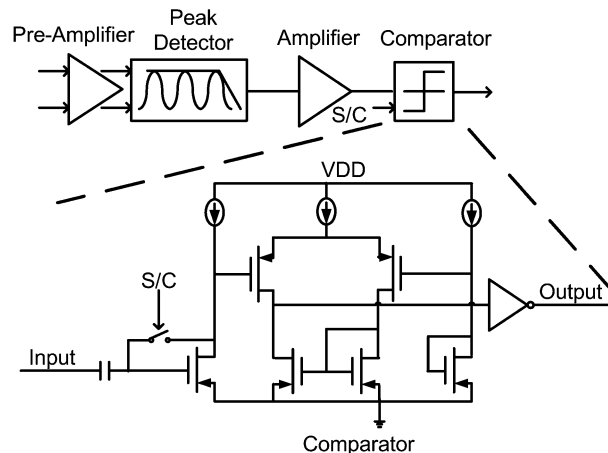


Fig. 2. Architecture of TX detector and comparator.

$I/Q$  path DC-offset cancellation is performed in the following sequence:  $I$  path  $\rightarrow$   $Q$  path  $\rightarrow$   $I$  path. A  $-40$  dBc TX local leakage can be achieved using this algorithm.

The basic idea of TX  $I/Q$  gain mismatch calibrations is from [7]. The proposed transmitter architecture implements this idea with only 2.5% additional chip area. A DC test vector  $(0, V_T)$  or  $(V_T, 0)$  is applied to the TX  $I/Q$  input in different time slots, and different signal power levels caused by the  $I/Q$ -path gain mismatch will appear on the modulator output. The peak detector then is used to sense which test vector will give a higher output power on the modulator. And the comparator output gives information on which path of the modulator has less gain. A 4-bit gain-controlled TX input buffer is designed to compensate for the gain mismatch. The gain of the TX input buffer is then increased step by step on the smaller gain path. When the S/C comparator changes its output polarity, the  $I/Q$  path gain becomes balanced and the gain calibration process stops.

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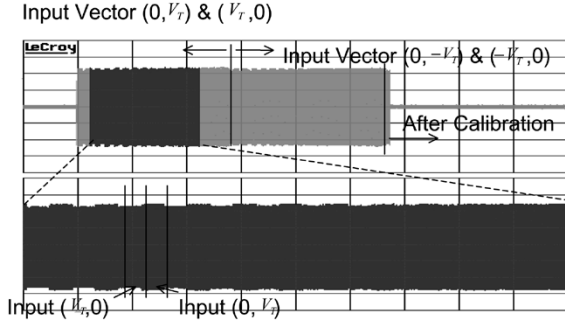


Fig. 3. Measured TX gain calibration.

$(V_T + \Delta V_T, 0 + \Delta DC)$  instead. But error can be eliminated by averaging the 4-bit TX buffer DAC values between input vectors  $(0, V_T)$  and  $(V_T, 0)$ ; and  $(0, -V_T)$  and  $(-V_T, 0)$ .

The TX gain calibration result is shown in Fig. 3. To track the IF output signal response when the circuits are auto-calibrating, the IF signal is down converted into a 5 MHz signal as shown in Fig. 3. The calibration process is divided into two segments. The first segment of calibration is performed with input vectors  $(0, V_T)$  and  $(V_T, 0)$ , then the second segment of calibration is performed with input vectors  $(0, -V_T)$  and  $(-V_T, 0)$ . The difference voltage swings are caused by the difference of gains obtained from the  $I$  and  $Q$  signal paths. During the calibration, voltage swings become smaller and smaller; finally when the voltage swings obtained at consecutive time slots are close to each other, the calibration will stop. After the calibration, the gain mismatch is reduced from about 0.4 dB to less than 0.1 dB.

After the gain mismatch calibration, a phase calibration is performed; the algorithm for phase calibration is similar to the TX gain calibration algorithm. The test vector is changed to  $(V_T, V_T)$  and  $(V_T, -V_T)$  instead of  $(0, V_T)$  and  $(V_T, 0)$  in different time slots. Local quadrature mismatch causes different output power levels on the modulator output in different time slots. An extra delay is added on the local (delay-cell) buffer [8] to balance the delay. When the comparator output changes its polarity, the calibration loop stops. The existing DC offset and gain mismatch on  $I/Q$  paths will generate an error in the phase calibration result, which is about  $0.54^\circ$  under a DC offset of  $-40$  dBc and a gain mismatch resolution of 0.1 dB. The resolution of phase delay in local buffer [8] is  $0.5^\circ$ , and thus the equivalent resolution of the quadrature mismatch is about  $1.04^\circ$ .

For the receiver  $I/Q$  mismatch calibration, a single tone is generated from the transmitter and is applied to the receiver demodulator. After down-conversion, a 5 MHz signal appears on the demodulator  $I/Q$  output. Fig. 4 shows both the gain and phase imbalance detection-and-comparison mechanisms. During the RX gain mismatch calibration, RSW1 changes the input from  $I$  path to  $Q$  path in different time slots. The comparator samples the  $I$  path signal and holds it to compare with the  $Q$  path signal. A compensated gain is added to the related path after the  $I/Q$ -auto calibration control logic senses the comparator output. A sequential search algorithm is used here and calibration will stop when the comparator changes its output polarity.

As shown in Fig. 1, a single-tone signal is generated as follows. A 5 MHz  $Q$  signal, obtained by dividing the 40 MHz ref-

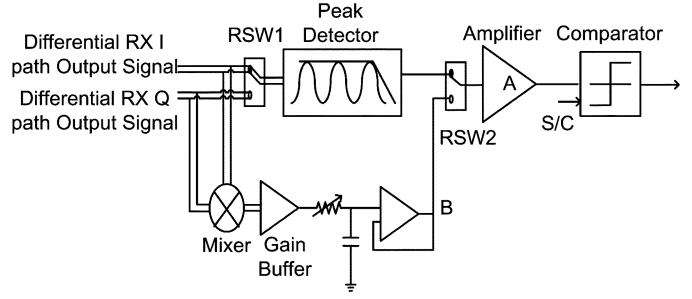


Fig. 4. Architecture of RX detector and comparator.

erence clock by 8, is applied to the up-conversion mixer through SW2. A 379 MHz signal is created after up-conversion with a single-sideband (SSB) suppression of higher than  $-40$  dBc. Finally, this single tone will loop back to the receiver through SW5.

The nonideal SSB generator in the transmitter will cause error during the RX gain mismatch calibration. Assume that the ratio of the image signal to the test tone signal is SSB, the peak detector output as shown in Fig. 4 is

$$V_{Ip} \approx \frac{1}{2} \times A - \frac{1}{2} \times A \times \text{SSB},$$

when RSW1 switches to the I path input (1)

$$V_{Qp} \approx \frac{1}{2} + \frac{1}{2} \times \text{SSB},$$

when RSW1 switches to the Q path input (2)

and

$$\begin{aligned} \text{compensated gain: } \Delta G_1 &= V_{Qp} - V_{Ip} \\ &= \frac{1-A}{2} + \frac{1+A}{2} \times \text{SSB} \approx \frac{1-A}{2} + \text{SSB} \end{aligned} \quad (3)$$

where  $A$  is the  $I/Q$  path gain ratio ( $A = 1$  in a balanced gain case).

The purpose of RX gain calibration is to compensate the gain imbalance caused by the term  $(1-A)$ , but in this case the image signal in SSB will affect the calibration result. To eliminate this effect, the gain calibration has to be performed once again with swapped  $I/Q$  path signals by setting the RSW7 switch that follows the second  $I/Q$  down-conversion mixers: these two mixers are placed physically very close to each other, thus the gain mismatch here can be ignored. The peak detector output then becomes

$$V_{Ip} \approx \frac{1}{2} - \frac{1}{2} \times \text{SSB},$$

when RSW1 switches to the I path input (4)

$$V_{Qp} \approx \frac{1}{2}A + \frac{1}{2} \times A \times \text{SSB},$$

when RSW1 switches to the Q path input (5)

and

$$\begin{aligned} \text{compensated gain: } \Delta G_2 &= V_{Ip} - V_{Qp} \\ &= \frac{1-A}{2} - \frac{1+A}{2} \times \text{SSB} \approx \frac{1-A}{2} - \text{SSB}. \end{aligned} \quad (6)$$

Combining (3) and (6), the obtained result contains only the  $(1-A)$  term, the effect of SSB is thus eliminated.

For the RX phase mismatch calibration, the  $I/Q$  signals are mixed together through the mixer circuit as shown in Fig. 4.

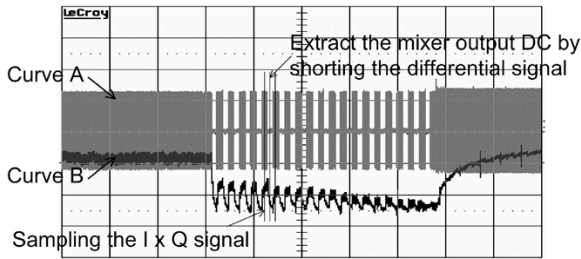


Fig. 5. Measured RX quadrature phase calibration.

When there is  $I/Q$  mismatch, a DC signal appears on the output of this mixer. The S/C comparator compares the DC operating point at the output of the gain buffer with the DC level obtained after the mixing of  $I/Q$  signals. The logic output of the comparator gives information on which quadrature local signal needs to add an extra delay to compensate the quadrature mismatch. The algorithm is similar to the TX phase calibration one, and an extra delay is implemented by a local delay-cell buffer [8] after the quadrature generator.

In this RX phase mismatch calibration case, the nonideal gain mismatch and SSB test tone will not affect the calibration result. The mixer output as shown in Fig. 4 is as follows:

$$\begin{aligned} &\text{Signal on mixer output } V_{\theta} \\ &\approx G \times \left( \frac{1}{4} \times A \times \text{SSB}^2 + \frac{1}{4} \times A + \frac{1}{4} \times A \times \text{SSB} \right) \times \sin(\theta) \end{aligned} \quad (7)$$

where  $G$  is the gain of the mixer and  $\theta$  is the quadrature mismatch vector. From (7), since both  $A$  and SSB are coefficients of  $\sin(\theta)$  only, they do not affect the calibration target, and it is thus easy to push  $V_{\theta}$  to 0.

Fig. 5 shows the RX phase mismatch calibration result. Curve A shows the RX  $I$  path signal output and curve B shows the voltage of node B in Fig. 4. Values of the DC voltages on curve B are caused by the quadrature phase mismatches in different time slots. During the calibration, after a compensated phase delay is added to the quadrature local signal through the delay cell [8], the difference on two consecutive DC voltages becomes smaller and smaller, until the S/C comparator output changes its output polarity and thus the calibration process stops. After quadrature phase mismatch calibration, the quadrature phase error is reduced from about  $3^{\circ}$  to less than  $1^{\circ}$ .

#### IV. IMPLEMENTATION OF $I/Q$ AUTO-CALIBRATION CIRCUITRY

The detector and comparator circuits used in TX  $I/Q$  calibration are shown in Fig. 2, where a comparator is used to sense the DC offset on the peak detector output under different input test vectors. To relax the resolution requirement of this comparator, a fixed-gain amplifier is placed before the peak detector, and a DC-gain amplifier is added between the peak detector and the comparator. The resolution of the comparator designed for  $I/Q$  gain calibration is

$$0.64 \text{ mV}_{(1)} \times 10_{(2)} \times 0.85_{(3)} \times 4_{(4)} = 12.8 \text{ mV} \quad (8)$$

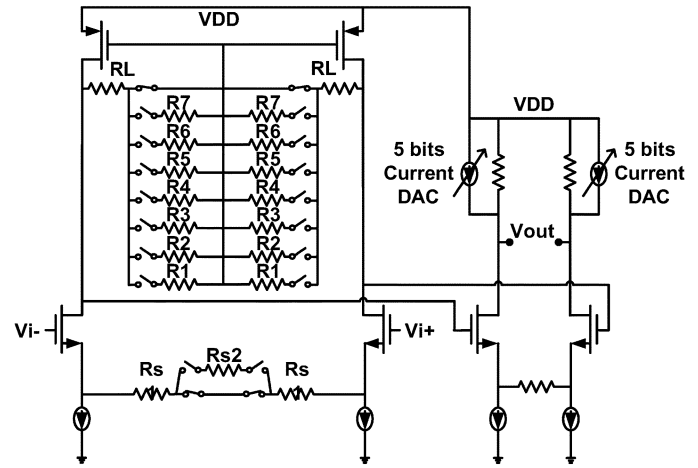


Fig. 6. Simplified circuit of TX input buffer with gain and dc offset tuning.

where

- (1) is the swing of 0.1 dB difference given an IF output power of  $-15$  dBm. A close loop is implemented here through the TX gain control VGA to lock the IF output power when TX is under gain and phase calibrating;
- (2) is the gain of the fixed-gain amplifier between the IF output and the peak detector;
- (3) is the gain of the peak detector given an IF frequency input;
- (4) is the gain of the DC-gain amplifier between the peak detector and the comparator.

From (8), without considering the factors of fixed-gain and DC-gain amplifiers, resolution of the comparator becomes 0.544 mV. With the same architecture, the calculated resolution of the comparator used in phase calibration under  $0.5^{\circ}$  resolution is 3 mV. That is, our designed comparator meets the sensitivity requirement of 3 mV. The comparator used for RX calibration is the same as this TX comparator and under the same relaxed resolution requirement.

The circuit of a TX input buffer for gain and DC-offset tuning is shown in Fig. 6, where switch resistors are used for gain tuning with 0.05 dB resolution, and a current DAC is used to create offset current with its resistor load and to generate the compensated DC voltage.

The circuit of a delay cell buffer is from Der *et al.* [8]. To obtain a signal delay, a current DAC is used to control the bias current on the delay path and the forward path, and different bias current conditions on these two paths will generate different signal delays. A disadvantage of this circuit is its output swing will change under different current bias conditions. Since different output swings on the  $I$  and  $Q$  local signals will cause different mixer conversion gains in both the TX/RX chains, a limiter is placed after the delay cell to solve this problem.

#### V. MEASURED RESULTS

A fully integrated 802.11g transceiver die microphotograph is shown in Fig. 7. The PLL performance is shown in Fig. 8 with an integrated phase noise measured on TX output from 10 kHz to 10 MHz is  $1.7^{\circ}$ . Calibrations for  $I/Q$  mismatch and DC offset were performed in an on-chip auto-tuning loop. After

TABLE I  
PERFORMANCE SUMMARY OF THE CHIP

Parameter	Measured result
Supply Voltage	2.7V ~ 3.3V
Supply Current	
RX mode	150mA
TX mode	120mA
RX chain noise figure	5.1dB
RX chain max gain/min gain	109dB/20dB
RX Chain IIP3 (min gain)	0dBm
I/Q amplitude error on TX/RX (after calibration)	0.1dB
I/Q phase error on TX/RX (after calibration)	1°
TX OP1dB	7dBm
TX EVM (-4dBm output power)	3.2%
LO integration noise (10KHz to 10MHz)	1.7°
Technology	0.25um 1P5M CMOS
Die size	10.2mm <sup>2</sup>

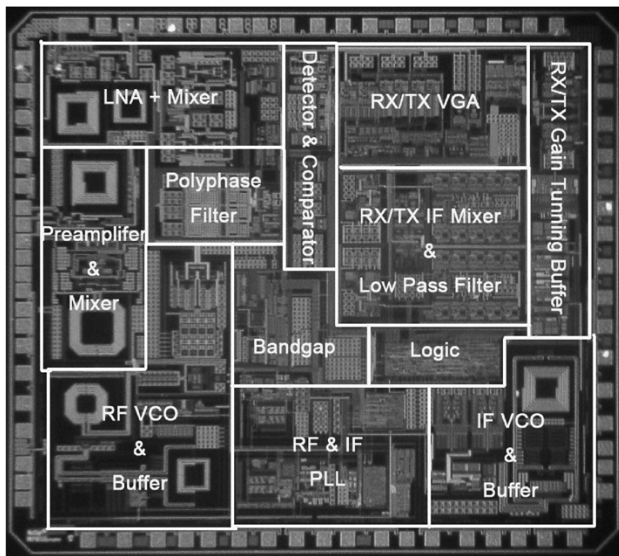


Fig. 7. Die microphotograph (3.4 mm × 3 mm).

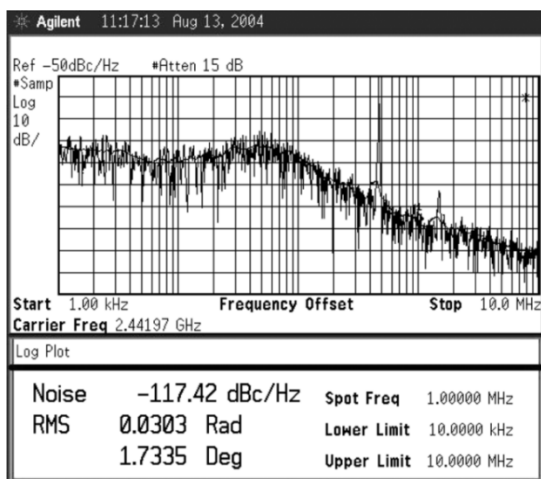


Fig. 8. Measured integrated phase noise on TX output.

the TX DC offset, *I/Q* gain, and *I/Q* phase calibrations, the transmitter EVM, as shown in Fig. 9, is about 3.2% at -4 dBm

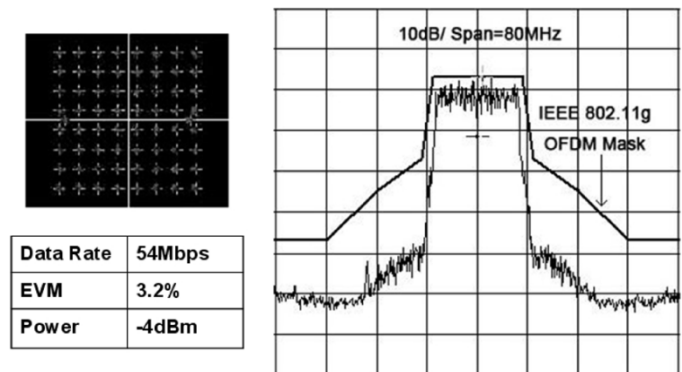


Fig. 9. Measured constellation diagram and spectra.

output. The receiver features a noise figure  $NF = 5.1$  dB. The receive IIP3 at minimum gain is 0 dBm. The maximum and minimum gains of receiver are 109 dB and 20 dB, respectively. The receiver EVM for the 54-Mb/s mode is about 4% after the RX *I/Q* gain and phase calibrations. The typical measurement results are summarized in Table I.

## VI. CONCLUSION

The presented transceiver supports a self-calibration mechanism for tuning both the receiver and the transmitter *I/Q* mismatches. Using the proposed innovative architecture, CMOS process-related imperfections on *I/Q* mismatch can be corrected such that the designed transceiver exceeds the standard specifications by a wide margin. The overhead of all the additional circuits needed for auto-calibration is just 5% of the total die area. The transceiver also features a good performance on both the receiving and the transmitting ends. Furthermore, the techniques presented in this paper can be extended to calibrate *I/Q* mismatch and DC offset in a zero-IF transceiver.

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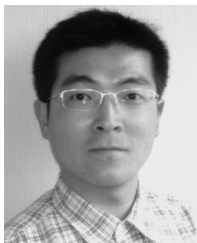
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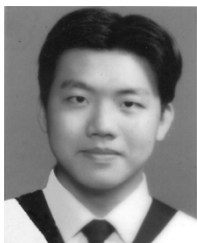
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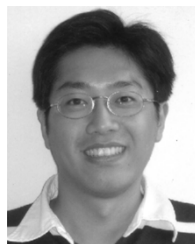
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