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TWO-DIMENSIONAL SIMULATION ON THE ELECTRIC FIELD SPIKE OF INDIUM ANTIMONIDE CHARGE INJECTION DEVICES

CHAO-WEN WU and HAO-HSIUNG LIN
Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan, R.O.C.

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Abstract—The surface breakdown induced by the electric-field spike existing in the gate overlay region and the device perimeter region is suspected to be one of the main factors which limit the charge storage capacity of a narrow bandgap InSb dual-gate metal–insulator–semiconductor (MIS) charge injection device (CID). In this study, a two-dimensional theoretical simulation is used to investigate the effect of device parameters, including bias voltage, oxide thickness, gate structure, gate overlay length, and field oxide thickness on the electric-field spike height in an InSb CID. In addition, it is found that a graded oxide structure can be used to lower the electric field spike.

NOTATION

ϕ_s	surface potential (V)
ϵ_0	vacuum permittivity (8.854×10^{-14} F/cm)
ϵ_{ox}	permittivity of SiO_2 ($3.9\epsilon_0$ F/cm)
ϵ_s	permittivity of InSb ($17.78\epsilon_0$ F/cm)
N_D	donor concentration (cm^{-3})
V_{FB}	flat-band voltage (V)
E_y^s	y-direction component of the electric field of InSb (V/cm)
E_y^{ox}	y-direction component of the electric field of SiO_2 (V/cm)
E_y^0	y-direction component of the electric field of the free space (V/cm)
ρ	charge density (cm^{-3})
V	potential variable in Poisson's equation (V)
q	electronic charge (1.6022×10^{-19} C)
k	Boltzmann constant (1.38×10^{-23} J/K)
T	temperature (K)
d_1, d_2	oxide thickness (cm or Å)
V_1, V_2	gate bias (V)
E, E_x, E_y	electric field intensity (V/cm)

1. INTRODUCTION

The indium antimonide (InSb) dual-gate charge-injection device (CID) is a favorite basic element for 2-D focal plane arrays (FPAs), which is suitable for the 3–5 μm IR detection window[1–4]. Because of the narrow bandgap, the surface-band-bending-induced tunneling effect plays an important role in the breakdown mechanisms of InSb dual-gate CID capacitors[5–9]. Anderson calculated theoretically the relation between surface band bending (ϕ_s), i.e. surface potential, and tunneling-current level [5, 6]. However, the calculation was done for a one-dimensional device only. For a real device, the anomalous surface-electric-field spike induced by the edge fringing-field effect[10] may further degrade the surface breakdown voltage. In this study, the electric-field spike taking place in the overlay region and the perimeter region of an InSb dual-gate CID was numerically analyzed in order to understand the effect of the device parameters, including bias voltage, oxide thickness, gate overlay length and field oxide thickness on the electric-field spike height. In addition, a design with a linear graded oxide[11] inserted between the gates was studied. The simulation results show that the spike height is lowered in this structure.

2. NUMERICAL ANALYSIS

There are two regions where the electric-field spike may exist. They are the overlap region of the gates, and the perimeter region of the whole CID unit cell. In the perimeter region, the unit cell is isolated using either field oxide or field plate[3, 4]. In the case of field-plate isolation, the structure is the same as that of the overlay region, i.e. dual-gate structure. The dual-gate structure consists of two adjacent MIS gates which are row and column gates in the central overlay region, or a field plate and one of the row and column gates in the perimeter region. The schematic diagram is shown in Fig. 1(a). Figure 1(b) shows the schematic diagram of the structure of field oxide isolation. The structure consists of the thick field oxide, one metal gate, and a conducting path which is on the top of the field oxide and is connected to the gate.

The metal used in these structures was Au/Cr. The oxide material was SiO_2 with a dielectric constant of $\epsilon_{ox} = 3.9\epsilon_0$, where ϵ_0 is the dielectric constant of free space. The InSb substrate was n-type with impurity concentration of $N_D = 5 \times 10^{14}\,cm^{-3}$ and a dielectric constant of $\epsilon_s = 17.78\epsilon_0$. The work function of Cr is 4.52 eV[12] and the work function of InSb reported in the literature is 4.42 eV when $N_D \sim 10^{15}\,cm^{-3}$[13]. Thus the flat-band voltage (V_{FB}) of the ideal $Cr/SiO_2/InSb$ MIS capacitor used in this study was 0.1 V. The operating temperature was 77 K.

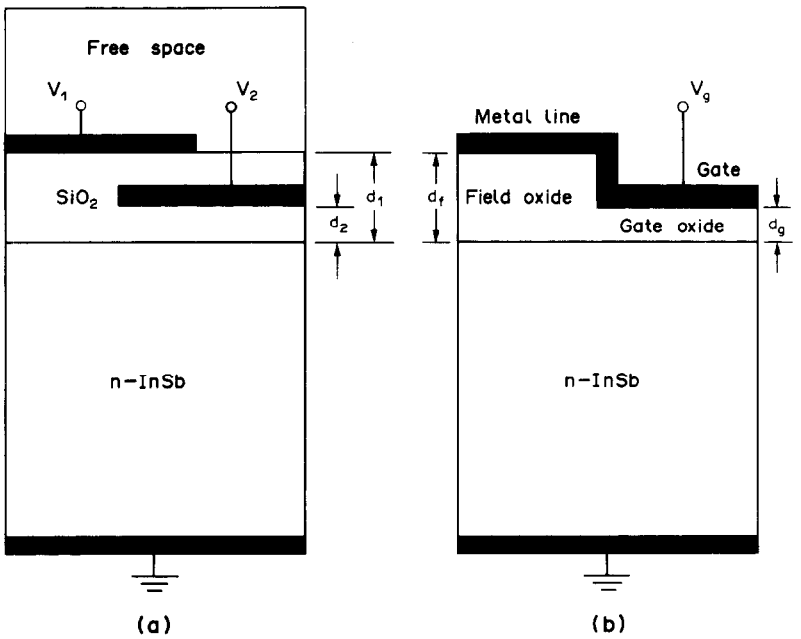

Fig. 1. (a) The schematic diagram of the dual-gate region of an InSb CID. (b) The schematic diagram of the field oxide region of an InSb CID.

The Poisson equation for the electric field distribution solving is

$$\nabla^2 V = -\frac{\rho}{\epsilon_s} \tag{1}$$

where V is the electrostatic potential, ρ is the charge density, and ϵ_s is the dielectric constant of InSb. Since breakdown takes place under the deep depletion condition, inversion carriers are not included in ρ. The charge density can be expressed as,

$$\rho(V) = q\left[N_D - N_D \exp\left(\frac{qV}{kT}\right)\right]$$

$$= qN_D\left[1 - \exp\left(\frac{qV}{kT}\right)\right] \tag{2}$$

where N_D is the impurity concentration, q is unit charge, T is the absolute temperature and k is Boltzmann's constant.

The boundary conditions are described as follows.

All of the bias voltages on the metal contacts are fixed boundary conditions. These boundaries include the row gate, column gate, field plate, conducting path and substrate contact as shown in Figs 1(a) and (b).

There are two interfaces of different materials. They are the SiO_2/InSb interface in Figs 1(a) and (b) and the SiO_2/free-space interface in Fig. 1(a). In this work, the SiO_2/InSb interface is assumed to be ideal, i.e. no trap states and interface charges. Since there are no surface charges accumulating at the interface, by Gauss' law,

$$\epsilon_s E_y^s = \epsilon_{ox} E_y^{ox} \tag{3}$$

where ϵ_s and ϵ_{ox} are the dielectric constants of InSb and SiO_2 respectively, and E_y^s and E_y^{ox} are the y-direction components of the electric field of InSb and SiO_2 at the interface, respectively. At the SiO_2/free-space interface, similar boundary conditions is derived,

$$\epsilon_{ox} E_y^{ox} = \epsilon_0 E_y^0 \tag{4}$$

where ϵ_0 is the dielectric constant of the free space, and E_y^0 is the y-direction component of the electric field of free space at the interface.

The left and right boundaries in Fig. 1, and the upper boundary in Fig. 1(a) are chosen on the region where the potential distribution is slowly varying. The boundary conditions are

$$\frac{\partial V}{\partial x} = 0 \tag{5}$$

for the left and right boundaries in Fig. 1, and

$$\frac{\partial V}{\partial y} = 0 \tag{6}$$

for the upper boundary in Fig. 1(a).

The finite-difference method is used to solve the Poisson equation with the boundary conditions. In the dual-gate structure as shown in Fig. 1(a), the upper boundary is extended into the free space, and the lower boundary is far away from the depletion region edge calculated using depletion approximation. The distance between the upper and lower boundary is about 5 μm which depends on the applied bias voltage on the gates. In the field-oxide isolation structure as shown in Fig. 1(b), the upper boundary is fixed on the conducting path, and the

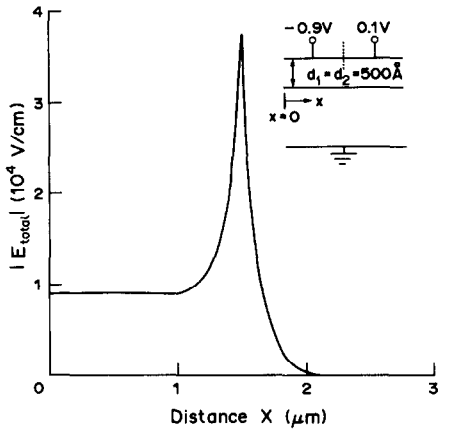

Fig. 2. The electric field distributions of the dual-gate structure with an oxide thickness of 500 Å. Bias voltages and device structure are shown in the insert of the figure. The separation of the gates is zero. The dotted line in the insert indicates the break of the gates.

vertical distance is about 3 μm which also depends on the applied bias voltage on the conducting path. The distance between the right and left boundary of both structures is chosen to be 3 μm, which is long enough to cover the transition region of the electric field distribution. For accuracy, the mesh is chosen to be uniform and square. The size is 100 × 100 Å. The solving algorithm is the Gauss–Seidel self-consistent iteration method[14].

3. RESULTS AND DISCUSSIONS

In this section, the effect of device parameters on the electric field spike taking place in the overlay region and the perimeter region of the dual-gate CID are discussed as follows.

3.1. The effect of oxide thickness

On the effect of oxide thickness, we firstly chose equal oxide thickness for both the gates, i.e. $d_1 = d_2$, and vary the thickness simultaneously. The separation of the gates is zero. In our numerical analysis, zero separation means that there are no mesh points existing between the edge mesh points of the gates. The gates bias voltages, i.e. V_1 and V_2, are −0.9 and 0.1 V, respectively. The right gate is just in its flat band bias. Figure 2 shows a surface electric field distribution with an oxide thickness of 500 Å. The vertical axis in the figure is the total electric field. It is calculated using $|E_{total}| = \sqrt{E_x^2 + E_y^2}$ where E_x and E_y are the x and y components of electric field, respectively. As can be seen, there is a significant electric-field spike existing at the interface, and the magnitude is almost four times higher than that in the left-flat region. The electric field in the right-flat region is zero because the gate bias is just in the flat-band voltage. In the left-flat region, the magnitude of the electric field is about 9×10^3 V/cm, and, in the spike peak region, it is about 3.8×10^4 V/cm. According to Anderson's formula[5, 6], when the

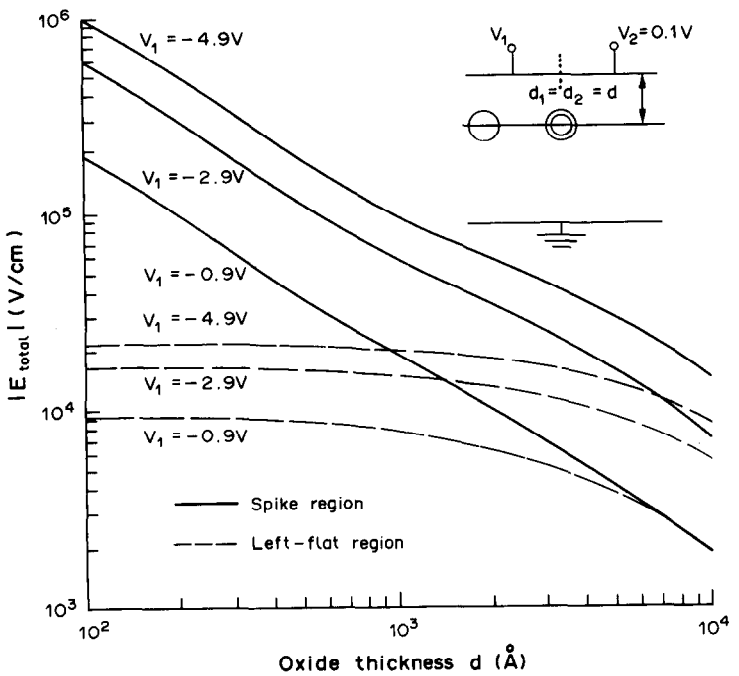

Fig. 3. The electric fields at the spike peak and the left-flat region as functions of oxide thickness under three different bias voltages, −0.9, −2.9 and −4.9 V. Bias voltage and device structure are shown in the insert of the figure. The separation of the gates is zero. The dotted line in the insert indicates the break of the gates. The dashed curves represent the electric fields of the left-flat region indicated by the single-circle in the insert. The solid curves represent the electric fields of the spike peak region indicated by the double-circle in the insert.

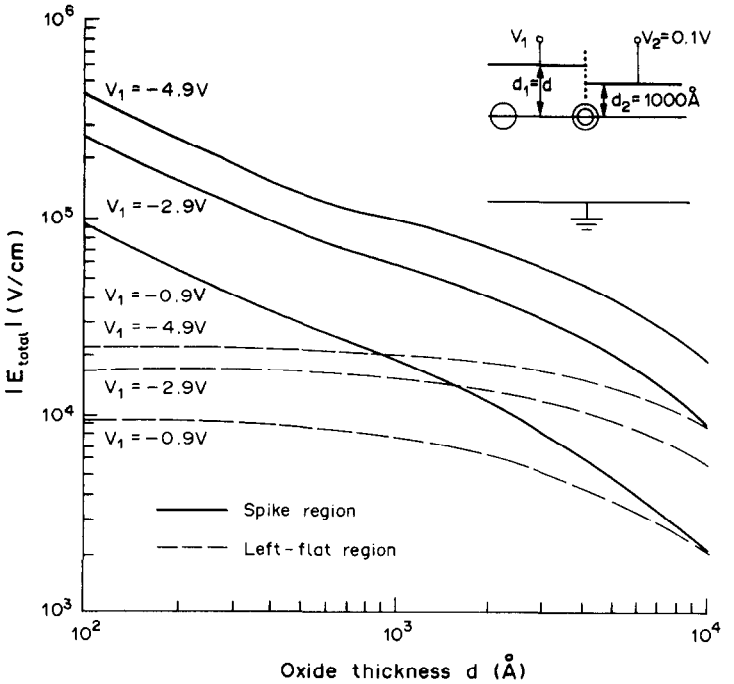

Fig. 4. The electric fields at the spike peak and the left-flat region as functions of the oxide thickness of left gate. Bias voltage and device structure are shown in the insert of the figure. The oxide thickness of the right gate is fixed at 1000 Å. The high–low gates have no overlap or separation in the horizontal direction. The dashed curves represent the electric fields of the left-flat region indicated by the single-circle in the insert. The solid curves represent the electric fields of the spike peak region indicated by the double-circle in the insert.

surface electric field is 2.2×10^4 V/cm, the magnitude of the tunneling current will be 1 μA/cm^2, which is comparable with that of the dark generation current in a dual-gate CID. Therefore, the extra spike field will further enhance the tunneling current and push the InSb CID into the surface tunneling breakdown condition.

The surface electric fields of the spike peak and the left-flat region as functions of oxide thickness under three different bias voltages, -0.9, -2.9 and -4.9 V are shown in Fig. 3. As can be seen, in the thin oxide thickness region, the electric field of the spike peak is much larger than that of the left-flat region. As the oxide thickness increases, the difference between them decreases. In the thick-oxide region, the electric fields gradually merge together. Figure 4 shows the electric fields of the spike peak and the left-flat region as functions of the oxide thickness of the left gate. The separation of the gates is zero. The oxide thickness of the right gate is fixed at 1000 Å. The trend of the difference between the electric fields of spike peak and left-flat region is the same as that in Fig. 3. In the thin-oxide thickness region, the difference is smaller than that of Fig. 3. However, the spike height is still an order of magnitude larger than the left-flat region when oxide thickness of the left gate is less than 500 Å. Although thicker oxide produces smaller spike height, it also decreases the oxide capacitance and lowers the charge-storing capability per unit bias voltage simultaneously. Therefore, an optimum thickness exists for the maximum storing capacity.

3.2. *The effect of gate bias*

The influence of bias voltage on the electric field distribution of a CID dual-gate structure was studied. The oxide thicknesses of the left and right gates were chosen to be 2000 and 1000 Å, respectively. Figure 5 shows the electric fields of the spike peak and left-flat region as functions of the bias voltage applied on the left gate, i.e. V_1. The bias voltage applied on the right gate, i.e. V_2, is fixed. Notice that the electric field in the left-flat region is independent of V_2. For each V_2, the spike height vs V_1 relation shows a concave curve, which touches the curve of the left-flat region at its lowest point. The contact point indicates the existence of the condition of no electric-field spike. The electric field distributions along the semiconductor surface are shown in Fig. 6. Under the bias condition of $V_1 = -1.9$ V, the electric field distribution is almost flat over the transition region, i.e. there is no electric field spike existing in this case. In order to further understand the reason of no electric field spike, the potential distributions of the CID cell under different bias conditions are compared. Figure 7(a) shows the 2-D potential distribution under the bias condition of $V_1 = -3.9$ V. In this case, the electric-field spike exists as shown in Fig. 6, and as can be seen in Fig. 7(a), the surface potential drops dramatically from the left side to the right side. Figure 7(b) shows the distribution under the

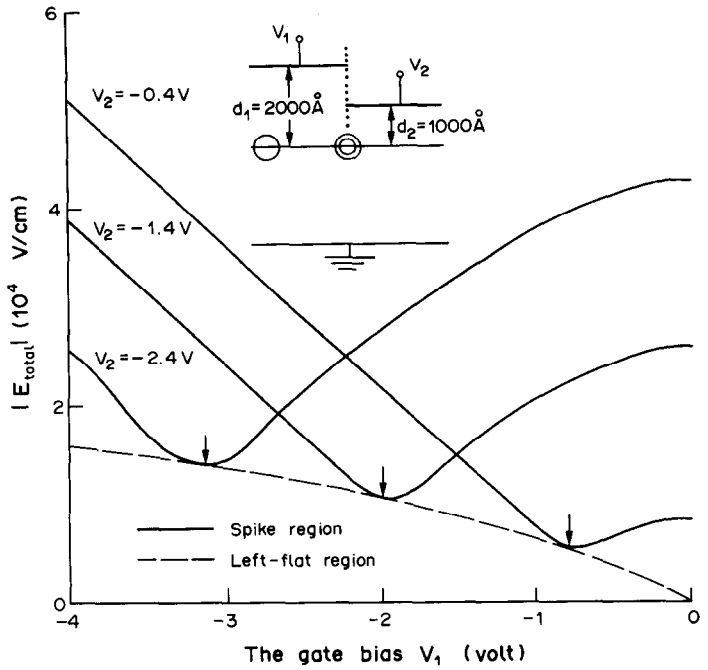

Fig. 5. The electric fields at the spike peak and left-flat region as functions of bias voltage applied on the left gate, i.e. V_1. Three bias voltages, -0.4, -1.4 and -2.4 V are chosen to apply on the right gate. Bias voltage and device structure are shown in the insert of the figure. The dashed curve represents the electric field of the left-flat region indicated by the single-circle in the insert. The solid curves represent the electric fields of the spike peak region indicated by the double-circle in the insert. The concave solid curves touch the curve of left-flat region at their lowest points which are indicated by the arrows. The electric field of the contact points is just that of the right-flat region. The high–low gates have no overlap or separation in the horizontal direction.

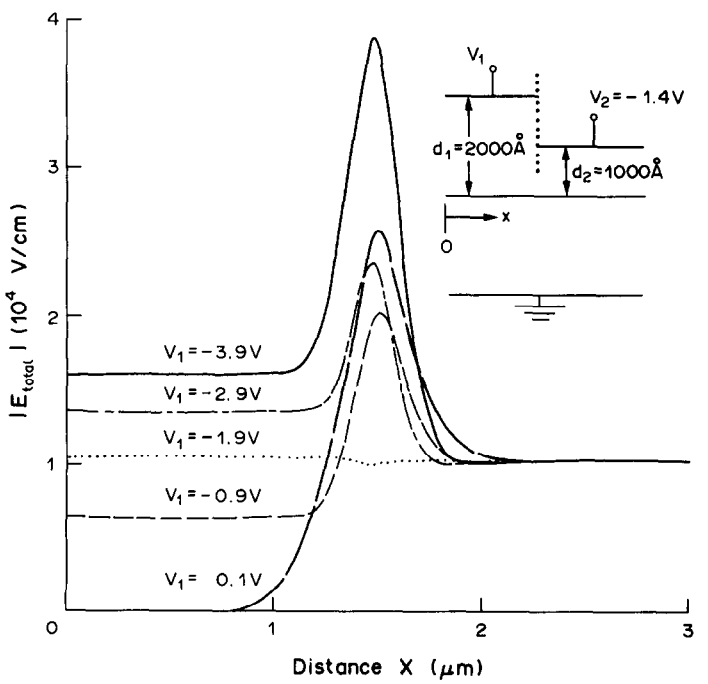

Fig. 6. The electric field distributions of the dual-gate structure under different bias conditions. The bias voltage of the right gate is fixed at -1.4 V and that of the left gate is varied from -3.9 to 0.1 V. The oxide thickness and device structure parameters are shown in the insert of the figure. The high–low gates have no overlap or separation in the horizontal direction.

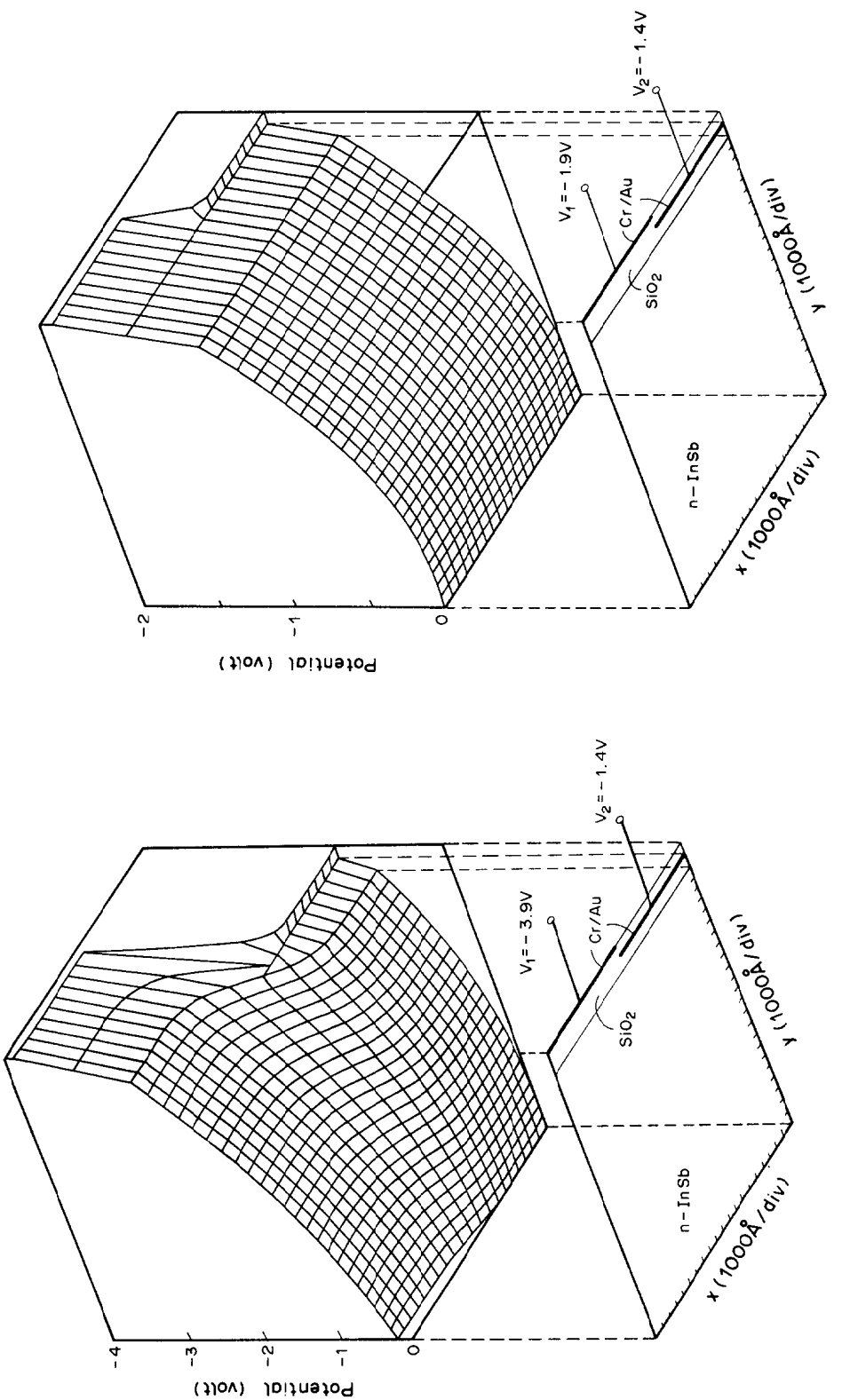

Fig. 7. The 2-D potential distributions of the dual-gate structure as function of $x - y$ position. The device structure is also plotted on $x - y$ plane. The oxide thicknesses of the left and right gates are 2000 and 1000 Å, respectively. The high–low gates have no overlap or separation in x-direction. (a) The case of electric field spike existing. The bias voltages of the left and right gates are -3.9 and -1.4 V, respectively. (b) The case of no electric field spike. The bias voltages of the left and right gates are -1.9 and -1.4 V, respectively.

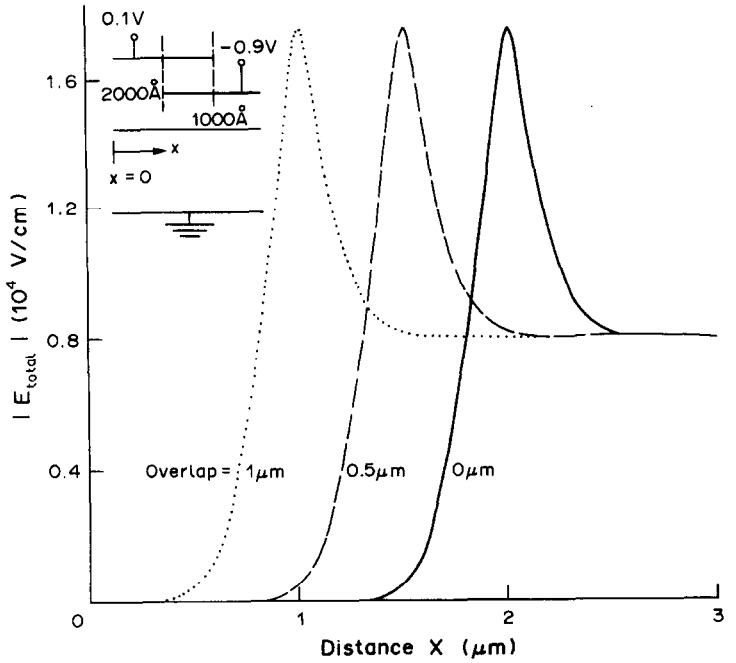

Fig. 8. The electric field distributions of the dual-gate structure with three different gate overlaps, 0, 0.5 and 1 μm. The bias voltages and oxide thicknesses of the left and right gates are shown in the insert.

bias condition of no electric field spike existing, i.e. $V_1 = -1.9$ V. As can be seen, the distribution becomes one-dimension-like, the potential becomes x-position independent. This indicates that the electric field spike is due to the unequal surface potentials along the semiconductor surface. It is suggested that putting some inversion charges under both the gates can eliminate the surface potential difference, because the region with more negative surface potential will attract inversion charges to raise its surface potential until no potential difference existing. The recently proposed charge-sharing mode and sequential row injection mode techniques[15] always keep bias charges in the potential wells of their dual-gate CID, and negligible spike is expected in their dual-gate structure. But, in their device perimeter with either field-plate or field-oxide isolation, the electric-field spike still exists there, because inversion charge can not be stored under field plate or field oxide.

3.3. The effect of the overlap and separation of the gates

In the row and column dual-gate structure, the metal contacts used have an overlap in order to ensure the charge transfer between the potential wells. How does the length of overlap influence the electric field distribution is shown in Fig. 8. Three different lengths are considered. They are 0, 0.5, and 1 μm, respectively. The oxide thicknesses and bias voltages of the left and right gates are 2000 Å and 0.1 V, and 1000 Å and -0.9 V, respectively. As can be seen, the shapes of the electric field distributions are not changed at all. They just shift horizontally to follow the movement of the lower gate. The gates are then pulled away to see the effect of separation on the electric field distribution. Again, three separation lengths 0, 0.5 and 1 μm, are considered. The oxide thicknesses are the same as those in the cases of overlap. The bias voltages of the left and right gates are -0.9 and -1.9 V, respectively. As can be seen in Fig. 9, in the case of 0.5 μm separation, the spike is smoothed out. But in the case of 1 μm, a notch appears. The notch can degrade the charge transfer between the two gates. Since the appearance of the spike and notch is also bias dependent, it is not feasible to design a separation gate structure with no spike and notch under the whole range of operating bias.

3.4. The effect of graded oxide

The spike occurring at the overlay region of the gates can be reduced by the charge-sharing effect as mentioned above. But this effect does not work in the device perimeter region. A linear-graded-oxide region[11] inserted between the gates may introduce a longer transition region for the electric field difference between the gates. In this design, the metal contact of the low gate is extended to cover the whole region. Three different graded lengths 1000, 4000 and 7000 Å, are considered. Figure 10 shows their electric field distributions. As can be seen, the spike heights are lowered, and the longer the graded length, the smaller the spike height. For detailed analysis, a plot of the electric field spike vs the graded length is shown in Fig. 11. The graded length is scanned from 0 to 1 μm and V_2 takes three values of -0.9, -2.9 and

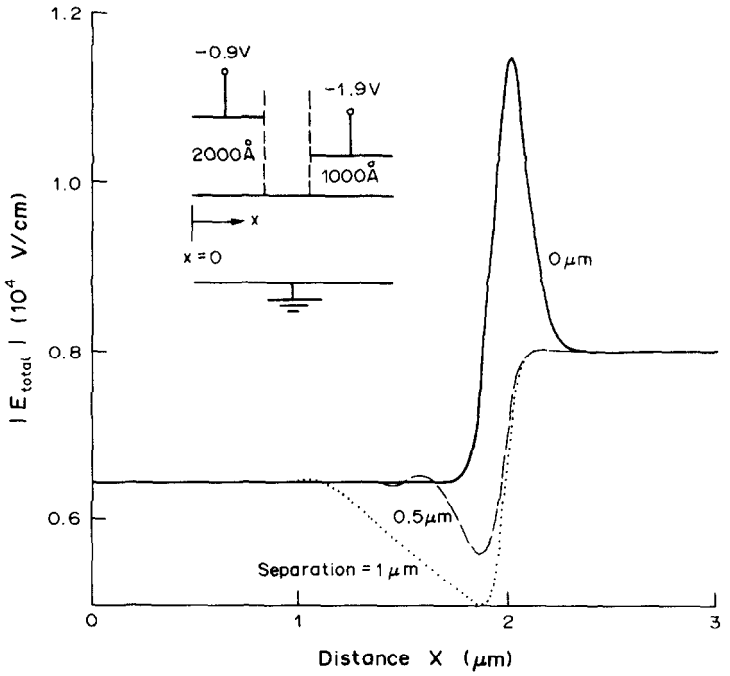

Fig. 9. The electric field distributions of the dual-gate structure with three different gate separations, 0, 0.5 and 1 μm. The bias voltages and oxide thicknesses of the left and right gates are shown in the insert.

-4.9 V. The V_1 is fixed at 0.1 V, and the oxide thickness of the left and right gates are 1200 and 600 Å, respectively. By comparing with the spike height of no grading length as shown in Fig. 11, it can be seen that more than 33% of the spike height can be reduced in the case of $V_2 = -4.9$ V when the graded length is over 1 μm. Notice that the higher the bias voltage, the larger the spike reduction. Thus the structure is more efficient when the bias is closer to the breakdown voltage.

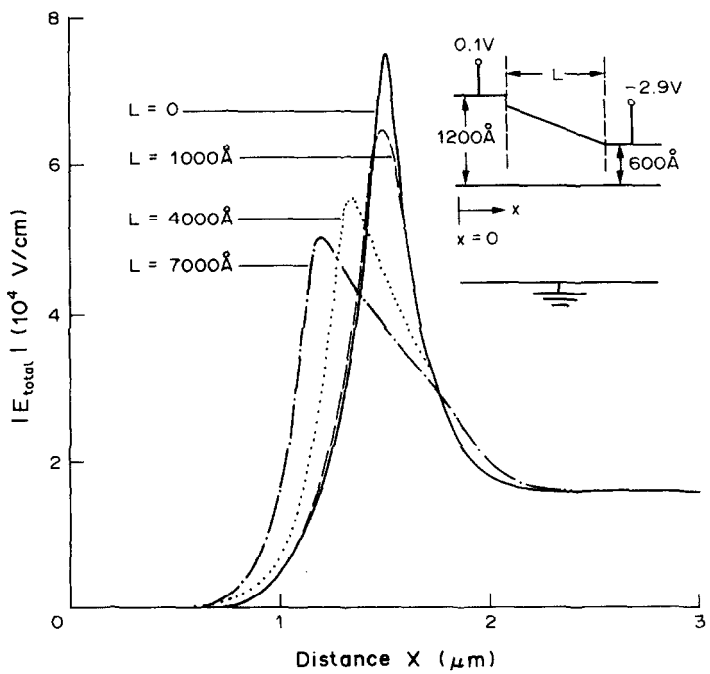

Fig. 10. The electric field distributions of the dual-gate structure with a graded oxide section inserted between the gates. The structure as well as the parameters are shown in the insert of the figure. Three graded lengths of 1000, 4000 and 7000 Å are chosen. The graded gate is connected to the right gate and there are no overlaps or separations between the left gate and it.

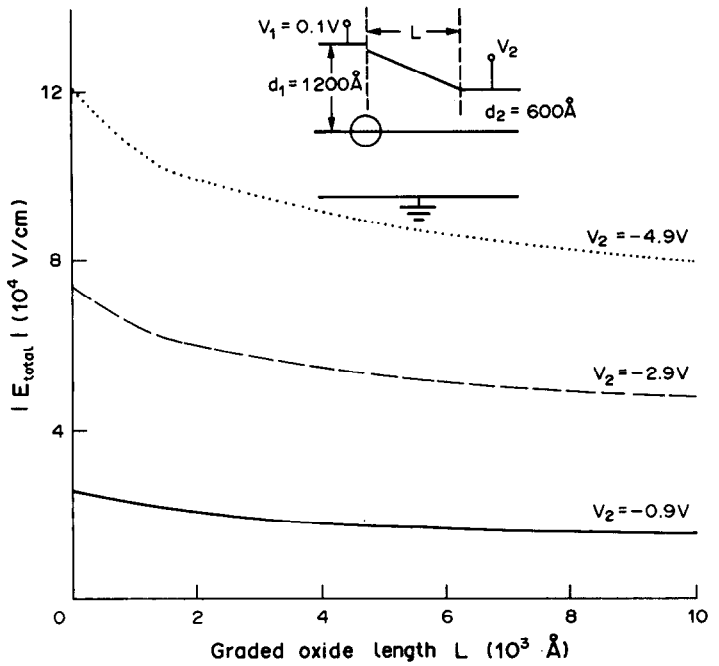

Fig. 11. The electric field spike as function of the graded oxide length. The length of the graded oxide region varies from 0 to 1 μm. The bias voltages, the oxide thicknesses as well as the structure of the linear graded oxide are shown in the insert of the figure. The graded gate is connected to the right gate, and there are no overlaps or separations between the left gate and it. The single circle in the insert indicates the spike region.

3.5. The effect of field oxide

The effect of field oxide thickness on the electric field distributions is shown in Fig. 12. The oxide thickness of the gate is 1000 Å, and the bias voltage applied on the conducting path is −0.9 V. Three field oxide thicknesses are considered firstly, they are 2000, 5000 Å, and 1 μm, respectively. As can be seen in Fig. 12, the thicker the field oxide, the higher the electric field spike height. The spike height enhancement is due to the fact that the thicker field oxide has smaller surface electric field, and the enlarged surface

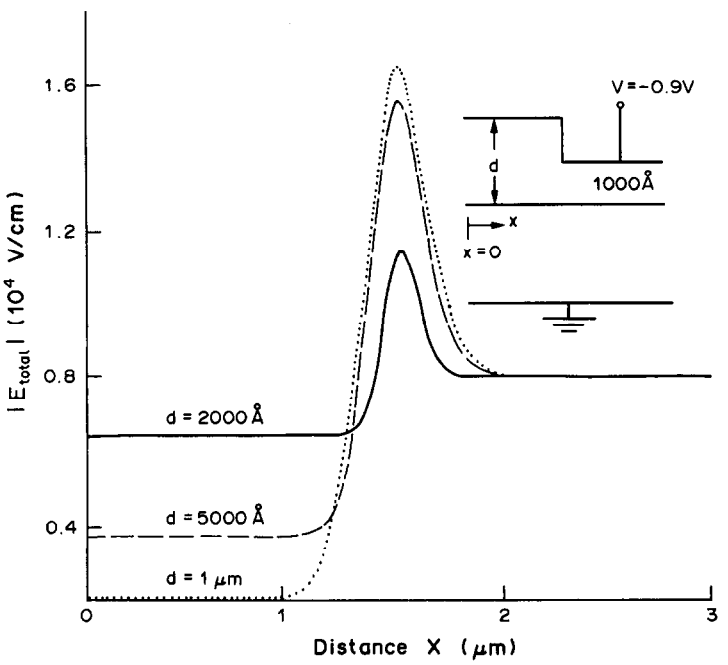

Fig. 12. The electric field distributions of the field oxide region. Three field oxide thicknesses of 2000, 5000 Å and 1 μm are analyzed. The structure as well as the parameters are shown in the insert of the figure.

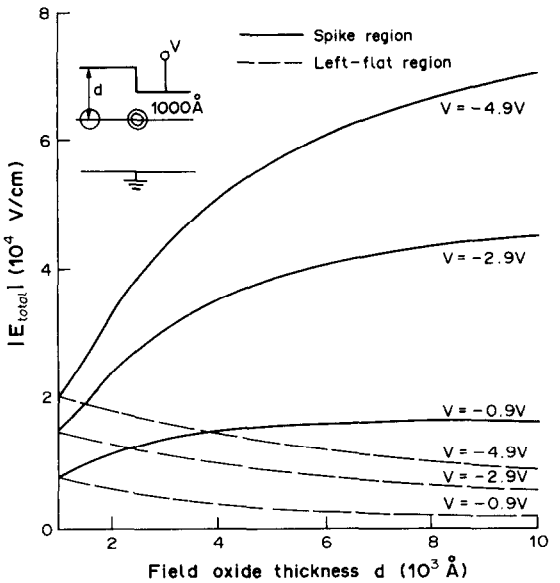

Fig. 13. The electric fields at the spike peak and the left-flat region as functions of the field oxide thickness under three bias conditions of −0.9, −2.9 and −4.9 V. The oxide thickness under the gate is fixed at 1000 Å and the field oxide thickness varies from 1000 Å to 1 μm. Bias voltage and device structure are shown in the insert of the figure. The dashed curves represent the electric fields of the left-flat region indicated by the single-circle in the insert. The solid curves represent the electric fields of the spike peak region indicated by the double-circle in the insert.

potential difference causes a higher electric-field spike. However, for the cases of 5000 and 10,000 Å thick field oxide, their electric field distributions merge together both in the transition region and gate region. This indicates that in the case of 5000 Å thick field oxide, spike height has reached its saturation value already. Figure 13 shows the electric fields at the left-flat region and the spike peak as functions of the field oxide thickness under three bias voltages of −0.9, −2.9 and −4.9 V. The oxide thickness under the gate is fixed at 1000 Å. For each bias voltage, the thicker the field oxide, the larger the difference between the fields. The difference drops to zero when the field oxide thickness is reduced to 1000 Å, the oxide thickness under the gate. Again, the higher bias voltage gives a larger spike height. In order to ensure the device isolation, the thicker the field oxide is the better; however, the thicker field oxide also causes a larger electric-field spike. Hence, there is a trade-off between them. The graded-field-oxide structure may be used to reduce the electric-field spike.

4. CONCLUSIONS

The electric-field distributions of InSb CID was studied using 2-D numerical simulation. It was found that in the dual-gate structure, the thinner the oxide, the higher the electric field spike. When the surface electric fields of both gates are equal, the electric field spike can be smoothed out. CID operated under charge sharing mode and sequential row injection mode have bias charge stored under their gates. It is expected that no spike exists at the interface of their row and column gates. However, the spike may still exist in the perimeters. The overlaps of the gates do not influence the spike height, and the separation may result in an electric-field notch which degrades the charge transfer between gates. The simulation results also show that the spike-height reduction can be as high as 33% in high-bias condition when a linear-graded oxide is inserted between the gates. In the field-oxide region, it is found that thicker field oxide produces a larger electric field spike. There is a trade-off on the thickness of the field oxide because thicker field oxide improves the isolation between CID cells.

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