we find. It can also be shown from the Gummel–Poon model that, to a comparable accuracy, the BC and BE diode characteristics could be used instead of the Gummel plots; the advantage of the Gummel plots is that the conditions in (2) can be checked.

The main inaccuracy at high-currents is from series resistances. The voltage from the RG plot has contributions from both base and collector resistance. Those contributions bend the curve $I_{b,\mathrm{RG}}$ to the right at high bias, decreasing the distance between $I_{b,\mathrm{RG}}$ and $I_{c,\mathrm{FG}}$ and so reducing the offset voltage obtained by construction. The measured offset voltage, however, does not have these contributions, and so will be larger than the value obtained graphically. On the other hand, the graphical construction does account for emitter resistance R_e, because at a given emitter current I_e both the voltage in a FG measurement as well as the measured offset voltage include a term $I_e R_e$.

One important assumption in the derivation of (6) is that the circuit elements in the Gummel–Poon model depend on only one junction voltage. When blocking of current by the discontinuities in the junctions becomes significant, this assumption breaks down [9]. For example, blocking in the BC junction will cause the FG plot to change if V_{bc} is varied, and such variation indicates that the construction here may be inaccurate.

A graphical approach allows relationships to be appreciated intuitively. For example, $\Delta V_{\mathrm{offset}}$ depends on the ratio of the emitter area A_E to the area A_C of the base-collector junction [3], and the form of this dependence can be understood from Fig. 2. If A_C is increased and everything else is kept the same, then the curve $I_{b,\mathrm{BC}}$ will shift upward, moving the point M′ to the left and increasing the distance between M′ and N′, and hence increasing $\Delta V_{\mathrm{offset}}$. Similarly, if A_E is increased, then $I_{c,\mathrm{FG}}$ will shift up, moving N′ to the left, and decreasing $\Delta V_{\mathrm{offset}}$. In the regions of Fig. 2 where current varies exponentially with voltage, $\Delta V_{\mathrm{offset}}$ will be proportional to $\log(A_C/A_E)$. (The device used in Fig. 3 has a smaller ratio of areas than that in Fig. 2, and consequently a smaller offset voltage.) Similarly, any changes in the emitter design that increase $I_{c,\mathrm{FG}}$ at a given bias, such as moving from an abrupt to a graded BE junction, will decrease $\Delta V_{\mathrm{offset}}$, whereas damage that increases the recombination in the BC junction will increase $I_{b,\mathrm{BC}}$ and consequently increase $\Delta V_{\mathrm{offset}}$.

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A PMOS Tunneling Photodetector

B.-C. Hsu, C. W. Liu, W. T. Liu, and C.-H. Lin

***Abstract*—A metal/oxide/n-Si structure with ultrathin gate oxide is utilized as a photodetector. At inversion gate bias, the dark current and photocurrent are determined by both the minority carrier (hole) generation rate in the deep depletion region and the electrons tunneling from the gate electrode to n-type Si, while only the former component is significant in the NMOS photodetector. The electron tunneling current dominates the photocurrent at sufficiently large negative gate voltage, and the sensitivity of PMOS detectors is, therefore, enhanced by approximately one order of magnitude, as compared to NMOS detectors.**

***Index Terms*—Photodetector, PMOS, tunneling diode.**

I. INTRODUCTION

Various semiconductor photodetectors and image sensors have been fabricated and studied such as charge coupled devices, photodiodes (p-i-n, Schottky, heterojunction, avalanche), and capacitive photodetectors [1]. The significant tunneling gate current of metal–oxide–silicon (MOS) diodes with ultrathin gate oxide can be applied to add new functions of MOS devices. Both NMOS [2] and PMOS [3] light-emitting diodes have been demonstrated. The NMOS photodetector have also been demonstrated as biased in the deep depletion region [4]. In this brief, we report the results of PMOS photodetector and enhanced sensitivity is observed. The fully CMOS-compatible light sources and detectors make it possible to have optoelectronic applications using a CMOS process.

II. DEVICE FABRICATION

The ultrathin gate oxide of the PMOS diode is grown by rapid thermal oxidation on 1–5 Ω-cm n-type wafer at 900∼1000 ° C. The gas flows are 500 sccm nitrogen and 500 sccm oxygen at reduced pressure. After growing ultrathin oxide, the sample is in situ annealed in nitrogen for 10 min at 900 °C. Thickness was measured by ellipsometry. The Al is used as the gate electrodes of PMOS diodes with the circular areas defined by photolithography. The device structure is shown in the inset of Fig. 1.

III. DEVICE OPERATION

Fig. 1 shows the current–voltage (I–V) curves of an Al/2.7 nm oxide/n-Si detector with an area of 3.2×10^{-4} cm^2. The photocurrent was excited by metal halide lamp with a spectrum similar to sun. Although the Al electrode blocks the light shined directly on the photodiode, the light still can be absorbed at the edge of the gate electrodes. The dark and photocurrents are relatively constant in the log scale at sufficiently large negative gate bias. For the photocurrent, the stepwise I–V curves indicate that there are two components in the photocurrents. Under the same light exposure, the current magnitude at the first plateau of the I–V curves of PMOS detectors (gate voltage $= -0.8$ V) is similar to that of a NMOS photodiode with similar substrate resistivity (Fig. 2). The photocurrent of a NMOS detector is determined by the

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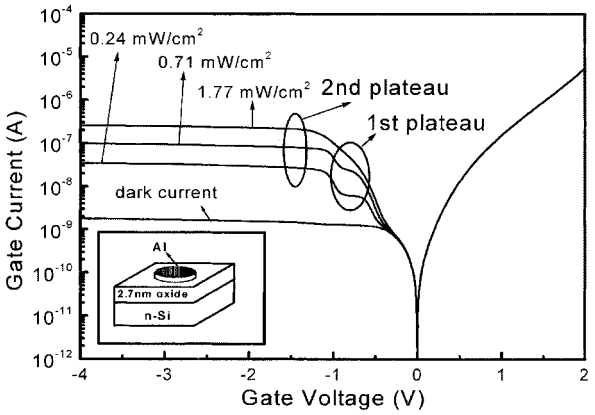

Fig. 1. Dark current and photocurrent of a PMOS tunneling photodetector. The device structure is shown in the inset.

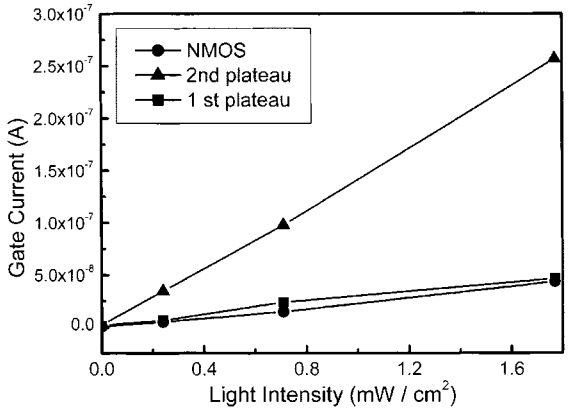

Fig. 2. Photocurrent versus light intensity at the first plateau and the second plateau of I–V curves of a PMOS photodetector as well as for NMOS photodetectors.

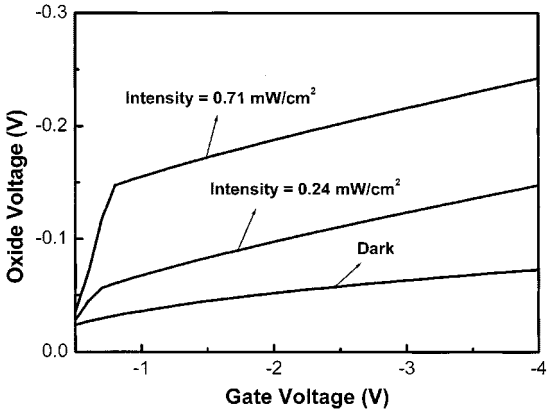

Fig. 3. Oxide voltage versus gate voltage under different light intensity.

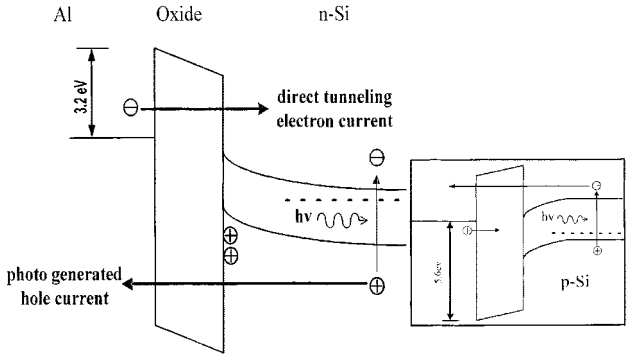

Fig. 4. Schematic diagram of photocurrent mechanisms for a PMOS photodetector. The photocurrent consists of photo-generated hole current and direct tunneling electron current. The transport mechanisms of a NMOS photodetector is shown in the inset.

minority (electron) generation rate in the deep depletion region, since the tunneling rate through the ultrathin oxide is sufficiently large at large gate bias [4]. Therefore, the first plateau of I–V curves of PMOS detector should originate from the minority (hole) generation rate in the deep depletion region. Both NMOS and PMOS photodetectors have the same magnitude of photocurrent at the first plateau under the same intensity of light exposure, since the electron generation rate in NMOS and the hole generation rate in PMOS are the same at the same light intensity. The hole concentration at Si/oxide interface of a PMOS detector is balanced by the photo-generation rate and the tunneling rate through the oxide. As negative gate bias continues to increase, the hole concentration at oxide/Si interface increases slowly, and oxide voltage also increases very slightly (soft pinning) [4]. The calculated oxide voltage versus the applied gate voltage under different light exposure is given in Fig. 3. The calculation model can be found in [4], and the parameter used for holes are $A = 1 \times 10^{-5}\ \mathrm{s}^{-1}$, $C = 6.325 \times 10^{6}\ \mathrm{V}^{-0.5}\ \mathrm{cm}^{-1}$, $t_{ox} = 2.7$ nm, $\phi_O = 4.5$ eV, and $N_A = 5 \times 10^{15}\ \mathrm{cm}^{-3}$. The oxide voltage increases with light exposure intensity, but still constitutes small fraction of the gate voltage. Since the oxide voltage increases slightly with gate voltage (Fig. 3), most gate voltage drops on Si, the avalanche condition of the detector is very similar to Si Schottky diode. No breakdown was observed for the negative gate voltage less than 10 V.

The oxide voltage causes the direct tunneling of electrons from the Al gate to n-type Si in PMOS detectors. This direct tunneling electron current forms the second plateau in the I–V curves in a PMOS detector, which is approximately one order magnitude larger than the photo-generated hole current at the first plateau (Fig. 2). Most gate voltage drops on Si and a deep depletion region is formed. The soft pinning of oxide voltage at large negative gate bias restricts the further increase of the direct tunneling electron current, which is strongly dependent on oxide voltage, and the photocurrent is relatively constant after some gate bias. Fig. 4 illustrates these two mechanisms. Note that the direct electron tunneling current in the PMOS detector has a barriers height of $\sim$3.2 eV, while the direct hole tunneling current in the NMOS detector has a barrier height of $\sim$5.6 eV (Fig. 4). The NMOS photodetector with Al gate has a barrier height of $\sim$5.6 eV for holes tunneling from Al to p-Si substrate, which is much larger than electron barrier height ($\sim$3.2 eV) in PMOS. This leads to a negligible direct tunneling hole current in a NMOS detector. The second plateau, therefore, is not observed in the I–V curve of NMOS detectors [4].

In Fig. 1, we can see that when light intensity increases to 1.77 mW/cm^2, the first plateau is not clearly observed, as comparing to the other two curves. It is because the first plateau is due to the hole generation in the deep depletion region, which is determined linearly by the light intensity, and the second plateau is due to the electrons tunneling from gate electrode to n-Si, which is determined exponentially by the oxide voltage. The small oxide voltage is approximately proportional to light intensity. Therefore, it is expected that the second plateau dominates the I–V curves under sufficient light exposures, and only one plateau can be observed in I–V curves although the photo-generated hole current still exists.

By comparing photocurrents in NMOS detectors with Al and transparent ITO (indium tin oxide) electrodes, the edge absorption of light around the nontransparent Al electrode is approximately 5% of the absorption of the ITO gate. The measured external quantum efficiency of

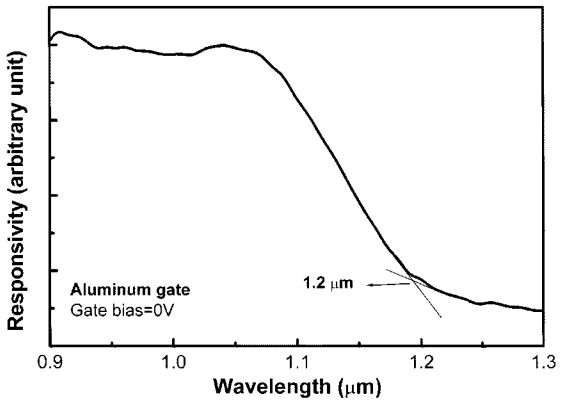

Fig. 5. Measured responsivity of the PMOS photodetector.

Al gate PMOS is 4% if the first plateau current is used as the photo signal, which is similar to the efficiency of Al gate NMOS. However, the efficiency of the PMOS detector can be as high as 40% if the second plateau is used as the photo signal. For current devices, no efficiency-enhanced structures such as grid gate electrodes (semi-transparent), transparent gate electrodes, and anti-reflection coating are used, but the optimization is under progress. The measured responsivity in the infrared region of the PMOS detector is given in Fig. 5. This PMOS photodetector has a cutoff wavelength at 1.2 μm.

IV. Conclusion

A photodetector using the PMOS tunneling structures is demonstrated. The direct tunneling electron current from Al electrode to n-type silicon is the main component of the photocurrent, which is one order of magnitude larger than minority generation current in the deep depletion region. The two plateaus in the I–V curves of the photocurrent are the signatures of these two mechanisms. The direct tunneling hole current in the NMOS is very small, and only the minority (electron) generation current forms the photocurrent. As a result, the sensitivity of a PMOS detector is much larger than that of a NMOS detector.

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