Novel Methods to Incorporate Deuterium in the MOS Structures

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***Abstract*—The deuterium concentration as high as 2×10^{20} cm^{-3} can be incorporated in rapid thermal oxide layers by a process of deuterium prebake and deuterium post oxidation anneal. The deuterium distributed not only at Si/oxide interface but also in the bulk oxide. The deuterium incorporation shows the improvement on soft breakdown characteristics and the interface state density at SiO_2/Si after stress. The addition of very high vacuum prebake process yields a deuterium concentration of 9×10^{20} cm^{-3}, but also leads to the formation of rough oxide.**

***Index Terms*—Deuterium incorporation, interface states, MOS, very high vacuum prebake.**

I. Introduction

THE ELECTRICAL degradation of metal–oxide–silicon (MOS) devices due to electrical stress has been extensively studied since the early 1980s [1]. Some degradation is related to the hydrogen release from the Si/oxide interface by hot electrons [2] and the incorporation of deuterium at the Si/oxide interface can significantly improve the device reliability [3]. The strong coupling between Si–D bond bending mode (460 cm^{-1}) and transverse optical phonons in bulk Si (463 cm^{-1}) is responsible for this giant isotope effect [4]–[6]. Recently, we have demonstrated that the deuterium incorporation can improve the soft breakdown in the NMOS tunneling diodes [7] and the reliability of MOS tunneling light emitting diodes [8]. The conventional method to incorporate the deuterium is performed by post metallization anneal after gate electrode deposition. In this letter, we report three kinds of deuterium process performed before the gate electrode deposition, and compare the deuterium concentrations with each process. The improvement of electrical properties is also demonstrated.

II. Growth and Fabrication

The 4-in p-type wafer was transferred to the process chamber through the load-lock chamber and the ultrathin gate oxide of the NMOS diode was grown by rapid thermal oxidation (RTO) at 800–1000 °C. The gas flows were 500 sccm nitrogen and 500 sccm oxygen at reduced pressure. The wafer temperature was monitor by pyrometry with a close loop control. The gate oxide thickness was measured by ellipsometry. NMOS diodes had Al gate electrodes with circular areas defined by photolithography.

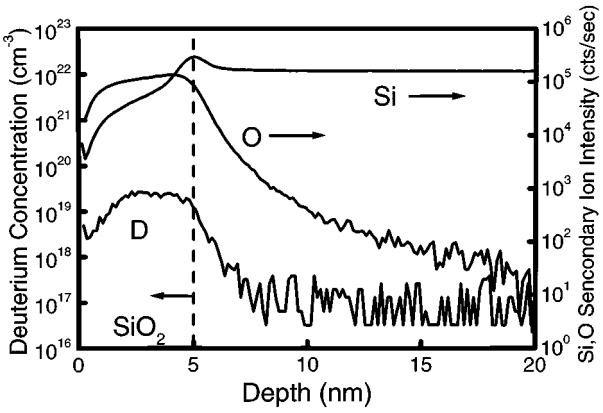

Fig. 1. SIMS profiles of the rapid thermal oxide with deuterium prebake.

III. Deuterium Incorporation

In order to incorporate deuterium in the ultrathin oxide, the first kind process is to prebake the wafers *in-situ* at 1000 °C for two min in deuterium gas. Then the gate oxide is grown, followed by a 900 °C nitrogen post oxidation anneal for 10 min. The secondary ion mass spectroscopy (SIMS) profiles of this deuterium prebake process shows a deuterium concentration of 2×10^{19} cm^{-3} in the oxide as shown in Fig. 1.

To further increase the deuterium incorporation, the second kind process is to add a deuterium post oxidation anneal for 10 min at 900 °C before the nitrogen anneal in the previous process. This yields a deuterium concentration of 2×10^{20} cm^{-3} in Fig. 2. The deuterium concentration increases by one order of magnitude, as compared to the first kind process.

Since the Si wafers are cleaned by a HF dip before the transfer to the process chamber, the Si surface is hydrogen-terminated and the hydrogen passivation will prevent the deuterium incorporation in the oxide [9]. Therefore, the third kind process performs a thermal bake of the hydrogen-passivated wafer in the very high vacuum environment before the deuterium prebake. During the very high vacuum prebake ($<3 \times 10^{-6}$ torr, maintained by a turbo pump), hydrogen can be removed from the Si surface. To estimate the hydrogen coverage after the very high vacuum prebake, the desorption rate R_d was calculated by first order analysis [10] with the assumption of the initial coverage $\theta = 1$, i.e., every silicon atom on the surface is bonded with hydrogen.

$$R_d = -\frac{d\theta}{dt} = k_d \cdot \theta = \theta \cdot k_d^0 \exp(-E_d/kT)$$

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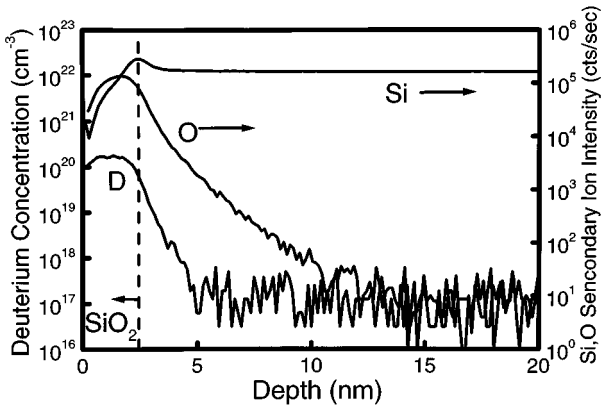

Fig. 2. SIMS profiles of the rapid thermal oxide with deuterium prebake and the post oxidation deuterium annealing.

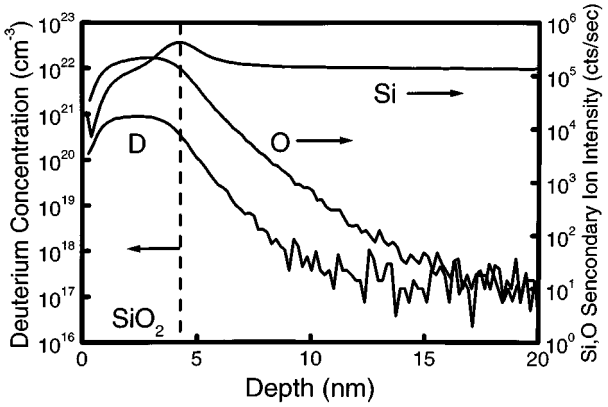

Fig. 3. SIMS profiles of the rapid thermal oxide with very high vacuum prebake, deuterium prebake, and the post oxidation deuterium annealing.

where the activation energy E_d and preexponential factor k_d° of hydrogen are 2.17 eV and 2.2 $\times$ 10^{12} s^{-1}, respectively [10]. The hydrogen is almost completely removed by the very high vacuum prebake for two min at 1000 °C, as indicated by the calculation. The deuterium incorporation in the oxide with very high vacuum prebake can reach as high as 9×10^{20} cm^{-3} from the SIMS data in Fig. 3. However, the very high vacuum prebake also yields rough oxide with roughness up to 1.5 nm [11]. Since the roughness can also enhance the oxide reliability [12], the sole isotope effect on the oxide reliability can not be resolved. Therefore, all the following electrical measurements are based on the oxide prepared by the second kind process.

The grown oxide thickness by the deuterium process is 10–20% smaller, as compared to the hydrogen process. The hydrogen desorption rate is approximately 1.6 times the deuterium desorption rate [10], and this may be responsible for the low growth thickness of deuterium process. For all three processes, the deuterium atoms not only distribute at Si/oxide interface but also in the entire SiO_2 layers (Figs. 1–3), very similar to the deuterium distribution of D_2O pyrogenic oxide [13]. The incorporation of deuterium both at interface and bulk oxide plays an important role to suppress the electron trap creation. Note that the D_2O pyrogenic oxidation [13] yields a much lower deuterium concentration of 1×10^{19} cm^{-3}, as compared to our process. Besides, to avoid the other

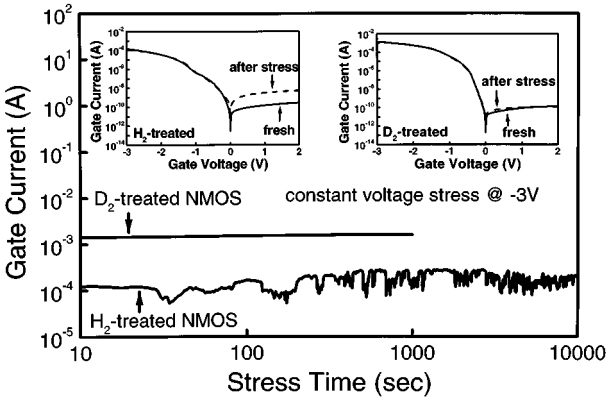

Fig. 4. Gate current versus stress time plot of H_2-treated and D_2-treated NMOS diodes with the area of 3×10^{-4} cm^2 under constant voltage stress with -3 V CVS for 10 000 and 1000 sec, respectively. The insets are the I–V characteristics of the devices before and after stress.

signal with mass-to-charge ratio of 2 such as H_2^+, the SIMS profile of a H_2-treated sample was also measured, and this signal was $\sim 1 \times 10^{18}$ cm^{-3}, which was negligible as compared to the deuterium concentration. The H_2-treated samples were processed using the same procedure except replacing deuterium with hydrogen.

IV. Electrical Characterization

In order to observe the isotope effect, we use the second kind process to fabricate H_2-treated and D_2-treated devices to avoid the roughness effect produced by the very high vacuum prebake [11]. Fig. 4 shows the gate current variation as a function of stress time for H_2-treated and D_2-treated NMOS diodes with the area of 3×10^{-4} cm^2 under constant voltage stress (CVS). There is no apparent fluctuation in gate current during the stress of the D_2-treated devices ($T_{ox} = 1.6$ nm), and the I–V curves of the devices after 1000 sec CVS at -3 V is almost identical to the fresh one, as shown in the right inset of Fig. 4. For H_2-treated devices ($T_{ox} = 1.8$ nm), the fluctuation in gate current under CVS implies that the degradation of oxide occurs and the inversion tunneling current increases significantly after the 10 000 sec CVS at -3 V (the left inset of Fig. 4). Note that the injection fluence (Q_{inj}) maintains the same (about 4×10^3 coul/cm^2) for both the H_2-treated and D_2-treated devices, and the D_2-treated devices have higher current densities. The D_2-treated device still remains intact even after 5000 sec stress (not shown here). We also perform the high–low frequency capacitance–voltage *(C-V)* measurement on MOS diodes with thick oxide ($T_{ox} = 4$ nm) with the area of 3×10^{-4} cm^2 to extract the interface state densities (D_{it}) of the fresh devices and the stressed devices (Fig. 5). Note that we have difficulties to obtain reliable C–V measurements on thin oxide (<3 nm). The extracted D_{it} increases by $\sim 7\times$ in H_2-treated devices after 15 sec constant voltage stress at -6 V since the Si–H bonds were broken by the injected electrons. No apparent increase of D_{it} for D_2-treated devices implies the isotope effect. Both devices with 4-nm oxide break down during the constant current stress at -1.5 μA (the insets of Fig. 5). It is similar to the previous report that there is an isotope effect on D_{it}, but no isotope effect on stress induced leakage current (SILC) for ultrathin oxide [14]. Note that the

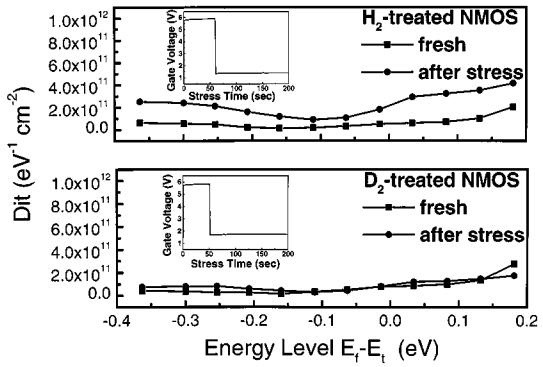

Fig. 5. Interface states density versus energy level of H_2-devices (upper) and D_2-devices (lower) with the area of 3×10^{-4} cm^2 before and after stress. D_{it} increases approximately 7× after stress in H_2 devices. No apparent increase of D_{it} in D_2-treated devices is observed. The insets are the gate voltage variation during constant current stress -1.5 μA.

isotope effect on SILC has been observed on the deuterium pyrogenic oxide, but not on the deuterium annealed thermal oxide [15].

Note that we have investigated the HF-dip only sample without H_2 treatment as a control sample. The value of D_{it} is 2×10^{12} eV^{-1}cm^{-2} for the control sample, and reduces to 4×10^{11} eV^{-1}cm^{-2} with H_2 prebake two min at 1000 °C. The D_{it} can further decrease to be less than 1×10^{11} eV^{-1}cm^{-2} with both H_2 prebake and H_2 postoxidation anneal (H_2 POA for 10 min) at 900 °C. However, the previous study reported that the degradation of the electrical properties was observed after the H_2 POA at temperature of 400–800 °C [16]. This may attribute to different POA temperature, N_2 POA, and oxidation conditions.

V. Conclusions

The deuterium distribution is not only at interface but also in the bulk oxide by these novel methods. The deuterium concentration as high as 2×10^{20}cm^{-3} can be achieved by a process of deuterium prebake and deuterium post oxidation anneal. The isotope effects on constant voltage stress and D_{it} are observed for the deuterium-treated MOS device.

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