Electron Mobility Enhancement Using Ultrathin Pure Ge on Si Substrate

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***Abstract*—We demonstrate enhancement of electron mobility in nMOSFET using an ultrathin pure Ge crystal channel layer directly grown on a bulk Si wafer. A thin Si crystal layer is also grown on top of a Ge crystal channel layer as a capping layer. Using the Si/Ge/Si structure, a maximum 2.2X enhancement in electron mobility is achieved while good gate dielectric properties and junction qualities of bulk Si devices are maintained.**

***Index Terms*—Effective electron mobility, Ge, high-K gate dielectric.**

I. Introduction

Replacement of SiO_2 with high-K gate dielectrics has highlighted new challenges such as channel mobility degradation [1], [2]. Recently, MOSFET on Ge substrate is extensively investigated as it can offer two times and four times higher electron and hole mobilities, respectively [3]. However, integration of bulk Ge into CMOS processes has encountered several critical problems, such as poor mechanical properties and limited supply of raw material. Unlike Si, the low thermal stability of Ge and water-solubility of GeO has hindered the realization of good interfacial quality with gate dielectric [4], [5]. In addition, smaller bandgap of Ge has resulted in high source/drain junction leakage current [4], [6]. In this letter, we propose and demonstrate a simple device structure to exploit the advantage of high carrier mobility of Ge channel, while utilizing other excellent properties of Si substrate, such as good mechanical properties, excellent integrity with gate dielectric and good on-off ratio of junction current.

II. Device Structure

Due to 4% lattice constant mismatch and surface energy difference between Ge and Si, formation of islands and three-dimensional clusters have been observed if Ge is grown directly on Si [7]. Nevertheless, growth of continuous and defect free crystal Ge layer on Si crystal is indeed still possible if the Ge layer grown is thinner than critical thickness, a thickness in which dislocations or islands starts to form when strain is relaxed. It is reported that the critical thickness of Ge on Si is below 10 nm, depending on the process conditions [8], [9]. Quantum mechanical behavior of the inversion electrons has shown that the electron concentration peaks at a distance of 1 to 2 nm from the gate dielectric/Si interface, with the whole inversion layer depth extends to several nm into the substrate, depending on the surface electric field. For the exploitation of advantage of high channel mobility, therefore, it is not necessary for high mobility channel to be thick. Considering such, we propose to use an ultrathin crystal Ge layer directly on Si substrate, with its thickness thinner than critical thickness. On top of this Ge layer, we grow an additional ultrathin Si epi layer. MOSFETs are then fabricated on this Si/Ge/Si (SGS) substrate, as shown in Fig. 1(a). In such transistor, carrier transport can occur in the Ge layer while majority part of source/drain junction is still in Si substrate. The electron population distribution will mainly reside in the Ge layer when the Si capping layer is very thin (<1 nm). Gate dielectric is formed on top of silicon surface. Therefore, we can achieve high channel mobility of Ge devices while maintaining other properties of Si devices.

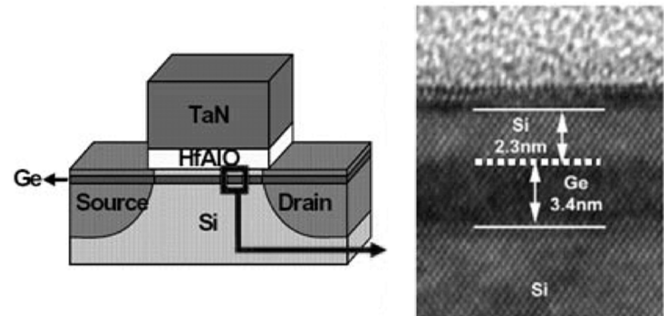

Fig. 1. (a) Schematic diagram of Si/Ge/Si (SGS) MOSFET. Majority part of the S/D is in the Si substrate and a thin Ge layer lies at the channel region. (b) XTEM image of 3.4 nm of Ge epitaxially grown on Si substrate, with a thin Si capping layer of 2.3 nm.

III. Device Fabrication

A Si buffer layer of 44 nm was epitaxially grown at 525 °C on a p-type Si (100) substrate (15–25 Ω cm) by UHV/CVD method, using SiH_4 as precursor. A pseudomorphic Ge layer was then epitaxially grown with GeH_4 precursor, followed by growth of a thin Si capping layer. Fig. 1(b) shows the cross-sectional transmission electron microscope (TEM) image of as-deposited Si/Ge/Si (SGS) layers, with thickness of Ge and Si capping layer of 3.4 and 2.3 nm, respectively. From the cross-sectional TEM

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image, no dislocations and defects are observed at the Ge/Si interfaces. The root mean square of surface roughness is 0.516 nm as measured by atomic force microscopy, indicating no sign of Ge island formation on top of Si substrate. For the MOSFET fabrication, Si capping layer thickness was further reduced just before gate dielectric deposition by repeating wet chemical oxidation and stripping process using SC1 (NH_4OH:H_2O_2: DIW) and diluted HF at room temperature. Three different final Si capping layer thicknesses of 2.3 nm, 1.5 nm, and 0.7 nm were prepared. HfAlO was deposited as gate dielectric at 450 °C, followed by a post deposition annealing at 500 °C for 60 s in a N_2 ambient. TaN was used as gate electrode. For source/drain (S/D) formation, a method of amorphization and solid-phase epitaxy (SPE) re-growth at a low temperature was employed. Arsenic ions were implanted with a dose of 3×10^{15} cm^{-2} at 32 keV and then annealed using furnace at 550 °C for 10 min in a N_2 ambient for SPE regrowth. Finally, Al metallization process for contact and forming gas annealing were implemented.

IV. Results and Discussion

Fig. 2 shows the capacitance–voltage (*C–V*) characteristic of SGS nMOSFET with Si capping layer thickness of 2.3 nm. Unlike the *C–V* curve of Ge MOS capacitors [5], no apparent $D_{\rm it}$ generated is observed in SGS MOS capacitors. A small plateau was observed during weak accumulation ($V_g = \sim 0$ V), attributed to holes confinement in the Si/Ge/Si heterostructure, as depicted in the inset of Fig. 2. The holes confinement in this potential well effectively increases the equivalent oxide thickness (EOT) during weak accumulation. Accumulated holes only occur at the Si capping/HfAlO interface during strong accumulation ($V_g < -1$ V). When the Si capping thickness is thinner, this effect becomes less prominent. Whereas during inversion ($V_g > 1$), electron will populate the HfAlO/Si capping interface.

Fig. 3(a) shows the leakage current density (J_g) *versus* EOT, both for SGS and bulk Si nMOSFETs. The SGS nMOSFET has shown comparable leakage current to those of other high-K on bulk Si devices obtained by other research groups [10], [11]. Fig. 3(b) shows the n^+ S/D junction properties of the SGS nMOSFET as compared to junction properties of bulk Si nMOSFET and bulk Ge nMOSFET [4]. Bulk Si nMOSFET implanted with arsenic with a dose of 1×10^{15} cm^{-2} at 100 keV and activated by rapid thermal anneal (RTA) at 900 °C for 30 sec is included for comparison. As majority of the S/D area is in the Si substrate, the reversed leakage current for the SGS MOSFET is about three orders of magnitude lower than reported data for n^+ S/D of Ge substrate at reversed bias of -1 V [4]. However, the reversed leakage current of SGS nMOSFET is more than one order of magnitude higher at -1 V, compared to bulk Si nMOSFET with high temperature RTA, which requires further optimization of S/D activation process for SGS devices.

Fig. 4(a)–(c) shows the I_d–V_d characteristics of SGS nMOSFET for different Si capping thickness, compared with Si nMOSFET. The SGS nMOSFET shows distinct enhancement of 19.4%, 35.7%, and 47.5% compared to bulk Si nMOSFET, for the Si capping layer thickness of 2.3 to 1.5 and 0.7 nm, respectively. The electron mobility in SGS nMOSFET, indicated in Fig. 4(d), measured using split *C–V* method, also shows significant enhancement of 1.4, 1.8, and 2.2 times in peak mobility for the different Si capping layer thicknesses, respectively. The mobility enhancement depends both on the electron population distribution across the SGS structure during inversion and its straining behavior. When the electrons reside mainly in the Ge layer, as for the case of 0.7 nm of Si capping layer SGS nMOSFET, the channel mobility

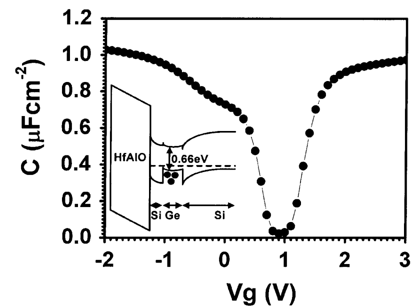

Fig. 2. *C–V* characteristics of TaN/HfAlO for SGS MOSFET with Si capping layer thickness of 2.3 nm. Inset shows the band diagram for SGS substrate, with Si capping layer of 2.3 nm, indicating confined holes in the Ge valence well, resulting in thicker EOT during weak accumulation.

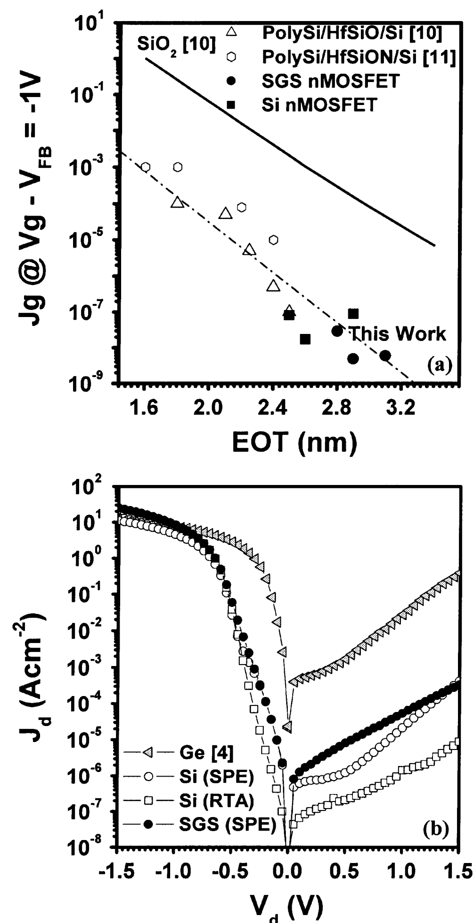

Fig. 3. (a) Gate dielectric leakage current (J_g at V_g–$V_{\rm FB} = -1$ V) *versus* EOT, showing HfAlO on SGS nMOSFET has comparable leakage current with that on bulk Si MOSFET in this letter and other reported high-K on bulk Si [10], [11]. (b) S/D junction properties of SGS, bulk Si, and bulk Ge MOSFET [4].

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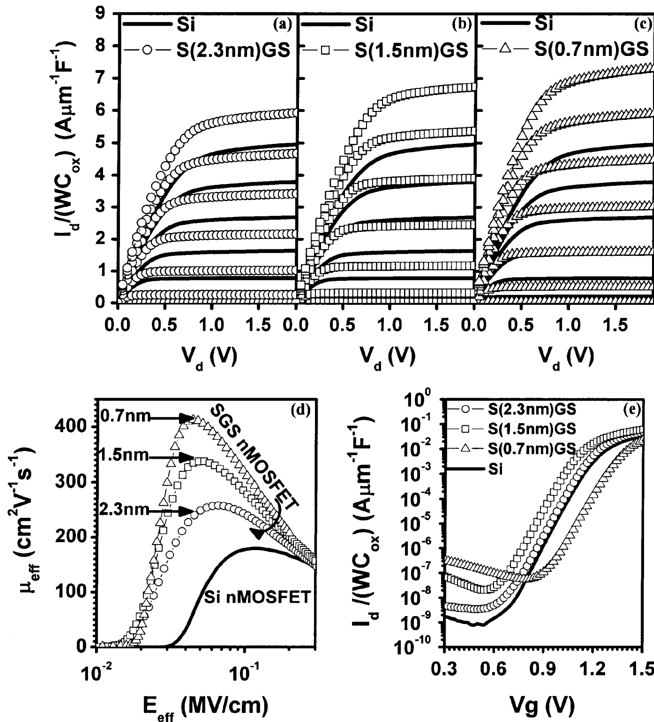

Fig. 4. I_d–V_d characteristics for SGS MOSFET with Si capping layer thickness of (a) 2.3, (b) 1.5, and (c) 0.7 nm. W/L of the MOSFET $= 320/8\ \mu$m. Each curve is for V_g–V_T of -0.2 to 1.2 V, in increments of 0.2 V. (d) The effective mobility *versus* vertical effective field for SGS and bulk Si MOSFET with HfAlO gate dielectric. (e) I_d–V_g characteristics for SGS nMOSFET, as compared with Si nMOSFET.

is greatly enhanced, compared to bulk Si nMOSFET. It is well known that the electron mobility in bulk Ge is two times of that of bulk Si. In this letter, 2.2 times enhancement in electron mobility is demonstrated. The additional enhancement may be attributed to strain in the channel layer, which will be further explored later.

Fig. 4(e) compares the I_d–V_g characteristics of SGS and Si nMOSFETs. The subthreshold swing for SGS nMOSFET with Si capping thickness of 2.3 and 1.5 nm is approximately 95 mVdec^{-1}. This is relatively comparable to that of Si nMOSFET fabricated simultaneously, indicating no interface states density degradation. However, the subthreshold swing is slightly degraded to 110 mVdec^{-1} when Si capping layer is 0.7 nm, probably due to diffusion of Ge through the ultrathin Si to the dielectric/Si interface.

V. Conclusion

In this letter, we have demonstrated SGS nMOSFET with high-K gate dielectric, showing a maximum mobility enhancement of 2.2 times than bulk Si nMOSFET. Although further optimizations on thickness combination and thermal processes need to be done, the SGS MOSFET shows a good feasibility as a new way for carrier mobility enhancement, with minimal modification to current CMOS process flow.

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