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Hole confinement at Si/SiGe heterojunction of strained-Si N and PMOS devices

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Abstract

Due to the Fermi level pinning effect on the hole confinement at the valence band offset, the capacitance–voltage (*C–V*) characteristics of NMOS capacitor exhibit more obvious plateau than that of PMOS capacitor, demonstrated by both experimental and simulated results. Using device simulation, the ratio of hole density at the oxide/strained-Si interface to that at the strained-Si/relaxed SiGe interface for both N and PMOSFETs is investigated. The much higher hole density ratio in PMOSFETs than that in NMOSFETs also reveals the Fermi level pinning effect.
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Keywords: MOS *C–V*; Strain; Device simulation; Hole confinement; Pinning effect

1. Introduction

Sustaining the expected performance enhancement in each generation through geometric scaling has become an increasingly difficult problem [1]. One way to rise to the challenge of improving device performance is to enhance carrier transport in the MOSFET channel by changing the material properties. Many experiments and theoretical calculations [2–12] have revealed that the electron and hole mobilities in tensile-strained-Si layers grown on relaxed $Si_{1-x}Ge_x$ are significantly enhanced recently. Thus, strained-Si MOSFETs are regarded to have one of the promising high-performance device structures in sub-100-nm complementary metal oxide semiconductor (CMOS) technology. The *C–V* characteristics of strained-Si NMOS and PMOS capacitors exhibit a plateau at the accumulation and inversion regions, respectively, due to the band offset [11] at the strained-Si/SiGe heterojunction. Nevertheless, its applications are not yet clearly understood. This letter investigates the differences of *C–V* characteristics, band diagram, and hole density ratio between NMOS and PMOS strained-Si devices based on experiments and simulations. The Fermi level pinning effect on the hole confinement is demonstrated to explain the differences mentioned above.

2. Device fabrication and simulation

All the device simulations for strained-Si and control Si are carried out by ISE [13], a commercial two-dimensional (2-D) numerical device simulator. The drift-diffusion device simulations were carried out to analyze the impact of Fermi level pinning on *C–V* characteristics of NMOS and PMOS devices. The simulator uses Fermi–Dirac statistics, and allows each of the relevant material parameters (substrate doping, oxide thickness, interface trap charge

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density, conduction band offset, and valence band offset) to be slightly varied to fit the measured data. The simulated and experimental device structure and the corresponding band diagram are shown in Fig. 1, and the substrate doping is 10^{17} cm^{-3}. The energy band models for unstrained SiGe and strained Si were generated based on [2,7,14]. The material properties used in the simulations are summarized as follows:

$$\chi_{\text{strained-Si}} = 4.05 + 0.6x \quad (1)$$

$$E_{\text{g(strained-Si)}} = 1.12 - 0.4x \quad (2)$$

$$\chi_{\text{SiGe}} = 4.05 \quad (3)$$

$$E_{\text{g(SiGe)}} = 1.12 - 0.43x + 0.206x^2 \quad (4)$$

$$\varepsilon_{\text{r(strained-Si)}} = 11.9 \quad (5)$$

$$\varepsilon_{\text{r(SiGe)}} = 11.9 + 4.1x \quad (6)$$

where x is the Ge fraction in $Si_{1-x}Ge_x$ layer, χ is the electron affinity, E_g is the band gap energy and ε_r is the relative permittivity. The mobility parameters in this study were simply modified with Ge content x and the quantum mechanical effects were considered to ignore. The mobility enhancement factors of $1 + 3.5x$ and $1 + 5x$ are used for electrons and holes in the strained Si, respectively, while the SiGe layer has a lower electron mobility of $1 - 3.7x$ and a lower hole mobility of $1 - 2x$ as compared to control Si. The type II band alignment of strained Si/SiGe heterojunction can have the electron confinement in the conduction band of the strained Si, and the hole confinement at strained Si/SiGe heterojunction.

The epitaxial SiGe graded layers (Ge content increased from 0% to 20%) with the thickness of ~1 μm were deposited on Si(100) wafers by ultra-high-vacuum chemical vapor deposition (UHVCVD) using silane (SiH_4) and germane (GeH_4) precursors at 600 °C. Then, a relaxed SiGe layers (~1 μm-thick) with uniform Ge content of 20% were deposited on the graded SiGe layers. Finally, the strained-Si layers with different thicknesses (12–24 nm) were grown on relaxed $Si_{0.8}Ge_{0.2}$ buffer layers. The strain (~0.64%) in Si layers is measured by surface Raman spectroscopy. The MOSFET devices were fabricated with a design rule of 0.8 μm on 100 mm-wafer line. After the device process, the tensile strain in the strained Si layers increases due to the additional relaxation of $Si_{0.8}Ge_{0.2}$ buffer layers. The strained-Si with thicknesses of 12, 18 and 24 nm was used for NMOS devices with the in situ channel doping of B_2H_6 (1 sccm) during deposition of the film. The PMOS devices with the undoped strained-Si thickness of 20 nm was ex situ doped by implantation of PH_3 with the energy of 300, 180 and 50 keV at the doses of 8×10^{11}, 4×10^{11} and 5×10^{11} cm^{-2}, respectively. The projected range of N ions is estimated to be ~0.65 μm. The channel doping activation of PMOS devices was done using a furnace annealing treatment of 900 °C and 25 min. To avoid the strain relaxation in the strained-Si channel, the 30-nm-thick low temperature (~700 °C) oxide tetraethylorthosilicate (TEOS) was used as a gate oxide. The S/D doping activation temperature and time were 900 °C and 30 s, respectively, for both NMOS and PMOS devices. After the device process, the channel doping concentration was estimated to be $\sim 1 \times 10^{17}$ cm^{-3} for NMOS and $\sim 3 \times 10^{16}$ cm^{-3} for PMOS devices. The interface trap charge density (D_{it}) at midgap energy, extracted by high-low frequency C–V method, is about 1×10^{11} cm^{-2} eV^{-1}, which is acceptable for Si MOSFET technology.

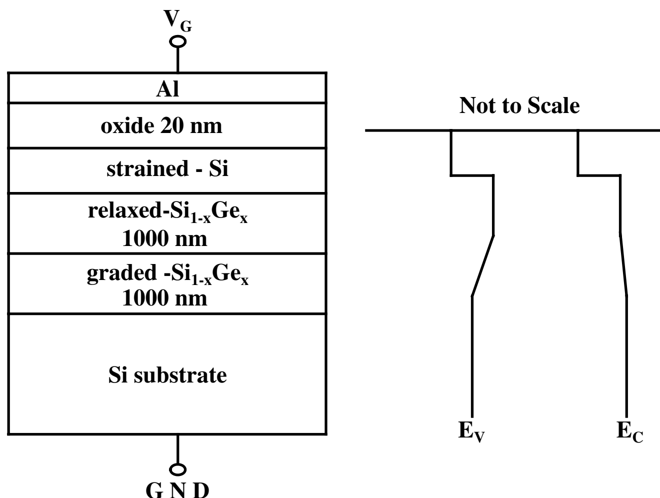

Fig. 1. Layer structure and schematic band diagram of strained-Si/$Si_{1-x}Ge_x$/Si MOS capacitor.

3. Results and discussion

Fig. 1 shows the MOS capacitor structure used for the characterization of oxide/strained-Si/relaxed $Si_{1-x}Ge_x$ quantum well and the band diagram also shows the formation of the well in the valence band. Fig. 2(a) and (b) compares the quasi-static C–V characteristics of strained-Si NMOS and PMOS capacitors, respectively, with the experimental data and the simulated result. In NMOS capacitor, the more obvious plateau in the accumulation region clearly shows the hole confinement at the strained-Si/relaxed SiGe heterojunction at a lower gate bias value. When the capacitors are driven from deep depletion to the accumulation region, the accumulated holes reside initially in the relaxed SiGe layer and the MOS exhibits a lower capacitance due to hole confinement giving rise to the plateau. As the structure is biased more negatively, the capacitance saturates to the oxide capacitance in the accumulation region. But in PMOS capacitor, the same phenomenon is not so evident in the inversion region. Fig. 3(a) and (b) presents the band diagram for strained-Si NMOS and PMOS capacitors with different gate biases. The energy between the Fermi level and the valence band must be pinned for NMOS capacitor far from the oxide/strained-Si interface, since no depletion region is formed at accumulation bias and little electrostatic potential cross the Si/SiGe heterojunction. The valence band moves upward slowly with increasing negative gate bias and the

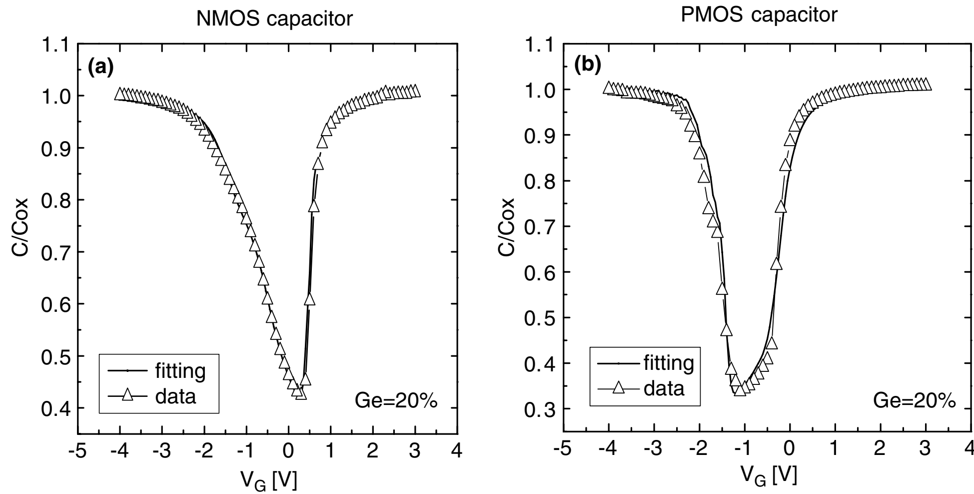

Fig. 2. Measured and simulated quasi-static C–V characteristics of the hole confinement at the strained-Si/relaxed $Si_{0.8}Ge_{0.2}$ interface for (a) NMOS capacitor with 12-nm-thick strained-Si and (b) PMOS capacitor with 20-nm-thick strained-Si.

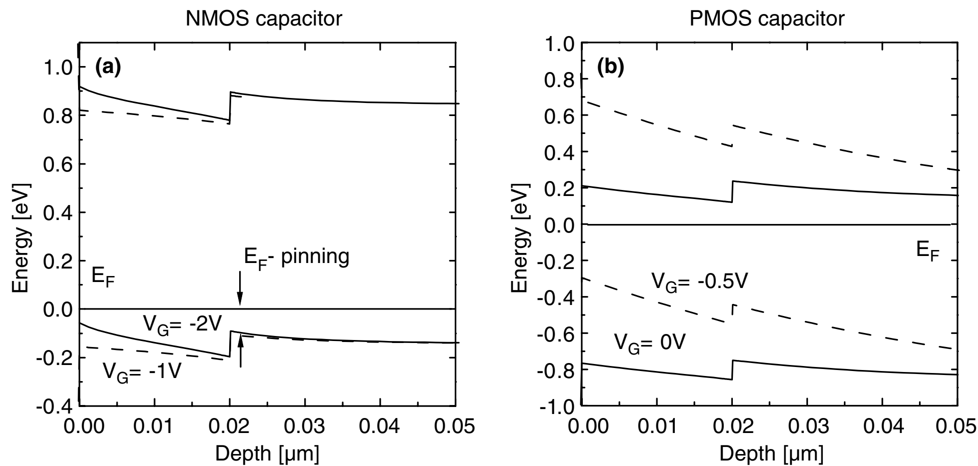

Fig. 3. Simulated energy band diagrams of strained-Si/relaxed $Si_{0.8}Ge_{0.2}$ heterojunctions with different gate biases for (a) NMOS and (b) PMOS capacitors.

accumulation holes are easily confined at the band offset and stay in the buried channel. On the other hand, the electrostatic potential from the depletion region can easily change the energy between the Fermi level and the valence band in PMOS capacitor. So it is revealed that the valence band moves upward faster in the weak inversion region of PMOS capacitor than in accumulation region of NMOS capacitor. The inversion holes initially residing the buried channel enter the surface channel quickly, making the C–V plateau in the inversion region not so evident for PMOS capacitor.

In strained-Si PMOSFETs, the negative band offset is linearly proportional to the Ge content (=0.6x) in the relaxed $Si_{1-x}Ge_x$ as shown in Fig. 4. The hole concentration at the strained-Si/relaxed SiGe heterojunction increases with increasing the Ge content because the increasing valence band offset pushes the valence band spike close to the Fermi energy in PMOSFETs and forms a parasitic buried channel confining a substantial amount of holes at the interface between the strained-Si and SiGe [15]. Thus, the ratio of inversion hole density at the surface channel to that at the buried channel decreases with raising the Ge content as shown in the solid triangle line in Fig. 5. The solid circle curve shows the correlation between the hole density ratio mentioned above and the strained layer thickness. If the strained-Si thickness is smaller, the electrostatic potential cross the strained-Si is also smaller, and the valence band at the heterojunction will be closer to the Fermi level, that is, there are more holes at the buried channel with smaller strain layer thickness. On the other extreme, the larger thickness and the larger depletion region make the valence band at the heterojunction further from the Fermi level with fewer holes at the buried channel. Therefore, the inversion hole density ratio increases with the raise of the strained layer thickness. This result suggests that more Ge content in the relaxed buffer and smaller

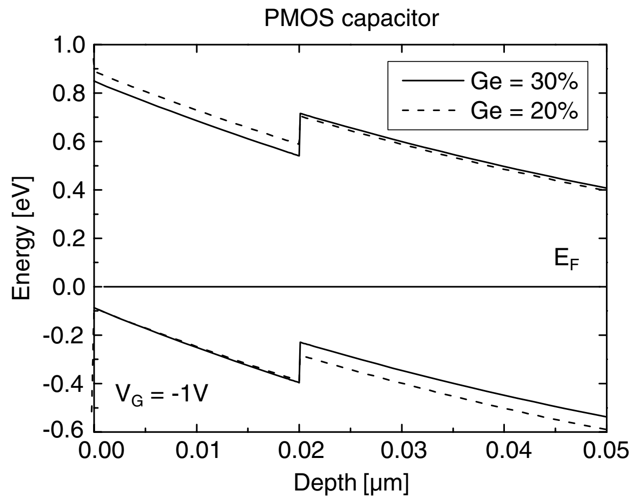

Fig. 4. Simulated energy band diagram of PMOS capacitor with different Ge contents in the relaxed SiGe buffer layers. It is observed that more strain (for high Ge content SiGe buffer) result in more negative valence band offset at the strained-Si layer and make the valence band spike at the strained-Si/SiGe interface closer to the Fermi level, inducing more hole concentration at the strained-Si/SiGe heterojunction.

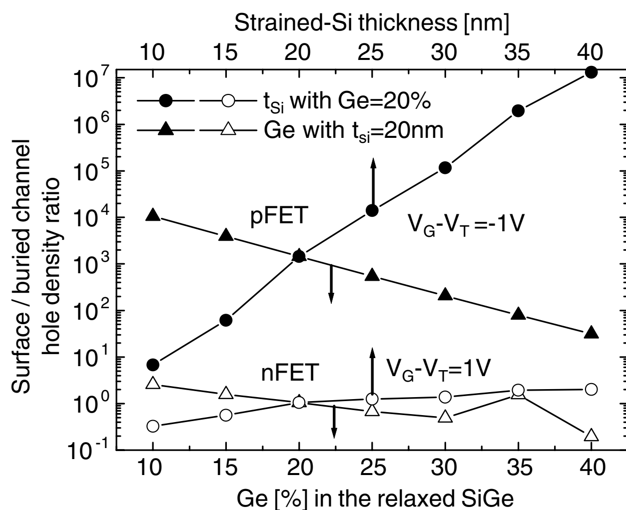

Fig. 5. Triangle symbols represent the simulated hole density ratio as a function of Ge content in the relaxed SiGe layer with 20-nm-thick strained-Si layer and circle symbols represent the simulated hole density ratio as a function of strained-Si layer thickness with 20% Ge content. The solid symbol represents PMOSFETs and the hallow symbol represents NMOSFETs. The gate length of all MOSFETs is 1.0 μm.

strained layer thickness make PMOSFETs to have more buried-channel conduction. In order to sustain the enough large inversion hole density ratio, less Ge content and larger strained layer thickness must be chosen. The strained layer thickness also needs to be thick enough to confine the wave function to keep the mobility enhancement [16], but less strain is a trade-off to mobility enhancement.

The accumulated hole density ratio in strained-Si NMOSFETs is presented with hollow symbol curves as shown in Fig. 5. The trend in NMOSFETs is consistent with that in PMOSFETs because of the same reason. But the hole density ratio in NMOSFETs shows much lower due to the Fermi level pinning effect, which makes hole easily to be confined at the heterojunction.

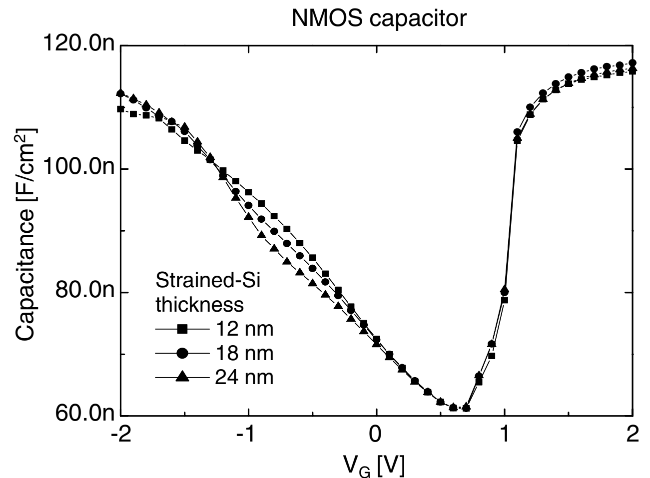

Fig. 6. The *C–V* characteristics of NMOS capacitors with different strained-Si thicknesses. The plateau due to hole confinement at the strained-Si/SiGe heterojunction is occurred at the lower capacitance when the strained-Si thickness is thicker.

The *C–V* characteristics are measured for different strained-Si layer thickness in NMOS capacitor as shown in Fig. 6. The thicker strained-Si thickness shows the plateau with lower capacitance, which occurs the hole confinement at strained-Si/SiGe heterojunction. So the *C–V* characteristics may be applicable for extraction of the strained-layer thickness, and the analytical model should be established.

4. Conclusion

The *C–V* characteristic of NMOS capacitor shows a more obvious plateau than that of PMOS capacitor, due to the Fermi level pinning effects on the hole confinement to the valence band offset at strained-Si/SiGe heterojunction. The ratio of hole density at the oxide/strained-Si interface to that at the strained-Si/relaxed SiGe interface for both N and PMOSFETs is investigated based on device simulations. For PMOSFETs, the result suggests that less Ge content and larger strained layer thickness must be chosen to sustain enough gate inversion hole density ratios. Since more strain and thinner strained layer are taken to keep mobility enhancement, the compromise must be made to solve the trade-off.

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