行政院國家科學委員會專題研究計畫　期中進度報告

總計畫(2/3)

計畫類別：整合型計畫
計畫編號：NSC92-2215-E-002-017-
執行期間：92 年 08 月 01 日至 93 年 07 月 31 日
執行單位：國立臺灣大學電子工程學研究所

計畫主持人：陳良基
共同主持人：吳安宇，張耀文，楊佳玲，賴永康，黃俊郎
計畫參與人員：陳良基，吳安宇 ，張耀文 ，楊佳玲 ，賴永康 ，黃俊郎

報告類型：精簡報告

處理方式：本計畫可公開查詢

中　華　民　國 93 年 6 月 1 日

多媒體通訊系統中可重組化運算技術之研究(2/3)

The Study on Reconfigurable Computing Technology for Multimedia Communication System

計劃編號：92-2215-E-002-017
執行期限：92/08/01　93/07/31
總計劃主持人：陳良基 教授　Email: lgchen@cc.ee.ntu.edu.tw
執行機構：國立台灣大學電子工程學研究所

一、中文摘要

本整合型技術發展研究計畫係針對可重組化運算此一新穎的系統架構研究領域之相關核心技術進行研究，並以多媒體通訊應用作為系統整合平台的發展目標。針對可重組化運算系統之研究趨勢，本整合型研究計畫的目的是研究多媒體通訊系統的數個可重組化運算之核心技術：首先對可重組化架構層次中的一般用途(General Purpose)、多媒體(Multimedia)與通訊(Communication)等重要的應用領域，進行新興應用的運算特性轉變之分析，然後進行架構的探討、設計與實現;同時在當前仍有待加強的系統整合 CAD 工具之研究上，也針對可重組化運算系統之應用發展的骨架以及架構的設計與實現上，提供系統層次的設計、軟/硬體整合設計、可測試性設計以及實體設計的完善工具支援。期望藉由此整合型計畫的相關基本技術之發展與研究成果的驗證，來發展出一套可重組化系統的設計法則與相關的設計軟硬體環境，以提供學術界與產業界在多媒體通訊系統架構的設計層次上，另一套前瞻性的設計經驗。

ABSTRACT

The group project will proceed on system analysis, suitable architecture design, and implementation, verification, and testing for key components for a reconfigurable computing system. We expect to provide a forward-looking experience in system-level architecture design for both academia and industry. In order to keep up with the research trend of reconfigurable computing systems, the goal of the main program targets at the research of core technology in various kinds of reconfigurable computing systems for multimedia communication systems. The analysis for characteristics of reconfigurable computing systems with the design and implementation of the hardware architectures are major topics of this main program. Besides, the consideration of testability for hardware design, hardware/software co-design, and support of CAD tool in physical layer design are also included.

二、各子計劃研究成果

■　子計劃一　（楊佳玲）

可重組化運算之系統分析與設計

1. System-Level Performance/Power Evaluation Framework

In this year, we have successfully built a hardware-software co-simulation framework in SsytemC. We have integrated an instruction set simulation together with the AMBA bus and an IDCT accelerator.

2. Task Scheduling of FPGAs

In cooperation with Prof. Yao-Wen Chang, we have derived a tree-based representation (T-tree) for 3D-floorplanning. We have also developed a SA (Simulated Annealing) engine based on the T-tree representation.

3. Energy-Efficient Reconfigurable Cache Architecture:

We have developed a hotspot cache which exploits the temporal and spatial locality in instruction streams for the I-cache energy reduction. We dynamically detect the hot spots in instruction streams and allocate them to the L0 cache.

■ 子計劃二（賴永康）
可重組化一般用途運算引擎之設計與實現暨可重組化運算系統整合平台之發展

The reconfigurable computing system consists of an ARM RISC processor, a reconfigurable computing engine, and other peripheral such as DMA controller and high bandwidth memory interface, which is the bridge between the AHB and the external main memory. ARM processor manages the high data-dependent operation and the control of the reconfigurable computing engine. The reconfigurable computing engine is the key component of the reconfigurable computing system. The architecture of the reconfigurable computing engine is shown below. The reconfigurable computing engine is composed of function units, data and instruction cache, and high flexible interconnection networks. The reconfigurable computing system can perform digital signal processing operation with high performance and flexibility, such as FSBMA and DCT algorithms and so on.

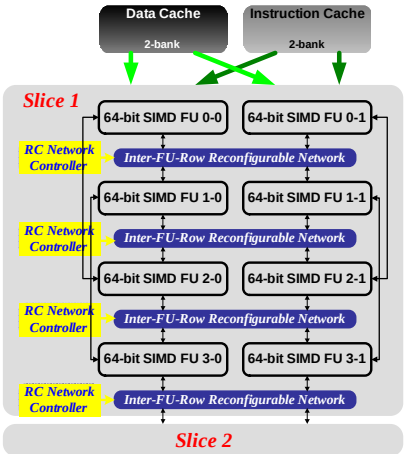

Fig. 1 系統架構

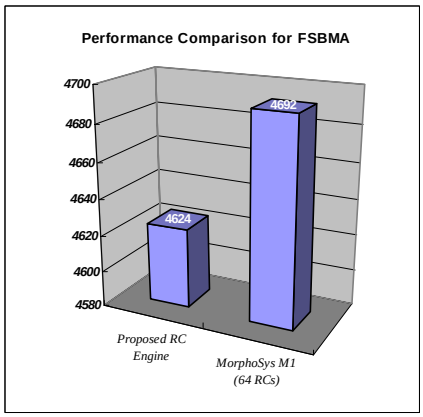

Fig. 2 FSBMA 效能比較

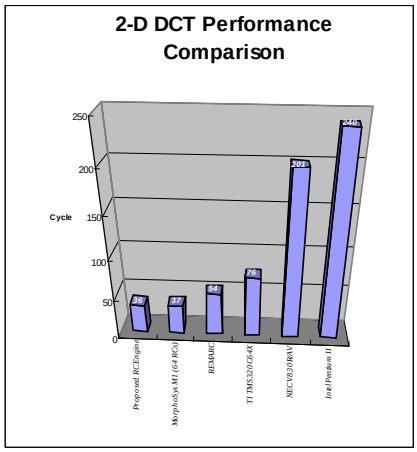

Fig. 3 2-D DCT 效能比較

■ 子計劃三 （陳良基）
可重組化多媒體運算引擎之設計與實現

在本年度的研究中，我們針對視訊編碼系統中的核心運算單元 -- Motion Estimation 做可重組化運算之設計考量，並且完成了兩個晶片設計，分別是 Ultra Low-Power Full-Search Motion Estimation Processor 和 Multi-Mode Power-Aware Reconfigurable Motion Estimation Processor。首先分析在視訊編碼系統中 Motion Estimation 為了提供功能彈性度而在運算上所增加的複雜度，接著針對該運算提出有效率的設計方法以得到最佳化的可重組化運算架構，進而完成架構之 FPGA 雛形與驗證和晶片實現與測試。

1. Ultra Low-Power Full-Search Motion Estimation Processor：

本超低功率全域搜尋移動估計處理器主要分為幾個部分，如 Fig. 4 所示。AG 控制記憶體讀取位置，RAM Buffers 減少外部記憶體讀取。提出的 Parallel Tree 架構計算比對誤差，Decision Unit 決定出正確的移動向量。增加運算的平行度，可有效的降低運算時脈，如一般二維陣列或是樹狀架構的解決方法，但是無法有效的省略不必要的運算。針對之前陣列架構以及樹狀架構的缺點，我們提出了 Parallel Tree 架構。Parallel Tree 架構不但能有效的增加運算平行度，而且能有效的省略不必要的運算以及減少緩衝區讀取位元數。

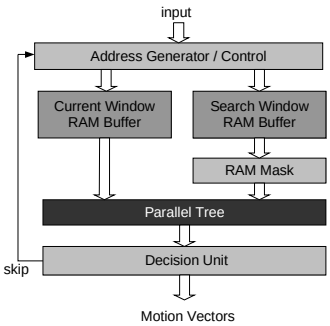

Fig. 4 LP-ME 功能方塊圖

2. Multi-Mode Power-Aware Reconfigurable Motion Estimation Processor：

提出的 Power-Aware 演算法主要根據兩個條件：判斷移動向量的複雜度，以及判斷移動向量的準確度。定義處理目前區塊時，周圍區塊的移動向量複雜度為左方、上方、及右上方移動向量的 variance。當 variance 很小時，以 MV 為中心點作快速演算法代替全搜尋區塊比對演算法，能夠大量減少運算且得到不錯的運算品質。這些快速演算法計算出移動向量的正確與否，絕大部分取決於一開始的預測向量是否準確。當計算完預測向量所指的候選區塊後，會得到比對後的最小 SAD 值。假如這 SAD 值超過一定範圍，可以得知這些預測向量是不太準確的，這時就可用適合移動向量較複雜的演算法以提昇運算品質。綜合以上判斷法則，提出的 Power-Aware 演算法如 Fig. 5 所示。A1 為適合移動向量較單純的演算法，而 A2 為適合移動向量較複雜的演算法。

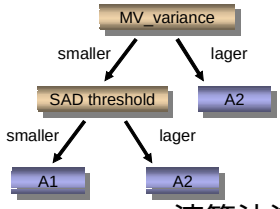

Fig. 5 Power-Aware 演算法流程圖

■ 子計劃四 （吳安宇）
可重組化通訊運算引擎之設計與實現

With the advent of the 2G/2.5G/3G high-speed telecommunication, the communication system of multi-standard / multi-mode and the multi-mode in single standard has become a trend as to offer a variety of communication services. In the 1st year of this project, we have finished the following three *Reconfigurable Communication Engines* (RCE), which are common in communication systems, Viterbi decoder, Reed Solomon encoder/decoder, and Fast Fourier Transform (FFT) processor. This year we integrate these three RCEs into a multimode communication system.

The chosen standard, *Digital Video Broadcasting-Terrestrial* (DVB-T), is the next generation of digital television, which is the future trend of video. DVB-T adopts Coded Orthogonal Frequency Division Multiplexing (COFDM) technology. FFT processor used for demodulation has 2k and 8k mode. Forward Error Correction (FEC) adopts Viterbi decoder and Reed Solomon decoder to be inner decoder and outer decoder. Viterbi decoder with generation polynomial $(171, 133)_{oct}$ support 5 kinds of code rate, 1/2、2/3、3/4、5/6 and 7/8. And RS(204, 188, t = 8) Reed Solomon code is adopted.

We use Simulink to build up each module for system integration. First floating point simulation is performed for functional verification and then fixed point simulation for hardware wordlength optimization.

Configure the RCE and integrate with the other necessary modules like deinterleaver and FEQ. Verify the system with pattern generated by Simulink. By utilizing RCE which meets various communication standards, we can reuse modules and build up communication systems fast.

■ 子計劃五 （張耀文）
可重組化系統之實體設計

Improving logic capacity by time-sharing, dynamically reconfigurable FPGAs are employed to handle designs of high complexity and functionality. In this report, we model each task as a 3D-box and deal with the temporal floorplanning / placement problem for dynamically reconfigurable FPGA architectures. We present a tree-based formulation, called T-tree, to represent the spatial and temporal relations among tasks. Each node in a T-tree has at most three children which represent the dimensional relationship among tasks. We present an efficient packing method and derive the condition to ensure the satisfaction of precedence constraints which model the temporal ordering among tasks induced by the execution of dynamically reconfigurable FPGAs. If a T-tree results in an infeasible placement, the T-tree is re-constructed to remove the violation conditions. To reduce the probability that a T-tree results in an infeasible placement after an operation, we filter out a set of operations that will definitely introduce precedence violations. Besides the classical 3D-floorplanning problem that minimizes the product of the area and execution time (i.e., the volume of the 3D floorplan/placement), in this report, we also propose a novel T-tree based SA mechanism to handle the fixed-outline floorplanning problem, for which the area of a reconfigurable device is fixed.

■ 子計劃六 （黃俊郎）
可重組化運算之測試設計

Microprocessor Self-Testing Technique:

In the area of microprocessor testing, we are interested in structural defect oriented self-testing program generation. Currently, we use the Parwan processor as the research vehicle.

Under the assumption that no Design-for-Testability hardware, e.g., scan design, is utilized, we first perform sequential test generation, using TetraMAX, to generate test sequences for the Parwan processor. Even though the processor itself is quite simple, the overall fault coverage is only 46%, which is unacceptable.

Then, we use the proposed test program generation technique to generate a test program for the ALU's stuck-at faults. First, combinational ATPG was performed on the ALU block to obtain the ALU test vectors. Note that we add some circuitry to the ALU's input part to ensure that the generated test patterns can be realized with instruction sequences. The ALU test patterns are then converted to a test program. To evaluate the test program's quality, we also implement a fault coverage evaluation framework. The test program achieves 92.2% fault coverage in the ALU block, and 73.2% fault coverage in the whole Parwan processor, which shows that the proposed technique is promising.

We are currently working on test programs for other blocks. Then, we will study other processor cores, e.g., the RISC 8 core and the CMU DSP core, to gain more experience.

三、結論

本整合型計畫在第二個年度中，各個子計劃皆已順利完成預定之目標，在接下來的年度中，將繼續朝著預定的目標，針對可重組化運算研究領域之相關核心技術

進行研究，並以多媒體通訊應用作為系統整合平台的發展目標。