

Fig. 5. (a) Forward voltage drop versus d/m ratio at a forward current density of 100 A/cm^2 and (b) reverse leakage current density versus d/m ratio at a reverse bias of 25 V for the ShOC and the LMDS rectifiers. Here the trench width w is varied for a fixed m .

advantage of using only one high-barrier Schottky metal contact. The ShOC rectifier also exhibits significantly enhanced breakdown voltage compared to the conventional high-barrier or low-barrier Schottky rectifiers. The combined low forward voltage drop and excellent reverse blocking capability make the proposed ShOC rectifier attractive for use in low-loss high speed smart power IC applications.

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An Analysis of Base Bias Current Effect on SiGe HBTs

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Abstract—The anomalous dip in scattering parameter S_{11} of SiGe heterojunction bipolar transistors (HBTs) is explained quantitatively for the first time. Our results show that for SiGe HBTs, the input impedance can be represented by a "shifted" series RC circuit at low frequencies and a "shifted" parallel RC circuit at high frequencies very accurately. The appearance of the anomalous dip of S_{11} in a Smith chart is caused by this inherent ambivalent characteristic of the input impedance. In addition, it is found that under constant collector-emitter voltage (V_{CE}), an increase of base current (which corresponds to a decrease of base-emitter resistance (r_π) and an increase of transconductance (g_m)) enhances the anomalous dip, which can be explained by our proposed theory.

Index Terms—Anomalous dip, base current, heterojunction bipolar transistor (HBT), S -parameters, SiGe.

I. INTRODUCTION

The anomalous dips in scattering parameters S_{11} and S_{22} of MOSFETs/MESFETs and scattering parameter S_{22} of bipolar junction transistors/heterojunction bipolar transistors (BJTs)/HBTs, which have been explained quantitatively [1]–[3], can be seen frequently in the literature [4], [5]. However, the anomalous dip in scattering parameter S_{11} of BJTs/HBTs has never been reported. In this paper, the anomalous dip in S_{11} of SiGe HBTs is reported and explained quantitatively for the first time. It is found that under constant collector-emitter voltage (V_{CE}), an increase of base current (I_B) enhances the anomalous dip. That is to say, for devices with lower base-emitter resistance (r_π) and higher transconductance (g_m), the anomalous dip is more prominent.

The concept of dual-feedback circuit methodology is used to simplify the circuit analysis of the hybrid π -model of a SiGe HBT and then the input impedance of the HBT is derived. The formula shows that the input impedance of the HBT follows a "shifted" constant resistance (r) circle at low frequencies and then a "shifted" constant conductance (g) circle at high frequencies, which is in good agreement with the experimental results.

II. DEVICE STRUCTURE AND S_{11} VERSUS BASE CURRENT

The HBTs studied in this paper were fabricated with a $0.35\text{-}\mu\text{m}$ BiCMOS technology. The frequency-dependent S -parameters measurements were performed from 0.1 to 50 GHz in a common-source configuration by an HP-8510C network analyzer. Before the measurements, a full two-port short load open through calibration was done on a separate alumina impedance standard substrate to calibrate the measurements to the probe tips. This setup together with Cascade air coplanar ground-signal-ground probes was able to provide reliable RF measurements.

Small-signal hybrid π -models of the SiGe HBTs were created for studying the anomalous dip in scattering parameter S_{11} [see Fig. 2(a)]. The pad parasitic effect could be modeled by an equivalent C component parallel to a series LR circuit. The followings are a brief description of the steps. First, the S -parameters of the four on-wafer dummy

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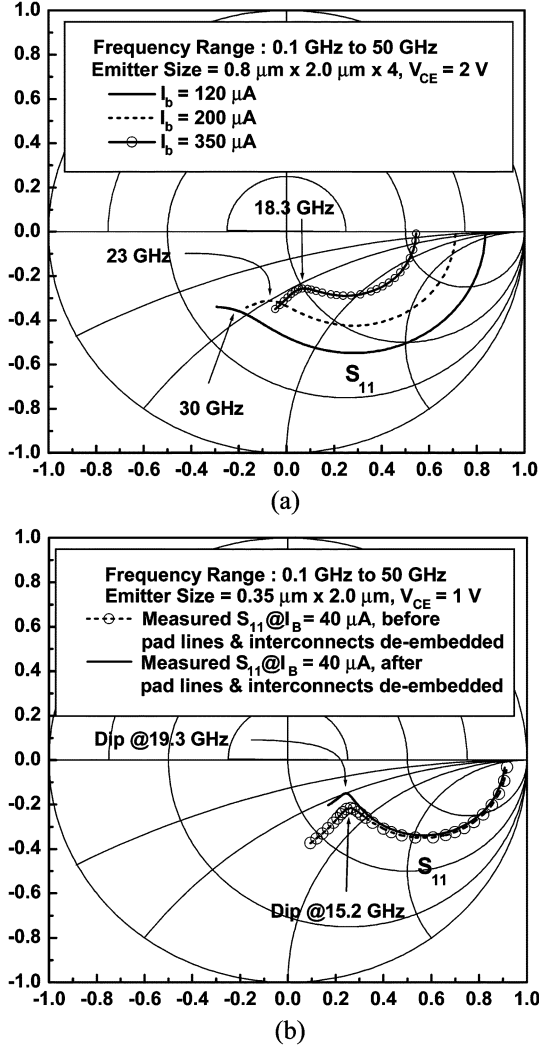


Fig. 1. (a) Measured scattering parameters S_{11} of a SiGe HBT with emitter size of $0.8 \times 2.0 \mu\text{m} \times$ (four fingers) biased at $V_{CE} = 2 \text{ V}$ and $I_B = 120, 200, \text{ and } 350 \mu\text{A}$. (b) The measured scattering parameters S_{11} before and after pad lines and interconnects de-embedded of a SiGe HBT with emitter size of $0.35 \times 2.0 \mu\text{m}$ biased at $V_{CE} = 1 \text{ V}$ and $I_B = 40 \mu\text{A}$.

structures (namely, an *open*, a *short1*, a *short2*, and a *through*) were measured and converted to Y-parameters using a conversion table [6]. Then, the values of the parasitic parameters [i.e., $R_b, R_e, R_c, L_b, L_e, L_c, C_{pbe}$, and C_{pce} in Fig. 2(a)] were obtained based on the analytical transformations proposed by Vandamme, Schreurs, and Dinther [7]. And then, the intrinsic device Y-parameters were deduced by using the three-step de-embedding procedure [7], [8]. Finally, the values of the intrinsic parameters were obtained based on the analytical transformations proposed by S. Bousnina *et al.* [4].

Fig. 1(a) shows the measured scattering parameter S_{11} of a SiGe HBT with four connected emitter fingers. The emitter size is $0.8 \times 2 \mu\text{m}$ per finger. The bias conditions are V_{CE} equal to 2 V and I_B equal to 120, 200, and 350 μA . The measurements range from 0.1 to 50 GHz. The extracted r_π is 400.1, 161.9, and 64.3 Ω , respectively, for devices biased at V_{CE} equal to 2 V and I_B equal to 120, 200, and 350 μA . In addition, the extracted g_m is 0.27, 0.56, and 1.11 S, respectively, for devices biased at V_{CE} equal to 2 V and I_B equal to 120, 200, and 350 μA . That is to say, under constant V_{CE} , an increase of base current corresponds to a decrease of r_π and an increase of g_m , which makes the anomalous dip more prominent. A further discussion will be given in Section IV.

Fig. 1(b) shows the measured scattering parameters S_{11} before and after pad lines and interconnects de-embedded of a SiGe HBT with emitter size of $0.35 \times 2.0 \mu\text{m}$. The bias condition is V_{CE} equal to 1 V and I_B equal to 40 μA . The measurements range from 0.1 to 50 GHz. As can be seen, after the pad lines and interconnects [i.e., $R_b, R_e, R_c, L_b, L_e, L_c, C_{pbe}$, and C_{pce} in Fig. 2(a)] are de-embedded, the kink frequency increases from 15.2 to 19.3 GHz. This means the series RL elements due to pad lines and interconnects can enhance the dip phenomenon in the S_{11} parameters. However, the dip phenomenon in S_{11} is an inherent characteristic of HBTs. That is to say, it originates from the interaction of the intrinsic parameters $r_\pi, C_\pi, C_\mu, C_{\mu 1}, R_{bin}, g_m$, and r_o . A further discussion will be given in Section IV.

For the measured S -parameters of the SiGe HBT with emitter size of $0.8 \times 2 \mu\text{m} \times$ (four fingers) shown in Fig. 1(a), the base current level is high. Therefore, a base capacitance (C_b) should be added to the intrinsic base resistance (R_{bin}) in parallel to model the current crowding effect [9], [10]. That is, both ac and DC current crowding effects might play an important role for the abnormal behavior of S_{11} . To simplify the analysis and to verify the dip phenomenon is an intrinsic characteristic for SiGe HBTs, in the following, we will focus on the analysis of the measured data of the typical device (i.e., the HBT with emitter size of $0.35 \times 2.0 \mu\text{m}$) which has less influence from current crowding effect.

III. THEORY

The setup for the measurement of transistor S -parameters is shown in Fig. 2(a), where $Z_O (= 1/Y_O)$ equals to 50 Ω and is connected to the input and output ports of the device under test. S_{11} and S_{21} can be measured by setting $V_2 = 0$ and $V_1 \neq 0$, while S_{22} and S_{12} can be measured by setting $V_1 = 0$ and $V_2 \neq 0$. What is also shown in Fig. 2(a) is the extracted small-signal hybrid π -model of the SiGe HBT with emitter size of $0.35 \mu\text{m} \times 2.0 \mu\text{m}$ biased at $V_{CE} = 1 \text{ V}$ and $I_B = 40 \mu\text{A}$. The values of " L_b " and " L_c " are nearly the same due to the symmetry in RF pad layout.

If the expression for the input impedance Z_{in} of this circuit has been found, then S_{11} is given by

$$S_{11} = \frac{Z_{in} - Z_O}{Z_{in} + Z_O}. \quad (1)$$

In general, it is hard to find the input impedance of the circuit in Fig. 2(a). However, the problem will be much easier to solve if the circuit is viewed as a dual-feedback circuit in which $R_e + j\omega L_e$ is the local series-series feedback element and $C_{\mu 1}$ is the local shunt-shunt feedback element. In addition, pad parasitic capacitances C_{pbe} and C_{pce} can be neglected because their effect is very small. In order to simplify the circuit analysis, we temporarily neglect the inductors and transform the circuit of Fig. 2(a) into that of Fig. 2(b) with some necessary circuit element modifications [3], which are also shown in Fig. 2(b). Note that the equivalent r (1.65 Ω) resulting from the parasitic inductance " L_e " is negligibly small.

The intrinsic input impedance defined in Fig. 2(b) can be expressed as (2) shown at the bottom of the next page where $g'_{m0} = g_{m0}/(1 + g_{m0}R_e)$, $C'_{\mu 1} = C_{\mu 1} + C_\mu$, $C'_\pi = C_\pi/(1 + g_{m0}R_e)$, $r'_\pi = r_\pi/(1 + g_{m0}R_e)$, $R'_{bin} = R_{bin}(1 + g_{m0}R_e) + R_e$, $g'_{m0} = (g'_{m0} \cdot r'_\pi)/(r'_\pi + R'_{bin}(1 + sC'_\pi r'_\pi/(1 + sC'_\pi r'_\pi)))$, $r = g_{m0}L_e/C_\pi$ (which is usually negligibly small), $r' = rR'_{bin} + rr'_\pi + R'_{bin}r'_\pi$, and R_L is the parallel combination of $Z_O + R_e$ and $r'_o (= r_o(1 + g_{m0}R_e))$. Once this intrinsic input impedance is known, the normal input impedance is simply the parallel combination of $Z_{in,i}$ and $[(1/sC'_\pi) + r] \parallel r'_\pi + R'_{bin}$, followed by a series combination with R_b as follows:

$$Z_{in} = R_b + \left[Z_{in,i} \parallel \left(\left(\frac{1 + sC'_\pi r}{sC'_\pi} \right) \parallel r'_\pi \right) + R'_{bin} \right] \quad (3)$$

$$\approx R_b + \left[Z_{in,i} \parallel \left(R'_{bin} + \frac{1}{sC'_\pi} \right) \parallel (r'_\pi + R'_{bin}) \right] \quad (4)$$

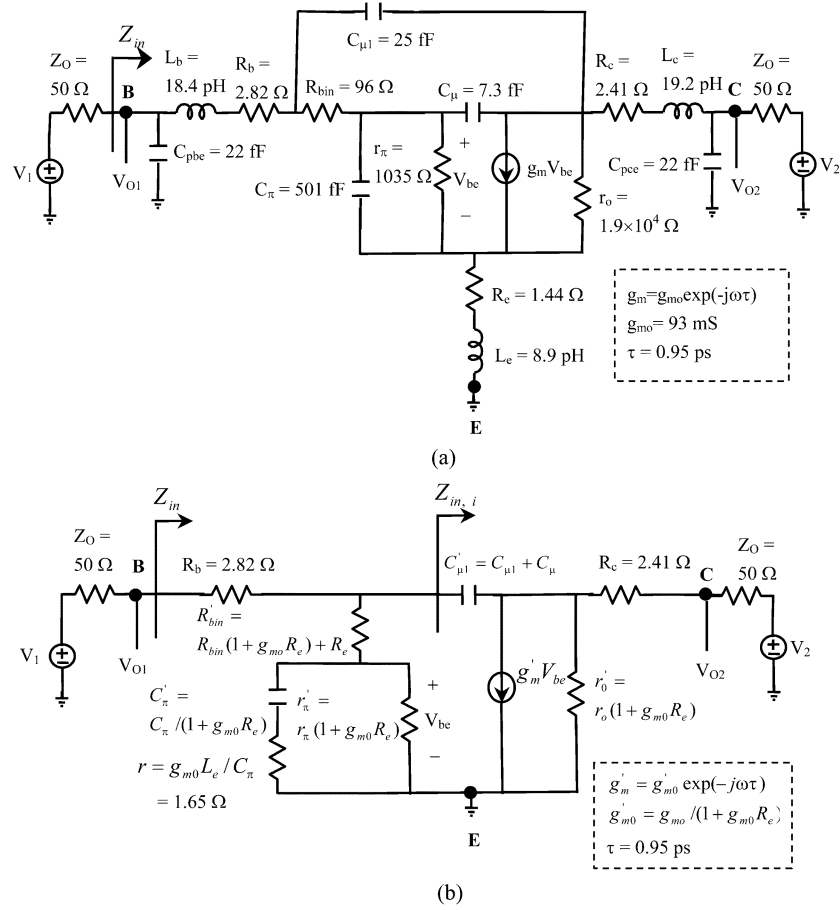


Fig. 2. Setup for the measurement of the SiGe HBTs S -parameters. (a) A complete circuit including a small-signal hybrid π -model and extracted equivalent circuit parameters of the SiGe HBT with emitter size of $0.35 \times 2.0 \mu\text{m}$ biased at $V_{CE} = 1 \text{ V}$ and $I_B = 40 \mu\text{A}$. (b) A simplified circuit with the local series-series feedback element (R_e) absorbed.

where $R_{bin}' = (r R_{bin}' + R_{bin}' r_{\pi}' + r r_{\pi}') / (r + r_{\pi}')$, and $C_{\pi}'' = C_{\pi}' (r + r_{\pi}') / (r_{\pi}' + R_{bin}')$. In (4), we assume that $(r_{\pi}' + R_{bin}') \gg s C_{\pi}' (r r_{\pi}' + r R_{bin}' + r_{\pi}' R_{bin}')$, which is usually the case.

At low frequencies, the input impedance can be simplified to a “shifted” series RC circuit as follows:

$$\begin{aligned}
 Z_{in} &\approx R_b + \left((r_{\pi}' + R_{bin}') \left\| \left(R_M \cdot \left(\frac{C_M}{C_{\pi}'' + C_M} \right)^2 + R_{bin}' \cdot \left(\frac{C_{\pi}''}{C_{\pi}'' + C_M} \right)^2 + \frac{1}{j\omega(C_{\pi}'' + C_M)} \right) \right\| \right) \\
 &= R_b + \left(r_1 \left\| \left(r_s + \frac{1}{j\omega C_s} \right) \right\| \right) \\
 &\approx r_1 \left\| \left(r_s + \frac{1}{j\omega C_s} \right) \right\|
 \end{aligned} \quad (5)$$

where $R_M = [C_{\mu 1}' R_L (r_{\pi}' + R_{bin}') + C_{\pi}' r'] / [C_{\mu 1}' (g_{m0}' r_{\pi}' R_L + r_{\pi}' + R_{bin}')] + s C_{\mu 1}' R_L C_{\pi}' r'$ and $C_M = C_{\mu 1}' (g_{m0}' r_{\pi}' R_L + r_{\pi}' + R_{bin}') / (r_{\pi}' + R_{bin}')$.

At high frequencies, the input impedance can be simplified to a “shifted” parallel RC circuit as (6) shown at the bottom of the next page where $R_b' = R_b + [R_e \parallel (R_c + 50)]$, $R_{bin}''' = R_{bin}' + r_{\pi}' (1 + g_{m0}' R_L)$, and $C_{\pi}''' = C_{\pi}' / (R_{bin}' + r_{\pi}')$.

From (5) and (6), we can find that the input impedance of HBTs follows a “shifted” constant r circle at low frequencies and then a “shifted” constant g circle at high frequencies. The appearance of the anomalous dip of S_{11} in a Smith chart is caused by this inherent ambivalent characteristic of the input impedance.

In addition, (5) can be applied to design 2.4/5.2/5.7 GHz multiband LNA for WLAN application (or 0.9/1.8/1.9 GHz multiband LNA for GSM application) achieved by switching between different base bias currents (I_B) [11]. A brief explanation for this is as follows. If we consider the input stage of the LNA shown in [11] (i.e., a common-emitter SiGe HBT with an input matching gate inductor L_G), the input impedance is equivalent to a series L_G - R_s - C_s network at the frequencies in interest. Since input capacitance C_s is a function of g_m (i.e., a function of I_B), it varies as I_B changes. Accordingly, the resonant frequency determined by C_s and L_G is changed. In turn, the resonant frequency for input matching also varies. As a result, the change of frequency bands can be achieved by switching between different base bias currents.

$$\begin{aligned}
 Z_{in,i} &= \frac{\frac{1}{s C_{\mu 1}'} + R_L}{1 + g_{m0}' R_L} \\
 &= \frac{(r_{\pi}' + R_{bin}') + s [C_{\mu 1}' R_L \cdot (r_{\pi}' + R_{bin}') + C_{\pi}' r'] + s^2 C_{\mu 1}' R_L C_{\pi}' r'}{s C_{\mu 1}' (g_{m0}' r_{\pi}' R_L + r_{\pi}' + R_{bin}') + s^2 C_{\mu 1}' C_{\pi}' [r r_{\pi}' g_{m0}' R_L + r']}
 \end{aligned} \quad (2)$$

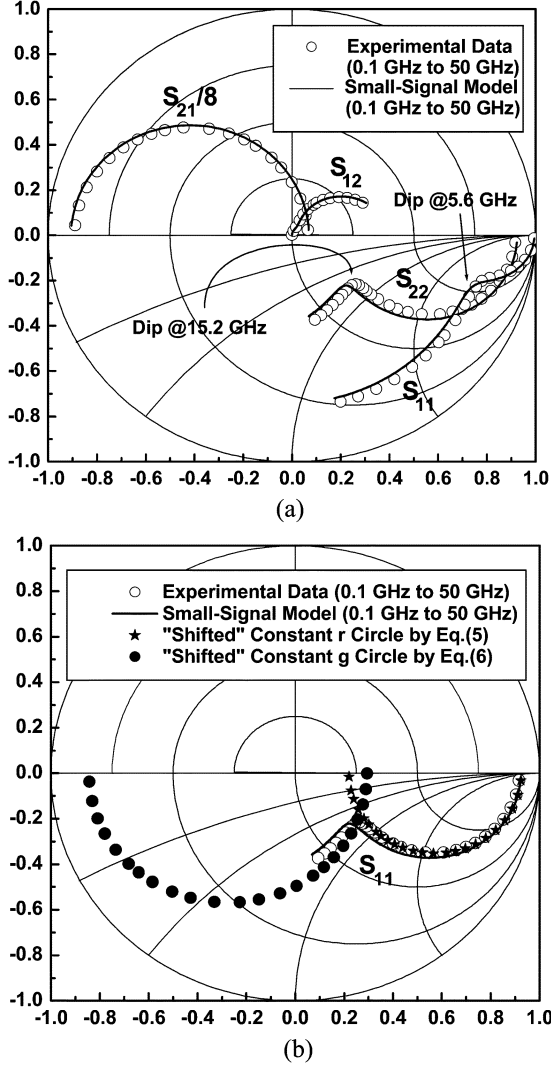


Fig. 3. (a) Measured and modeled S -parameters of the SiGe HBT with emitter size of $0.35 \times 2.0 \mu\text{m}$ biased at $V_{CE} = 1\text{ V}$ and $I_B = 40 \mu\text{A}$. (b) Comparison of the experimental and calculated scattering parameters S_{11} at low and high frequencies of the SiGe HBT with emitter size of $0.35 \times 2.0 \mu\text{m}$ biased at $V_{CE} = 1\text{ V}$ and $I_B = 40 \mu\text{A}$.

IV. RESULTS AND DISCUSSIONS

Fig. 3(a) shows the measured S -parameters from 0.1 GHz to 50 GHz of the SiGe HBT with emitter size of $0.3 \times 2.0 \mu\text{m}$ biased at $V_{CE} = 1\text{ V}$ and $I_B = 40 \mu\text{A}$. The anomalous dips of S_{11} and S_{22} appear at about 15.2 and 5.6 GHz, respectively. The S -parameters generated by the small-signal model are also shown in Fig. 3(a), which is in good agreement with the experimental results.

Fig. 3(b) shows the measured scattering parameters S_{11} and our calculated results at low and high frequencies based on (5) and (6).

The solid asterisks represent calculated “shifted” constant r circle according to (5). The calculated r_1 , r_s and C_s is 1283.9 and 80.0 Ω , and 0.563 pF, respectively, according to (5). The input impedance at low frequencies of BJTs/HBTs is not very large because r_π is connected in parallel with C_π . Therefore, S_{11} starts at a point where the resistance is equal to approximately $r'_\pi + R_b + R'_{bin}$ [or $R_b + r_1$ in (5)], and therefore, a “shifted” constant r circle is usually observed [12], [13]. This explains why in Fig. 1(a) the frequency = 0 point of S_{11} intercepts the real axis of the Smith chart at a smaller r value when I_B increases. In addition, this is different from MOSFETs/MESFETs where the input impedance at low frequencies is very large because of the simple series RC combination; therefore, S_{11} starts at a point near the open circuit point of the Smith chart, which makes the low frequency characteristics of S_{11} of MOSFETs/MESFETs follow a simple constant r circle. What is also shown in Fig. 3(b) is the calculated “shifted” constant g circle according to (6). The calculated g_p and C_p is 11.5 mS and 44.1 fF, respectively, for the “shifted” parallel RC circuit.

The reason why under constant V_{CE} , an increase of I_B makes the anomalous dip more prominent [see Fig. 1(a)] can be explained as follows. An increase of I_B makes the values of r_π lower and g_m higher (see Section II), then from (5) and (6), r [i.e., r_s in (5)] increases and g [i.e., g_p in (6)] decreases, and hence, the anomalous dip moves to a new intercept point with a larger r , a smaller g , and a smaller frequency, which makes the anomalous dip more prominent. It is the inherent ambivalent characteristic (“shifted” constant r circle at low frequencies and then “shifted” constant g circle at high frequencies) of the input impedance that causes the appearance of the dip of S_{11} in a Smith chart. That is, the “anomalous dip” is a “normal behavior” of S_{11} . From the perspective of device physics, the appearance of the dip has nothing to do with any nonideal characteristic due to device defects or trapping of carriers, etc. It simply results from the interaction among r_π , C_π , C_μ , $C_{\mu 1}$, R_{bin} , g_m , and r_o . If any of the previous terms cause an increase of r and a decrease of g , then the dip will become more prominent.

V. CONCLUSION

In this brief, the anomalous dip in scattering parameters S_{11} of SiGe HBTs is reported and explained quantitatively for the first time. Our results show that for SiGe HBTs, the input impedance can be represented by a “shifted” series RC circuit at low frequencies and a “shifted” parallel RC circuit at high frequencies. The appearance of the anomalous dip of S_{11} in a Smith chart is caused by the inherent ambivalent characteristic of the input impedance. The calculated S_{11} based on the proposed analytical expressions is in good agreement with the measurement results of SiGe HBTs. The present analyzes enable RF engineers to understand the behaviors of S -parameters more deeply, and hence are helpful for them to create a broadband model of HBTs for designing multibands radio-frequency integrated-circuits (RF-ICs).

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$$Z_{in} \approx R'_b + \left\{ \frac{C'_\pi [C'_{\mu 1} R_L (r + r'_\pi) + (C'_{\mu 1} + C''_{\pi} (r + r'_\pi)) R'_{bin} r'_\pi] + C''_{\pi} C'_{\mu 1} [R_L R'_{bin} r'_\pi + R'_{bin} r']}{C'_\pi C'_{\mu 1} R_L (R'_{bin} r'_\pi + r') + r' C'_\pi C''_{\pi} R'_{bin} r'_\pi} \right. \\ \left. + j\omega \left[\frac{C''_{\pi} C'_{\mu 1} R'_{bin} r'_\pi [(r + r'_\pi) R_L + r']}{C'_\pi C'_{\mu 1} R_L (R'_{bin} r'_\pi + r') + r' C'_\pi C''_{\pi} R'_{bin} r'_\pi} \right] \right\}^{-1} = R'_b + (g_p + j\omega C_p)^{-1} \quad (6)$$

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Effects of PAI on Interface Properties Between HfSiO Gate Dielectric and Silicon Substrate

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Abstract—The effects of preamorphization implantation (PAI) on the interface properties between hafnium-silicate (HfSiO) gate dielectrics and silicon substrates were examined. In the case of an NH_3 nitrided interface, it was found that the PAI can improve the interface trap density (D_{IT}) compared with the no PAI case. However, for the PAI samples, it was also found that samples with sacrificial screening oxide (Sac Ox) had worse interface properties compared with the samples without Sac Ox. It is attributed to the recoiled oxygen from Sac Ox during PAI.

Index Terms—Gate dielectrics, silicon process technology.

I. INTRODUCTION

Recently, alternative high- κ gate dielectrics are being investigated for sub-100-nm MOSFET to suppress the high gate leakage found in conventional silicon dioxide (SiO_2) gate transistors. Good interface

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TABLE I
SUMMARY OF PROCESS SPLIT CONDITIONS

ID	Preamorphization Implantation (PAI)	Intentionally made Interface Layer
A1	No PAI	Thermally grown SiO_2 & Oxynitrided by O_3/NH_3 PDA
A2	No PAI	Chemically Oxynitrided by O_3/NH_3 PDA
A3	No PAI	Chemically Nitrided by NH_3 PDA
B1	PAI	Thermally grown SiO_2 & Oxynitrided by O_3/NH_3 PDA
B2	PAI	Chemically Oxynitrided by O_3/NH_3 PDA
B3	PAI	Chemically Nitrided by NH_3 PDA
C1	PAI with Sac Ox	Thermally grown SiO_2 & Oxynitrided by O_3/NH_3 PDA
C2	PAI with Sac Ox	Chemically Oxynitrided by O_3/NH_3 PDA
C3	PAI with Sac Ox	Chemically Nitrided by NH_3 PDA

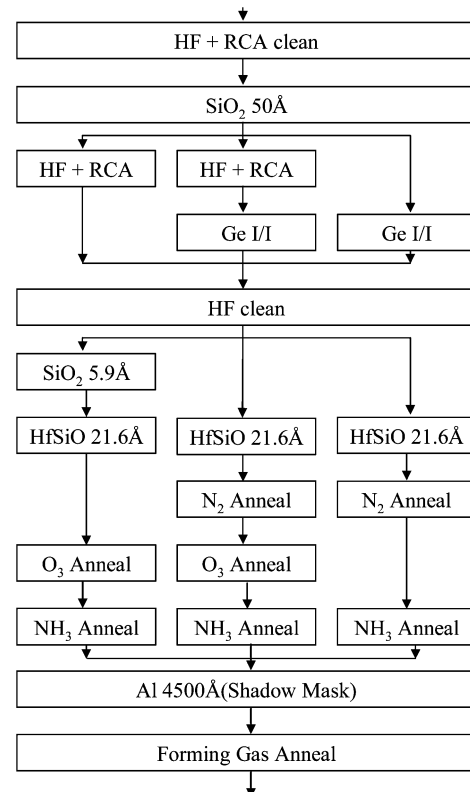


Fig. 1. Fabrication process flow.

properties between high- κ and silicon are among the several requirements for high- κ dielectrics. In this brief, the interface properties of samples with a preamorphization implantation (PAI) prior to the high- κ dielectrics deposition were compared to those without PAI. PAI samples were recrystallized by rapid thermal annealing (RTA) after high- κ