CMOS Current-Mode Divider and Its Applications

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***Abstract*—Compact, accurate and low-power analog CMOS circuits for current-mode division and pseudo-exponential function generation are presented, based on a new variable transresistance amplifier. Experimental results of the circuits fabricated in a 0.5-μm 2P2M n-well CMOS process show better than 0.3% total harmonic distortion. Measured power is less than 0.22 mW at 100-MHz bandwidth and $\pm$1.5-V supply voltages.**

***Index Terms*—Divider, exponential function, transresistance.**

I. Introduction

THE ANALOG divider is an important building block in the design of analog signal processing integrated circuits, such as analog computation, fuzzy control, neural network, and analog–digital (A/D) converters and communication systems [1]–[6], etc. However, most of the analog dividers operate in the voltage mode [4], [7]–[9] and only few of them are designed to operate in the current mode [10], [11]. In the past decade, current-mode signal processing has received much attention for their potential advantages such as wide bandwidth, wider dynamic range, simple circuitry, and lower power consumption [12]. In this brief, a new CMOS current-mode divider is presented. Two different applications are presented to demonstrate the proposed current-mode divider. Experimental results of all the proposed circuits are given to verify the theoretical analysis.

II. Circuit Description

Consider the circuit shown in Fig. 1 [13]. Assume that both M1 and M2 are biased in the triode region without body effect, their drain currents are given by [14]

$$I_1 = \frac{K_{n1}}{2}\left(2(-V_{SS} - V_{\mathrm{Tn1}})V_{DS1} - {V_{DS1}}^2\right) \tag{1}$$

$$I_2 = I_{\mathrm{in}} + I_4 = \frac{K_{n2}}{2}\left(2(V_{G2} - V_{SS} - V_{\mathrm{Tn2}})V_{DS2} - {V_{DS2}}^2\right) \tag{2}$$

where V_{G2} is a bias voltage, $K_{n1,2}$ are the transconductance parameters and $V_{\mathrm{Tn1,2}}$ are the threshold voltages of M1 and M2,

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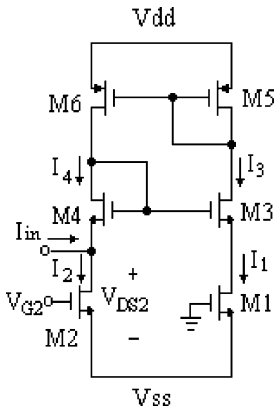

Fig. 1. Proposed voltage-controlled resistor.

respectively. The current mirrors M5 and M6 are used to generate the current I_3 and I_4, so that

$$I_3 = I_4 = I_1. \tag{3}$$

Assume that M3 and M4 are perfectly matched (i.e., $K_{n3} = K_{n4}$ and $V_{\mathrm{Tn3}} = V_{\mathrm{Tn4}}$) and both of them are biased in saturation. According to the square-law characteristics of MOSFETs, the following are given [14]:

$$V_{GS3} = V_{GS4} = \sqrt{\frac{2I_1}{K_{n3}}} + V_{\mathrm{Tn3}}. \tag{4}$$

Since $V_{GS3} + V_{DS1} = V_{GS4} + V_{DS2}$, it leads to

$$V_{DS1} = V_{DS2}. \tag{5}$$

Because source voltages of M3 and M4 are equal, i.e., $V_{\mathrm{SB3}} = V_{\mathrm{SB4}}$, therefore the assumption that $V_{\mathrm{Tn3}} = V_{\mathrm{Tn4}}$ could be held. Substituting (1), (3), and (5) into (2) and assuming that M1 and M2 are perfectly matched (i.e., $K_{n1} = K_{n2} = K_n$ and $V_{\mathrm{Tn1}} = V_{\mathrm{Tn2}} = V_{\mathrm{Tn}}$), I_{in} is derived as

$$I_{\mathrm{in}} = K_n \cdot V_{G2} \cdot V_{DS2}. \tag{6}$$

From (6), a voltage-controlled resistor may be given and its equivalent resistance is given as

$$R_{\mathrm{eq}} = \frac{V_{DS2}}{I_{\mathrm{in}}} = \frac{1}{K_n V_{G2}}. \tag{7}$$

According to (7), the equivalent resistance is reversely proportional to the bias voltage V_{G2}.

Based on the proposed voltage-controlled resistor, the proposed current-mode divider is shown in Fig. 2. Assume that both M7 and M8 are biased in saturation, they can realize a current-to-voltage converter [15]. Assume that M7 and M8 are perfectly matched (i.e., $K_{p7} = K_{p8} = K_p$ and $V_{Tp7} = V_{Tp8} = V_{Tp}$) and both of them are embodied in individual wells to avoid the body effect. If the supply voltages $V_{\mathrm{DD}} = |V_{SS}|$, yields

$$V_{G2} = \frac{I_8 - I_7}{2K_p(V_{\mathrm{DD}} - |V_{Tp}|)} = \frac{I_D}{2K_p(V_{\mathrm{DD}} - |V_{Tp}|)}. \tag{8}$$

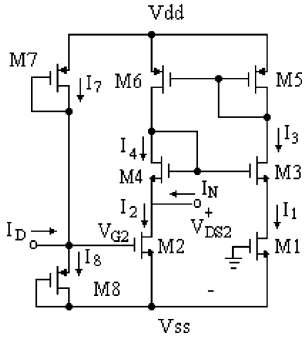

Fig. 2. Proposed current-mode divider.

Substituting (8) into (6) yields

$$V_{DS2} = \frac{2K_p(V_{\rm DD} - |V_{Tp}|)}{K_n} \cdot \frac{I_N}{I_D}. \tag{9}$$

According to (9), a current-mode divider would be realized. However, the output voltage of the proposed current-mode divider is influenced by the variation of the supply voltage. To keep the proposed current-mode divider work properly, M1 and M2 should be biased in the triode region and other transistors should be in saturation. Since the current I_N must flow into the drain of M2 therefore the gate voltage of M2 should be larger than the ground potential. According to (8), yields

$$I_D > 0. \tag{10}$$

Next, for M2 to operate in the triode region, the output range may be derived as

$$V_{DS2} < \frac{I_D}{2K_p(V_{\rm DD} - |V_{Tp}|)} - V_{\rm Tn2} \tag{11}$$

where K_p is the transconductance of M7 and M8 and $V_{\rm Tn2}$ is the threshold voltage of M2, respectively.

III. Applications

A. Pseudo-Exponential Function Generator

A pseudo-exponential function may be written as [16]

$$\exp(4x) \cong \left(\frac{1+x}{1-x}\right)^2 \quad ;\ \text{if } |x| \ll 1. \tag{12}$$

The proposed pseudo-exponential function generator is shown in Fig. 3 [17]. Assume that M9 and M10 are perfectly matched (i.e., $K_{p9} = K_{p10} = K_p$ and $V_{Tp9} = V_{Tp10} = V_{Tp}$) and both of M9 and M10 are biased in saturation. Based on the square-law characteristics of MOSFETs, the currents I_D and I_N are written as

$$I_D = I_9 = \frac{K_p}{2}(V_{\rm DD} - (V_b + V_{\rm in}) - |V_{Tp}|)^2 \tag{13}$$

and

$$I_N = I_{10} = \frac{K_p}{2}(V_{\rm DD} - (V_b - V_{\rm in}) - |V_{Tp}|)^2 \tag{14}$$

where V_b is the bias voltage. Assume that $V_b < 0$ and $V_{\rm DD} - V_b > |V_{Tp}|$. Substituting (13) and (14) into (9) yields

$$V_{DS2} = \frac{2K_p(V_{\rm DD} - |V_{Tp}|)}{K_n} \cdot \left(\frac{1 + \frac{V_{\rm in}}{V_{\rm DD} - V_b - |V_{Tp}|}}{1 - \frac{V_{\rm in}}{V_{\rm DD} - V_b - |V_{Tp}|}}\right)^2. \tag{15}$$

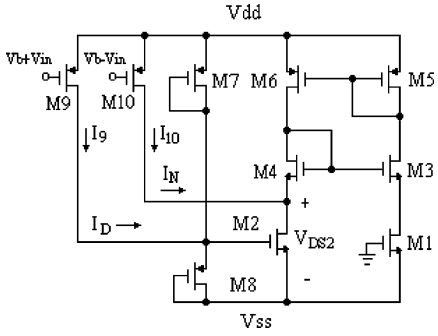

Fig. 3. Proposed pseudo-exponential function generator.

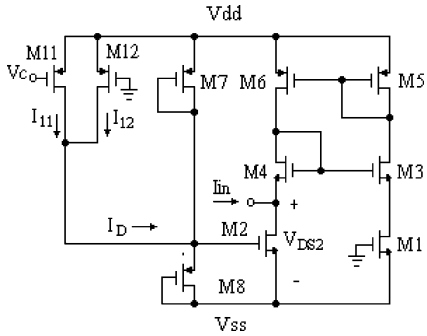

Fig. 4. Proposed variable transresistance amplifier.

Comparing (15) with (12), results in

$$V_{DS2} = b \cdot \left(\frac{1 + aV_{\rm in}}{1 - aV_{\rm in}}\right)^2 \cong b \cdot \exp(4aV_{\rm in}) \quad \text{if } |aV_{\rm in}| \ll 1 \tag{16}$$

where $a = 1/(V_{\rm DD} - V_b - |V_{Tp}|)$ and $b = 2(K_p/K_n)(V_{\rm DD} - |V_{Tp}|)$. According to (16), a pseudo-exponential function generator may be realized.

B. Variable Transresistance Amplifier

The proposed variable transresistance amplifier is shown in Fig. 4. M11 and M12 realized an exponential function generator [18]. Assume that M11 and M12 are biased in saturation and the transconductance parameters and the threshold voltages of M11 and M12 are equal (i.e., $K_{p11} = K_{p12} = K_p$ and $V_{Tp11} = V_{Tp12} = V_{Tp}$). According to the square-law characteristics of the MOSFETs, the currents I_{11} and I_{12} are given as [14]

$$I_{11} = \frac{K_p}{2}(V_{\rm DD} - V_c - |V_{Tp}|)^2 \tag{17}$$

$$I_{12} = \frac{K_p}{2}(V_{\rm DD} - |V_{Tp}|)^2. \tag{18}$$

According to the assumptions $|(a/b)x| \ll 1$ and $b^2 + (b + ax)^2 \cong \exp((a/b)x)$ [18], the current I_D is given as

$$\begin{aligned} I_D &= I_{11} + I_{12} \\ &= K_p(V_{\rm DD} - |V_{Tp}|)^2\left(\frac{{V_c}^2}{2(V_{\rm DD} - |V_{Tp}|)^2} - \frac{V_c}{(V_{\rm DD} - |V_{Tp}|)} + 1\right) \\ &\cong I_{b1} \cdot \exp(-a_1 V_c) \end{aligned} \tag{19}$$

where $I_{b1} = K_p(V_{\rm DD} - |V_{Tp}|)^2$, $a_1 = 1/(V_{\rm DD} - |V_{Tp}|)$ and V_c is a control voltage. Substituting (19) into (8) and let the current I_N be the input current $I_{\rm in}$ yields

$$V_{DS2} \cong \frac{2}{K_n(V_{\rm DD} - |V_{Tp}|)} I_{\rm in} \cdot \exp(a_1 V_c). \tag{20}$$

Therefore, a variable transresistance amplifier may be realized.

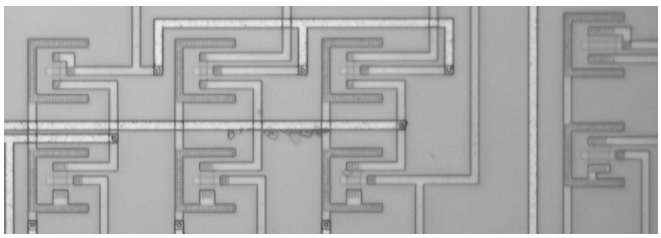

Fig. 5. Die photograph of the proposed current-mode divider.

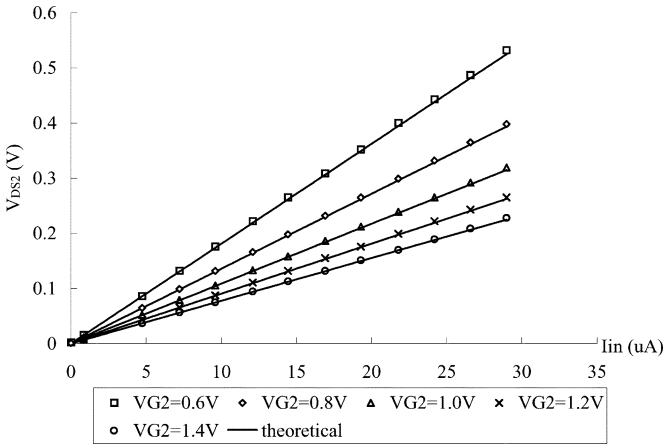

Fig. 6. Experimental results of the proposed voltage-controlled resistor.

IV. Experimental Results

All the proposed circuits have been fabricated in a 0.5-μm 2P2M N-well CMOS process. The die photograph of the current-mode divider is shown in Fig. 5. The threshold voltage for the NMOS is 0.78 V and that for the PMOS is -1.1 V in our process and the transconductance parameters in our process are $K_n = 2.02K_p = 0.186$ mA/V^2. All the experiments were performed with supply voltages $V_{\rm DD} = |V_{\rm ss}| = 1.5$ V.

Fig. 6 shows the experimental results of the proposed voltage-controlled resistor which were performed with the bias voltages $V_{G2} = 0.6$, 0.8, 1.0, 1.2, and 1.4 V, respectively. As the input current $I_{\rm in}$ varies from 0 $\sim$ 30 μA, the measured equivalent resistors are 18.44 kΩ (at $V_{G2} = 0.6$ V), 13.76 kΩ (at $V_{G2} =$ 0.8 V), 10.87 kΩ (at $V_{G2} = 1.0$ V), 9.22 kΩ (at $V_{G2} = 1.2$ V) and 7.85 kΩ (at $V_{G2} = 1.4$ V), respectively, which is consistent with the theoretical analysis calculated by (7).

The experimental results of the proposed current-mode divider are shown in Fig. 7(a) and (b) which have been performed with $I_D =$, 40, 50, 70, and 80 μA while I_N varies from 0 $\sim$ 30 μA and $I_N =$ 10, 15, 20, 25, and 30 μA while I_D varies from 1 $\sim$ 70 μA, respectively. The measured output offset voltage is less than 1.5 mV under all situations and the measured maximum linear error is less than 0.85%. The measured total harmonic distortion (THD) at 100 kHz of the output voltage for $I_D = 30$ μA and the amplitude of the current I_N is 0.1, 0.5, and 1 μA are 0.03%, 0.122%, and 0.243%, respectively. Also, the measured power consumption is less than 0.22 mW (at $I_D = I_N = 30$ μA). For the proposed current-mode divider to work properly, the current I_D must be limited by (10) and (11). As the current I_D was increased to 86 μA, the corresponding output deviated from its theoretical value [calculated by (9)] by

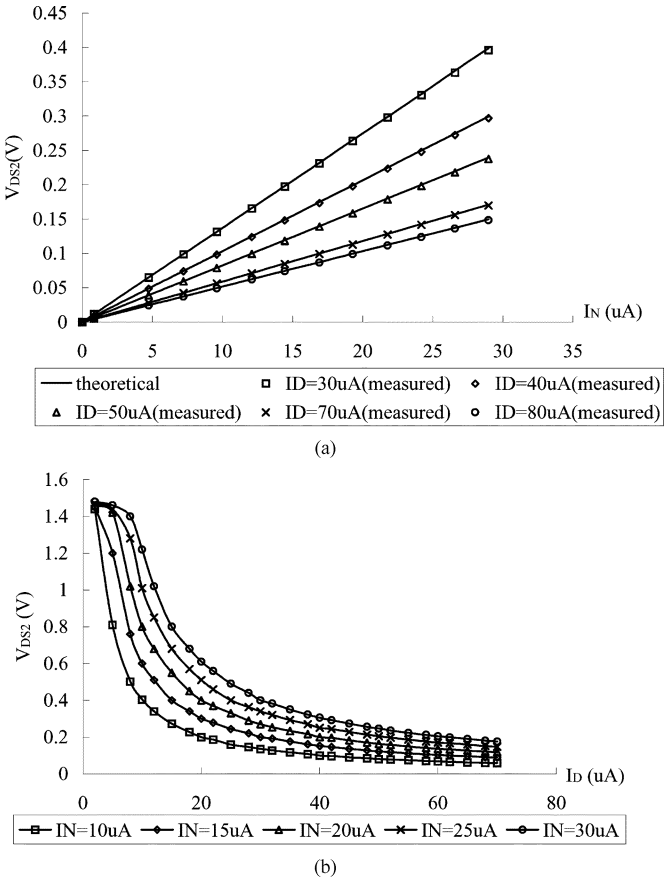

Fig. 7. Experimental results of the current-mode divider (a) V_{DS2} vs. I_N (b) V_{DS2} vs. I_D.

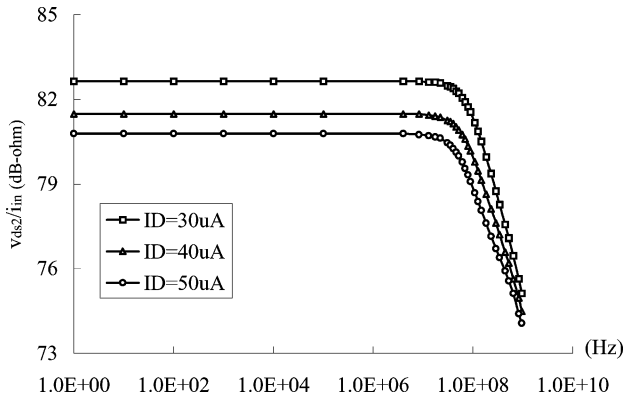

Fig. 8. Frequency response of the proposed current-mode divider.

2.78% (at $I_N = 30$ μA). The experimental results are consistent with the theoretical analysis calculated by (9). For measuring the power-supply rejection ratio (PSRR), assume that a ripple was generated along with the supply voltage $V_{\rm DD}$. If the magnitude of the ripple is 10% of the $V_{\rm DD}$ and the frequency is 100 kHz, the measured PSRR is about 26.67 dB. The frequency response of Fig. 2 is shown in Fig. 8 which was performed with the current $I_D =$30, 40, and 50 μA while the current $I_N = 20$ μA and the small-signal current was set to 1% of the current I_N. The corresponding $-$3-dB bandwidth are 231, 191, and 179 MHz, respectively. Also, the measured input referred noise (at 100 kHz) is 1.49 $\times 10^{-8}$ A/$\sqrt{\rm Hz}$.

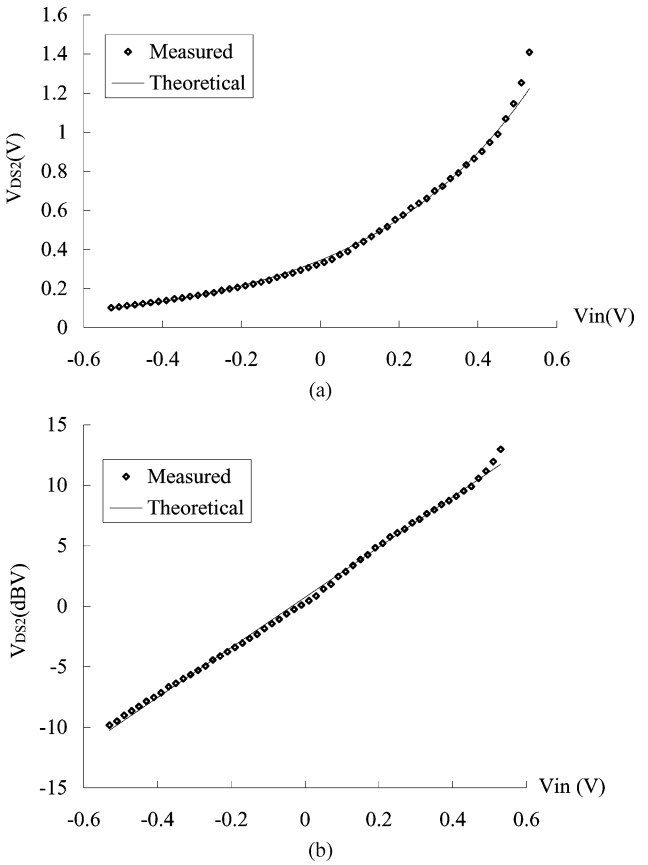

Fig. 9. Experimental results of the proposed pseudo-exponential function generator. (a) Linear scale. (b) Semi-logarithmic (dB) scale.

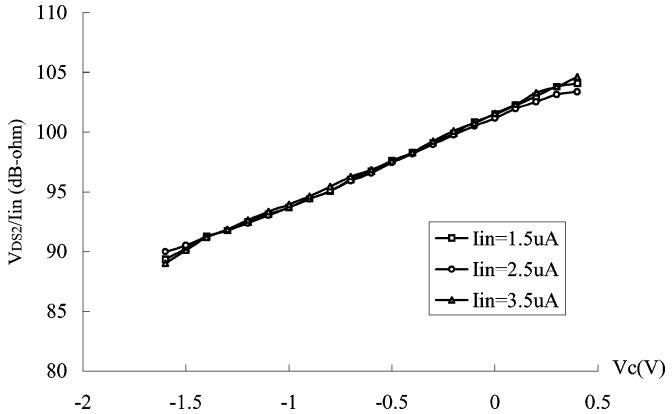

Fig. 10. Experimental results of the proposed variable transresistance amplifier.

The experimental results of the proposed pseudo-exponential function generator are shown in Fig. 9(a) and (b), respectively. With the bias voltage $V_b = -0.4$ V, as $V_{\rm in}$ varies from -0.5 to 0.5 V, the output operating range could be more than 20 dB while the linearity error is less than ± 0.5 dB. The experimental results confirm the theoretical analysis calculated by (16).

Fig. 10 shows the experimental results of the proposed variable transresistance amplifier. The experiments were performed with the input currents $I_{\rm in} = 1.5$, 2.5, and 3.5 μA, respectively. As the control voltage V_c varies from -1.6 to 0.4 V, the transresistance ranges from 90 to 102 dBΩ while the linearity error is less than ± 1 dB. The experimental results verify the theoretical analysis calculated by (20). As a comparison, two different samples were tested using the same procedure, with very similar results.

V. Conclusion

In this brief, a new CMOS current-mode divider is developed. Experimental results have been given to confirm the validity of the theoretical analysis. The proposed current-mode divider can be used to realize a voltage-controlled resistor, a pseudo-exponential function generator and a variable transresistance amplifier.

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