Magnetic-field-to-digital converter using PWM and TDC techniques

C.-H. Kuo, S.-L. Chen and S.-I. Liu

Abstract: A high resolution magnetic-field-to-digital converter (MDC) is presented. It is composed of a magnetic-field-to-pulse width converter (MPC), a cyclic pulse-shrinking time-to-digital converter (TDC) and a polarity detector. This prototype circuit has been fabricated in a 0.5 μm CMOS DPDM process. With a clock rate of 16.6 kHz, the power consumption is 42.5 mW under 5 V supply voltage. The equivalent resolution less than 16 μT can be achieved within the range of ±10 mT. After off-line calibration, the remaining offset is 0.017 mT and its gain error is smaller than 0.4%.

1 Introduction

The magnetic transducer has found many applications in modern communications and industry [1–4]. There is a trend to integrate the magnetically sensing system with digital processor circuits into single chips for low cost, high reliability and on-chip processing capability. Sensor signal conditioners can provide many kinds of output, such as voltage, current, frequency, pulse width, duty-cycle period. Digital outputs can offer more robust data transmission against noise and interference [4]. Although some techniques using Hall sensors have proved beneficial for good sensitivity and linearity, the MAGFET-based sensor systems have difficulty reaching resolution smaller than 100 μT [5, 6].

To convert an analogue signal into a digital one, one of the most promising solutions is to use pulse width modulation (PWM) techniques [7]. PWM signals can convert the voltage/current signal into the pulse width in the time domain. The signal processing in the time domain can avoid the dynamic range reduction caused by low supply voltages. In this work, the resolution of the magnetic-field-to-digital converter (MDC) is improved by using a time-to-digital converter (TDC). Moreover, the digital output will make the digital signal processing more robust against noise and interference. In addition, the polarity of the applied magnetic field could be achieved by a simple polarity detector.

Based on the PWM and time-to-digital conversion techniques, a CMOS MDC is presented in this paper. This paper is organised as follows: in Section 2, the architecture of the proposed MDC is discussed. The building blocks in this MDC will be described. In Section 3, an off-line calibration method is introduced to compensate offset and gain errors of the proposed circuit. In Section 4, the experimental results are shown. Finally, conclusions are given in Section 5.

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2 Circuit description

The block diagram of the proposed MDC is shown in Fig. 1. It consists of a magnetic-field-to-pulse converter (MPC), a cyclic time-to-digital converter (TDC), and a polarity detector, which can indicate the direction of the magnetic field applied to the chip perpendicularly. The MPC transforms the magnetic field to its corresponding width of the pulse. Then, the modulated pulse could be digitised by the high resolution TDC and a ripple counter. The detailed circuit implementations are discussed as follows.

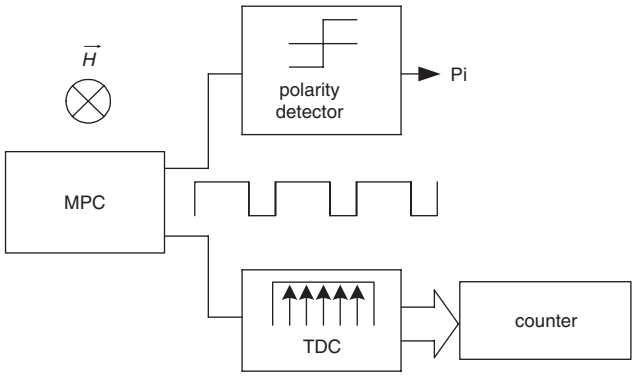

Fig. 1 *Proposed magnetic-field-to-digital converter*

2.1 Magnetic operational amplifier (MOP)

The magnetic operational amplifier (MOP), which is similar to that mentioned in [8, 9], with the switched-capacitor common mode feedback (CMFB) circuit is shown in Fig. 2. The MAGFET arrays are merged with an operational amplifier to sense the external magnetic field. According to [9], the *n*-channel concave MAGFET device with the aspect ratio $W/L = 80\,\mu m/40\,\mu m$ and $d = 2\,\mu m$ is chosen as the sensing element to take the layout mismatch problem and optimal sensitivity into account simultaneously. When a magnetic field is applied, there will be a current imbalance between two drains of the MAGFET. The voltage difference between the differential outputs, V_{out+} and V_{out-},

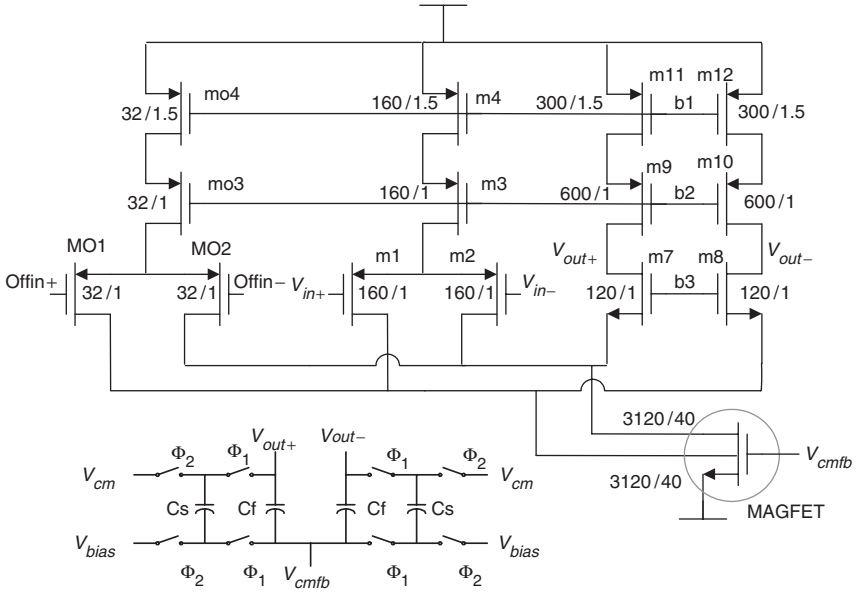

Fig. 2 *Fully differential MOP with CMFB circuit*

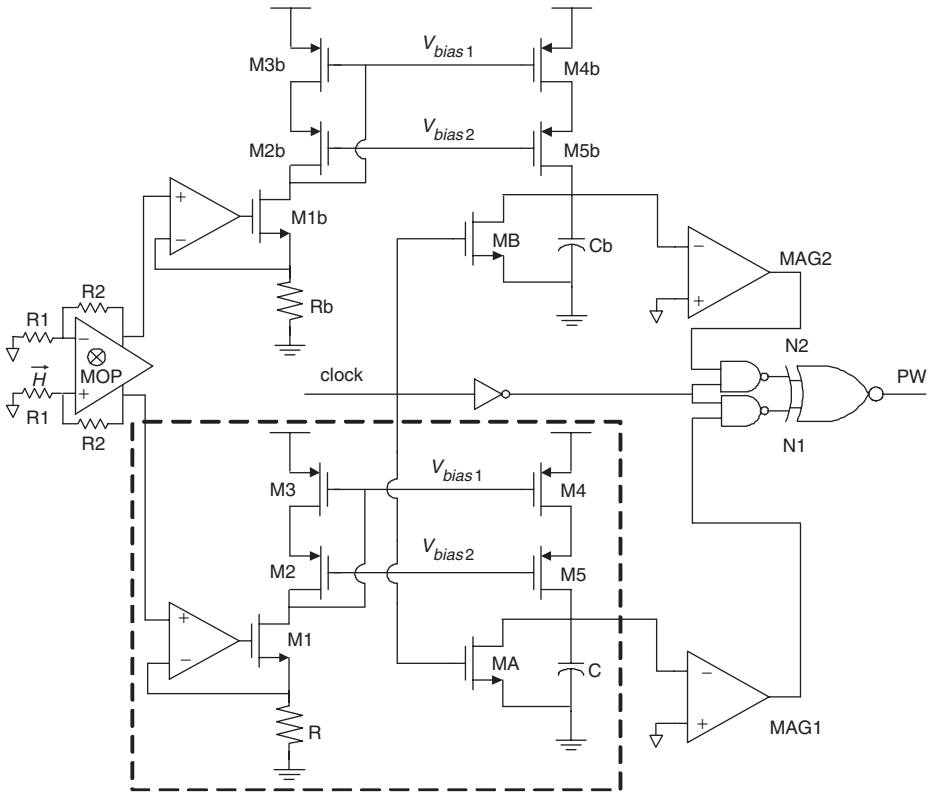

Fig. 3 *Magnetic-to-pulse converter*

of the operational amplifier will be generated. The output voltage difference of the MOP can be expressed as

$$V_{out+} - V_{out-} = A_V \cdot (V_{in+} - V_{in-} + S_m \cdot H_\perp) \qquad (1)$$

where A_V is the open-loop gain of this operational amplifier and $H_\perp$ is the applied magnetic field that is perpendicular to the chip, and S_m denotes the conversion gain from the magnetic field to the induced voltage. The linearity and sensitivity can be improved by connecting the MOP into an inverting amplifier.

2.2 Magnetic-field-to-pulse converter

A differential version of the magnetic-field-to-pulse converter is shown in Fig. 3, and the timing diagrams of the corresponding signals are shown in Fig. 4. It is composed of an amplifier stage and two saw-tooth generators followed by digital circuits to extract the modulated pulses.

In the saw-tooth generator, as shown by the dashed line in Fig. 3, the conventional operational amplifier (OP) and the transistor M1 together with the resistor R realise a constant current source, which is generated by the output voltage of the MOP. Hence, the whole magnetically controlled current can be obtained by

$$I + \Delta i = I + \frac{r \cdot S_m \cdot H_\perp}{R} \qquad (2)$$

where I is the bias current when no magnetic field is applied, and $r(\equiv 1 + R_2/R_1)$ denotes the closed-loop gain of the

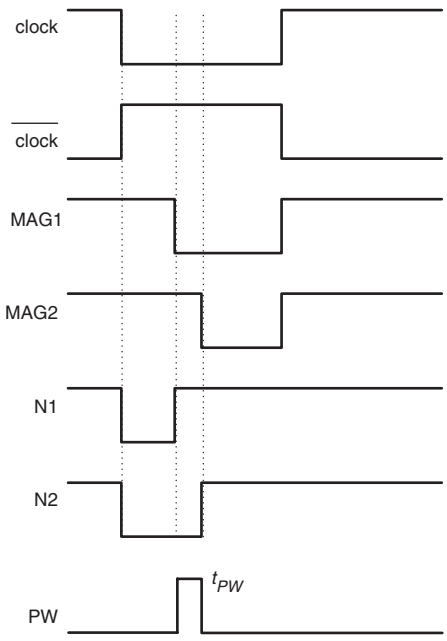

Fig. 4 *Timing diagrams of signals in Fig. 3*

amplifier. The total current would be mirrored by a wide-swing cascade structure [10], composed of M2–M5. It will charge the capacitor C while the transistor MA is off. In other words, when clock is high, the output N1 of the NAND gate is reserved to 'high'. Alternatively, when the transistor MA is turned on, the charge stored on the capacitor is set to zero. When clock goes low, N1 is forced to 'low' and the transistor MA is turned off, hence, the current starts to charge the capacitor through M3 and M4. Once the voltage stored on the capacitor is larger than the reference voltage, V_{ref}, the comparator changes its output state, MAG1, and retrieves N1 to 'high'. The resulting time slot of N1 in the 'low' state is dependent on capacitor size, clock rate, and the charging current, which is a function of the magnetic field applied. In general, the charging and discharging to the output capacitance are performed by the PMOS and NMOS sensing currents, respectively. However, the mismatch between PMOS and NMOS sensing currents would be excluded since only charging behaviour is needed in the proposed magnetic to pulse converter. The mismatch between upper and lower MPC paths could be minimised by routing the layout carefully. Moreover, the time-to-digital converter followed the digital filter by the counter will average the noises.

When no magnetic field is applied, the outputs of the MOP would result in the same pulse width at the outputs of two comparators, theoretically. Thus, there is no pulse at the output, PW, of the XOR gate. When the magnetic field is applied, the differential outputs of the MOP would excite different currents into current mirrors. The modulated pulse could be therefore triggered by means of the subsequent XOR gate. This pulse width difference, which is proportional to the magnetic field, can be derived as follows.

$$t_{PW} = T_{N2} - T_{N1} = \frac{C \cdot V_{ref}}{I - \Delta i} - \frac{C \cdot V_{ref}}{I + \Delta i}$$

$$= \frac{2 \cdot C \cdot V_{ref}}{I^2 - \Delta i^2} \times \Delta i \approx \frac{2 \cdot C \cdot V_{ref}}{I^2} \times \frac{r \cdot S_m \cdot H_\perp}{R} \quad (3)$$

where T_{N2} and T_{N1} denote the time slots of the outputs, N2 and N1, in 'low' state, respectively. It should be noted that the pulse width is proportional to the applied magnetic field if the induced current is small enough compared to the bias current, $\Delta i \ll I$. In other words, as the magnitude of the magnetic filed is getting large, the term Δi^2 would cause the nonlinearity of the converter.

It should be noted that the resulting pulse width is dependent on the charging current. The charging current has to be kept large to guarantee the linear transformation from magnetic field to pulse width. This requirement can be relaxed by speeding up the clock frequency. However, the narrower the pulse width, the higher the resolution of the subsequent TDC required. There is a tradeoff between the linearity and the resolution.

2.3 Cyclic pulse shrinking time-to-digital converter [11]

The pulse width generated from the MPC is too small to extract the corresponding count value for a general counter. A high resolution cyclic pulse shrinking TDC, as shown in Fig. 5, is utilised to get an equivalent count according to different pulse widths. After a couple of cycles, the pulse width would become narrower or even sharp, causing the pulse level beneath the threshold voltage to stop counting.

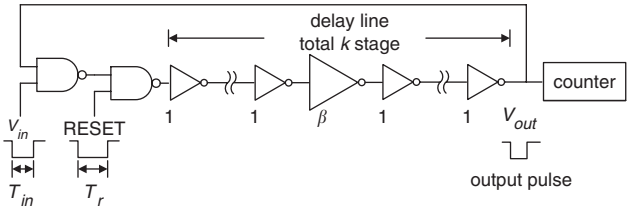

Fig. 5 *Cyclic pulse shrinking time-to-digital converter*

This TDC is composed of two NAND gates, a counter and a delay line which has k inverters. Suppose that all the inverters have the same dimension except one inverter whose width is β times of others. The inhomogeneous dimension between the specific inverter gate, served as a pulse shrinking element, and the other of each two NOT gates, served as a delay buffer, makes the pulse undergo different rising and falling time at the interfaces of them. When a pulse passed this delay line once, the total shrinking amount ΔW can be expressed as [11]

$$\Delta W \propto \left(\beta - \frac{1}{\beta}\right) \cdot C_1 \cdot \left(\frac{1}{K_p} - \frac{1}{K_n}\right) \quad (4)$$

where K_p and K_n are transconductance parameters of PMOS and NMOS in the unit inverter, respectively and C_I denotes the effective input capacitor of the unit inverter. The pulse will be is shrunk cyclically until it vanishes thoroughly. There is a tradeoff between resolution and the bit number of the counter. The smaller the pulse shrinking, the better the resolution, however, the more inverters are required. Here $\beta = 2$ is chosen for compromising these characteristics.

2.4 Polarity detector

The polarity detector is used to detect the direction of the external magnetic field applied, as shown in Fig. 6. Its timing sequence of the corresponding signals is plotted in Fig. 7. When CLK is low, the differential outputs of the MPC compare with the common mode voltage to distinguish which one of the differential paths has greater net magnetic field in the duration of the pulse. It is clearly that only one output of the D flip-flops will go to high, and the direction of magnetic field can be hence determined.

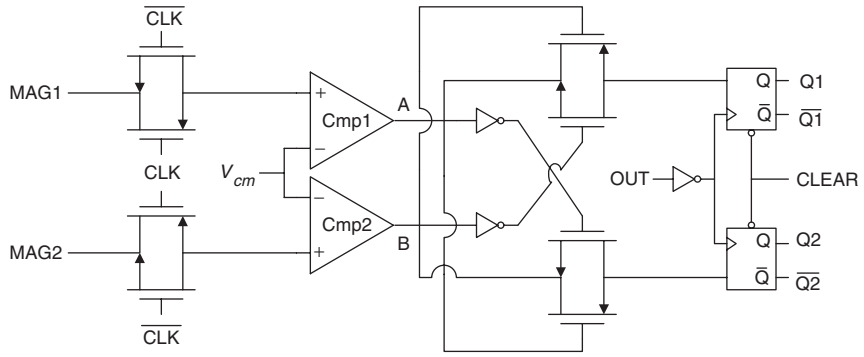

Fig. 6 *Polarity detector*

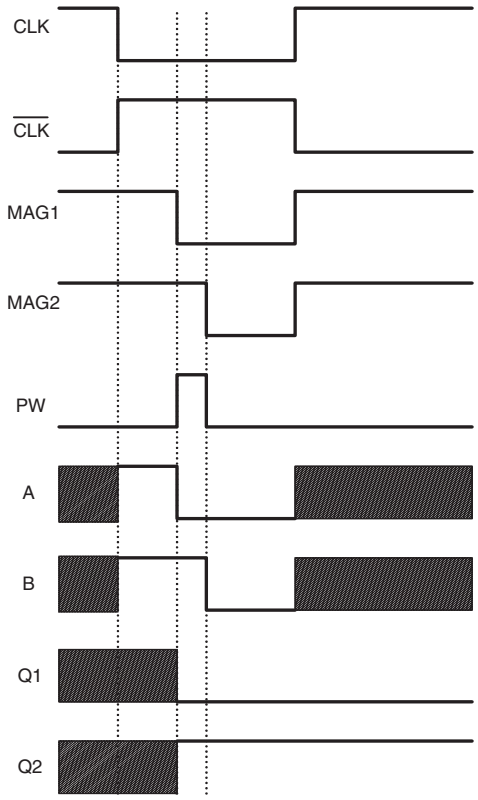

Fig. 7 *Timing diagram of Fig. 6*

3 Calibration

There are three main factors to limit the accuracy and resolution of the MDC. The first one is the mismatch between the differential paths in the MPC. Carefully sizing and layout of the devices can relax this problem. Second, the nonlinearity caused by the term Δi^2 in (3) detracts the accuracy of the pulse width. It can also be minimised by moderately increasing the bias current. The last one is the system offset caused by the time offset in this TDC. It should be noted that there is also an offset voltage in the MAGFET, and it can be trimmed by adjusting the offset voltage of the MOP. The following off-line calibration method can be adapted to eliminate the offset [12].

Applying two magnetic field H_{ref} and $H_{ref}/2$ into the system as the references, the corresponding pulse width T_{ref} and $T_{ref}/2$ would be generated at the MPC output, and the related codes N and N', respectively, could be read in the subsequent counter. The equivalent offset magnetic field, H_{offset}, in this system can be expressed as

$$H_{offset} = \frac{H_{ref} \cdot (N - 2N')}{2(N - N')} \tag{5}$$

Moreover, the effective resolution can be calculated as

$$\alpha = \frac{H_{ref}}{2(N - N')} \tag{6}$$

Note that little drift on parameters α and H_{offset} is assumed during successive measurements. Therefore, when an unknown magnetic field H_{in} is applied and the measured count value is n. Their relation can be calculated as

$$H_{in} = \frac{H_{ref} \cdot (n + N - 2N')}{2(N - N')} \tag{7}$$

In fact, the rising and falling edge of the pulses in the delay line of a TDC are exponential functions of time, the offset is more complicated than the discussion above. However, (7) would be precise enough for an estimated result.

4 Experimental results

The proposed MDC has been fabricated in a 0.5 μm CMOS technology. With a clock rate of 16.6 kHz, the power consumption is 42.5 mW under 5 V supply voltage. Its die photograph is shown in Fig. 8 and the area without pads is 1.9×2 mm. The maximum range of the detectable magnetic field is limited by the delay line in the TDC. In this TDC, two NAND gates and 344 inverters are chosen to realise this delay line to detect the magnetic field of 10 mT.

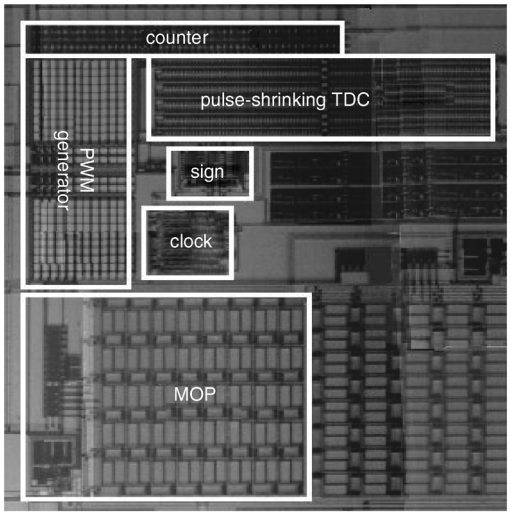

Fig. 8 *Photograph of proposed magnetic-to-digital converter*

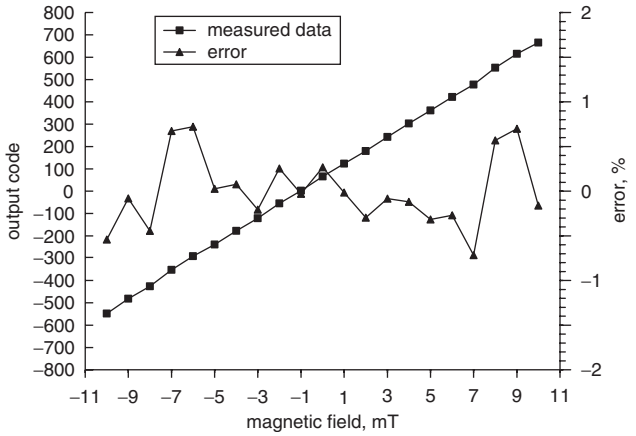

Fig. 9 *Measured results within ±10 mT*

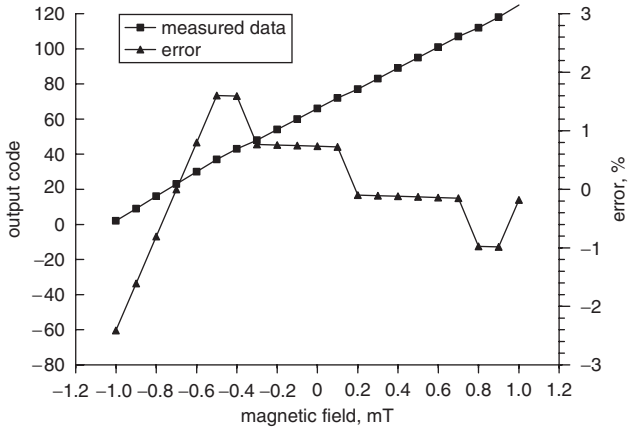

Fig. 10 *Measured results in range of ±1 mT*

The measured results are shown in Figs. 9–11. Each measured datapoint is obtained by averaging five measurements. The coarse measurement result is plotted in Fig. 9 where the range is within ±10 mT, and the magnitude increment is 1 mT. From this figure, the linear response owing to the magnetic field can be obtained. The calculated sensitivity is 60.4 code/mT. The measured result exhibits 16% degradation in sensitivity compared to the simulation one. The resolution test is shown in Fig. 10. The linearity is also maintained in this range of ±1 mT with 0.1 mT increment. From this figure, the nonlinearity is slightly

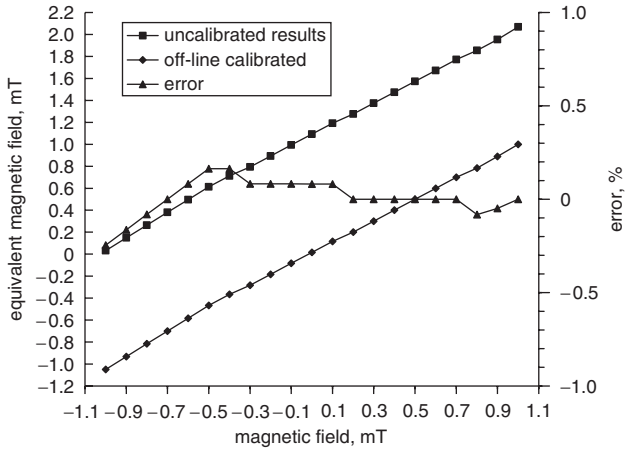

Fig. 11 *Equivalent magnetic field for uncalibrated and calibrated results in range ±1 mT*

Table 1: Performance comparison of uncalibrated, calibrated, and ideal conditions

	Ideal curve	Uncalibrated	Calibrated
Offset	0	1.093 mT	0.017 mT
Slope	1	0.915	1.004
Gain error	0	8.54%	0.4%

worse. This is because the smaller magnetic field produces a smaller width of the pulse, which is easily affected by noise. The measured result has an offset owing to the mismatch between upper and lower paths of the differential MPC. Since only the d.c. magnetic field signal is of concern and tested, the minimum detectable magnetic field of the proposed circuit is limited by $1/f$ noise rather than thermal noise.

Figure 11 shows the equivalent magnetic field that the output digital code is converted into. It shows the results without calibration, off-line calibration, and ideal cases within ±1 mT. The offset code is 66, which is equivalent to an offset magnetic field of 1.093 mT. After off-line calibration, the offset can be reduced to 0.017 mT, the gain error can be reduced to 0.4%. Table 1 gives the comparison of the performance for uncalibrated and calibrated measured results. Table 2 gives the performance summary with other BiCMOS/CMOS magnetic sensors.

Table 2: Comparisons with other BiCMOS/CMOS magnetic sensors

Study	[5]	[3]	[13]	[13]	[14]	[15]	[15]	This work
Technology	CMOS 0.7 μm	CMOS 0.8 μm	CMOS 0.5 μm	CMOS 0.5 μm	BiCMOS	CMOS 0.5 μm	CMOS 0.5 μm	CMOS 0.5 μm
Sensing device	MAGFET	Spinning current Hall device	MAGFET	MAGFET	Hall plate	MAGFET	MAGFET	MAGFET
Range	0–800 mT	±200 mT	±100 mT	±100 mT	±80 mT	±100 mT	±100 mT	±10 mT
System offset	1.6 mT	—	1 mT	1 mT	—	0.6 mT	0.4 mT	0.017 mT
Resolution	12.5 mT	100 μT	100 μT	100 μT	1 mT	50 μT	50 μT	16 μT
Area (mm^2)	—	—	1.87	0.888	—	1.9305	1.1592	3
Power	—	—	32.4 mW	32.4 mW	—	28.58 mW	20.73 mW	42.5 mW
Nonlinearity		—	<3%	<3%	—	<1.12%	<1.3%	<0.4%

5 Conclusions

A magnetic-field-to-digital converter is presented with the usage of PWM signals and cyclic pulse shrinking TDC to achieve high resolution. An off-line mathematical method can be further used to reduce the gain error and inherent offset dramatically, say 0.4% and 17 μT, respectively. Compared with published work with digital outputs by using MAGFETs, it exhibits a finest resolution of 16 μT.

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