行政院國家科學委員會專題研究計畫　成果報告

40Gb/s CMOS 光纖通訊收發系統

計畫類別：個別型計畫
計畫編號：NSC93-2213-E-002-109-
執行期間：93 年 08 月 01 日至 94 年 07 月 31 日
執行單位：國立臺灣大學電子工程學研究所

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報告類型：精簡報告
報告附件：出席國際會議研究心得報告及發表論文
處理方式：本計畫可公開查詢

中　華　民　國 94 年 10 月 18 日

40Gb/s CMOS 光纖通訊收發系統

A 40 Gb/s CMOS Transceiver Chipset for Optical Communication Systems

計畫編號：NSC 93-2213-E-002-109-
執行期限：93 年 08 月 01 日至 94 年 07 月 31 日
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中文摘要

本計畫使用先進之CMOS 製程發展下一代(40-Gb/s)光纖通訊系統 －SONET 標準之OC-768/STM-256 規格，拓展CMOS 製程在超高速及寬頻電路領域之應用。此光纖通訊收發器採用先進之系統組織與電路架構，並包含以下之獨立單元：40-Gb/s 四對一多工器、雷射驅動器、40-GHz 頻率合成器、40-Gb/s 轉阻放大器/等化器及 40-Gb/s 之時脈資料還原器(具自動解多工功能)。本計畫預定使用0.13-Mm 之CMOS 製程，將針對深次微米製程之雜訊、速度、及低電壓等特性因素對類比電路之影響，作廣泛而深入的研究。所提出之新的電路結構，將改善許多類比及混合電路之設計問題。

本計畫執行期限為三年，預期成果包括：(1)各獨立單元之設計、模擬、佈局、晶片製作及測試；(2)毫米波電路元件之應用與系統最佳化；(3)系統整合與測試。本計畫提供研究人員寬頻及超高速電路之設計訓練，並創造前瞻性之研發成果。

關鍵詞：光纖通訊、SONET、收發器、多工器、鎖相迴路、頻率合成器、轉阻放大器、時脈資料還原器、等化器

英文摘要

This project utilizes the advanced CMOS process to develop a 40-Gb/s transceiver for OC-768/STM-256 standard in synchronous optical networks (SONET), exploiting the territory of ultra high-speed and broadband circuits. Employing new architectures and circuit topologies, the transceiver consists of a 40-Gb/s 4-to-1 MUX and laser driver, a 40-GHz PLL-based frequency synthesizer, a 40-Gb/s TIA/preamplifier/equalizer, and a 40-Gb/s quarter-rate CDR which automatically retimes and demultiplexes the full-rate data into parallel channels. To be fabricated in 0.13-Mm CMOS technology, the fully integrated transceiver provides solutions to issues such as noise, speed, and voltage headroom in deep sub-micron CMOS process and contributes to numerous analog and mixed-signal designs. The duration of this project is three years and the deliverables include: (1) design, simulation, fabrication, and testing of individual building blocks (i.e., MUX, laser driver, frequency synthesizer, TIA, preamplifier, equalizer, and CDR); (2) mm-wave application and system optimization; (3) system integration, testing, and optimization. This project provides training in broadband and ultra high-speed circuit design for researchers and students, creating promising and profitable results for next generation's optical communication system.

Keywords: optical communication, SONET, transceiver, MUX, PLL, frequency synthesizer, TIA, limiting amplifier, CDR, equalizer

一、緣由與目的

The rapidly growing volume of data transmission over the internet has rekindled interest in high-speed optical and electronic devices and systems, demanding greater bandwidth for serial-data communication networks. Next generation's optical communication systems and circuits have been implemented in SiGe or GaAs technology [1]~[7], but they require high voltage supplies and draw a few watts of power. On the other hand, recent integration of 10-Gb/s serializers and deserializers in CMOS technology [8] [9] encourages further research on high-speed and low-power CMOS solutions. Enormous research and techniques have been investigated on individual sub-circuits such as clock and data recovery (CDR) [10], limiting amplifier (LA) [11], transimpedance amplifier (TIA), multiplexer/demultiplexer (MUX/DMUX) [12] and phase-locked loop (PLL), providing a solid foundation for future optical communication systems operating at tens of gigabit.

It is well known that optical fibers provide a tremendous transmission capability, the distortion as signal travels through the fiber leads to closure of the data eye. To overcome this issue caused by fiber loss and dispersion, the signal needs to be regenerated and retransmitted by a transceiver after a few tens of miles. Currently, the optical pulses are first converted into electric current, regenerated and processed in the electric domain and converted back into the optical pulses. Since this optical/electrical interface determines the maximum data transmission rate, extensive research has been performed on low-cost, lower-power, high-speed and high performance realization of such transceivers.

This project utilizes the advanced CMOS process to fulfill a 40-Gb/s transceiver for OC-768 standard in synchronous optical networks (SONET) [13], exploiting the territory thus far claimed by GaAs and InP devices. Greater levels of integration and circuit/architecture co-design are to replace the conventional modular, generalpurpose building blocks to achieve higher performance. The new architectures, circuit topologies, and broadband techniques created here can be easily adopted in other pioneer area such as 60 GHz RF systems, and solutions to issues such as noise, speed, voltage headroom in deep sub-micron CMOS technology can be contributed to numerous analog/mixed-signal designs.

二、系統架構

Figure 1 shows the proposed generic optical communication system consisting of three components: (1) the transmitter (TX), which serializes the input data and converts it to optical form; (2) a fiber, which carries the light produces by the laser; and (3) the receiver (RX), which senses the light at the end of the fiber and converts it back to an electrical signal. In this project, the fully integrated transceiver is planned to be designed and fabricated in 0.13-Mm CMOS technology.

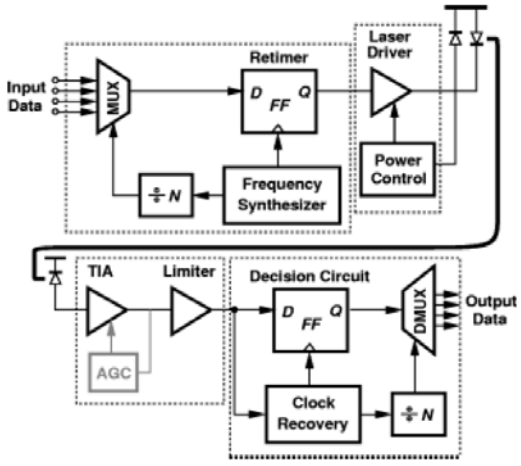


Figure 1: Generic transceiver architecture.

The transmitter multiplexes a number of channels into high-speed data stream, retiming and applying it to a laser driver. To achieve a data rate of 40 Gb/s, the MUX must incorporate inductive-peaking and transmission-line codesign and merge the retimer if necessary. A frequency synthesizer provides the required full-rate and divided clocks to different stages of MUX tree (and the retimer). Since the jitter of the transmitted data is primarily determined by that of the frequency synthesizer, it is essential to build a robust, low-noise PLL with high supply and substrate rejection. As shown in Fig. 2, modern high-speed PLLs typically consist of a phase/frequency detector (PFD), a charge pump, a loop filter, a voltage-controlled oscillator (VCO), and a chain of frequency divider. To provide the 40-GHz full-rate clock, an LC-tank VCO is incorporated to overcome difficulties in tuning range, phase noise, and output amplitude. The high-speed frequency divider presents some other design challenges in CMOS technology. Conventional static dividers can hardly achieve an operation frequency beyond 20 GHz, necessitating the exploitation of dynamic (Miller) dividers.

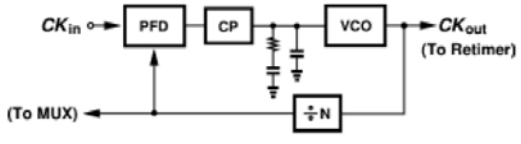


Figure 2: PLL-based frequency synthesizer.

三、設計與製作方法

The laser driver converts the digital data into current pulses that cause the optical emitter device to generate light. Since the large drive capability imposed on the laser driver necessitates the use of large input devices, the capacitance introduced by these devices is substantially large and may require a pre-driver stage with moderate gain. The light is fed into a fiber cable and propagated through a long distance before being received by the receiver.

In the receiver part, a photodiode captures the incoming optical signals and performs the optical/electrical conversion. This current is amplified by a low-noise TIA, yielding a voltage output to the limiting amplifier. The limiting amplifier enlarges the signal to logic level (at least hundreds of millivolts), and a CDR circuit extracts the timing information and cleans up the data. Since TIA and limiting amplifier deal with weak input signals of 40 Gb/s, conventional circuit topologies suffer from severe tradeoffs between bandwidth, gain, noise, device mismatch, and voltage headroom. Thus, the receiver may employ an equalizer to correct the dispersion introduced by the fiber. The use of optical amplifiers along the fiber link also eliminates the need of a high-gain limiting amplifier, relaxing the stringent gainbandwidth requirement in the receiver front-end. A preamplifier with moderate gain of 15 dB is placed between TIA and equalizer to provide sufficient bandwidth and linear phase response and suppress the noise contributed by the subsequent circuits. A bandwidth of around 26 to 28 GHz corresponding to 2/3 of the data rate is required and a transmission-line based distributed amplifier (DA) is a good candidate.

However, traditional cascaded and matrix DAs suffer from large coupling capacitor and significant signal loss. As shown in Fig. 3(a), a novel double-resonance technique

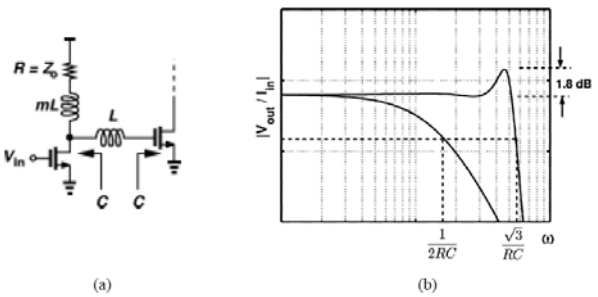


Figure 3: (a) Double-resonant amplifier, (b) the transfer response.

introduces an inductor between stages and improves the bandwidth by a factor of 3.5.

Figure 3(b) compares the transfer response of the double-resonant amplifier with that of the cascaded case. The design of ultra high-speed clock and data recovery circuit also poses difficult challenges and raise interesting research topics. The clock and data recovery circuit extracts the timing information and cleans it up by placing the recovered clock edges right in the middle of the data eye, producing an optimum sampling and improving the SNR of the receiver. However, conventional full-rate architectures [Fig. 4(a)] face severe speed and precision penalties in such a high data rate. It is mainly because the CMOS devices require a much higher swing to steer a given current than its bipolar counterparts, and a bipolar transistor having the same f_T allows much faster operation.

Since broadband data is much more difficult to amplify than are narrowband clocks, it is preferable to relax the data path design in exchange for more stringent clock generation. As shown in Fig. 4(b), a half-rate or quarter-rate CDR circuit inherently retimes and demultiplexes the data, obviating full-rate flipflops and frequency dividers. The sensitivity of the clock phase margin (jitter tolerance) to oscillator phase mismatches can be alleviated through the use of large devices and careful layout.

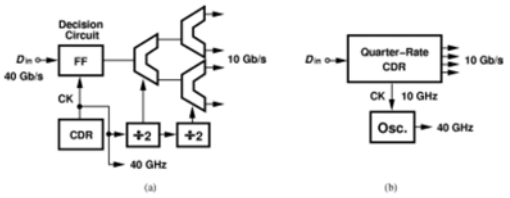


Figure 4: (a) Full-rate, (b) sub-rate deserializer.

In this project, we employ a quarter-rate CDR architecture to relax the issues described above. The circuit incorporates a multiphase VCO, a quarter-rate phase detector, a voltage-to-current (V/I) converter, and a simple loop filter. The PD uses the half-quarter phases provided by the VCO to sample the input data every 12.5 ps, thereby detecting data edges and determining whether the clock is early or late. Four of these samples fall in the center of the data eye, retiming and demultiplexing the 40-Gb/s input into four 10-Gb/s outputs. In the absence of data transitions, the V/I converter generates no output current, leaving the oscillator control line undisturbed. The circuit is fully differential, except for the oscillator control line. Other possible difficulties include (1) optimization of system integration, where the signal/noise coupling and long routing may degrade the performance; (2) analog/digital circuit isolation; (3) low supply-voltage design, where numbers of traditional circuit topologies may no longer be useful; (4) acquisition of testing equipments at this frequency; (5) expense on or availability of 0.13-Mm process. System-level simulation and noise-model estimation can provide an intensive understanding about system integration and the coupling effect. Further researches and studies will be performed on state-of-the-art system-on-a-chip (SoC) architectures so as to minimize the inter-block interference. In addition, previous experience on high-speed circuit designs provides extensive circuit topologies for low-supply

operation. Finally, rental program and academia-industry corporation could provide a solution for the costly expenses on testing equipments and tapeout. The circuit simulations, analysis, and design will be performed on workstations and PCs with the software provided by CIC.

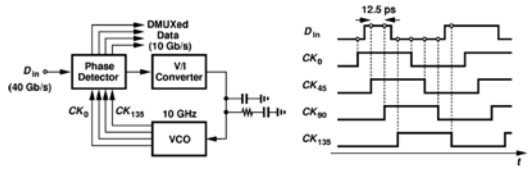
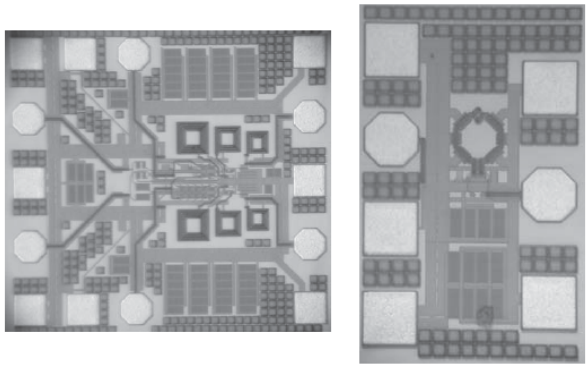


Figure 5: Quarter-rate CDR architecture.

四、模擬結果

The MUX and VCO circuits have been designed and fabricated in 0.18-μm CMOS technology. Figure 6 shows the die photos, which measure 0.7 × 0.7 mm2 and 0.3 × 0.45 mm2, respectively, including pads. The on-chip high-speed lines are designed as 50-Ω microstrip lines to absorb the routing capacitance. Both circuits are tested on a high-speed probe station.



(a) (b)

Figure 6:Chip photograph:(a) MUX (b) VCO

To simplify the testing hardware, a built-in shift register is included in the MUX circuit to propagate the input data, providing two retimed input data sequences with only one pseudo-random binary sequence (PRBS) source. The MUX circuit was tested the day before the paper submission deadline. Figure 7 depicts the preliminary results of the input and output waveforms in response to a 10-Gb/s pseudo-random input data of length $2^{31} - 1$, suggesting an rms and peak-to-peak jitter of 1.57 and 8.5 ps, respectively. The MUX consumes 22 mW from a 1.8-V supply excluding the buffer.

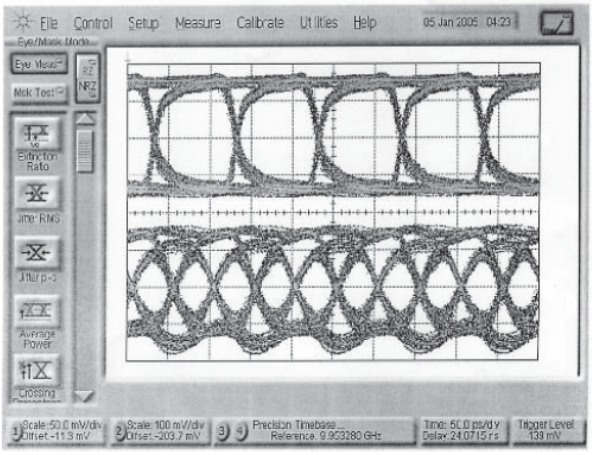


Figure7:Input and output waveforms of the MUX

The VCO achieves a phase noise of −90 dBc/Hz at 1-MHz offset while consuming 1 mW from a 1.3-V supply. Figure 8 plots the spectrum. The tuning characteristic is depicted in Fig. 9, where a tuning range of 1.4 GHz is obtained when the supply voltage is equal to 1.8 V. The "in-situ" measurement suggests an inductor Q of 12 at 40 GHz. The VCO begins to work at a tail current of 450 μA with a 1-V supply. This design presents a figure of merit [FOM, $L(\Delta f/f)2P$] of −182 dBc/Hz. Table 1 summaries the performance of these two circuits and some other previously published works realized in standard CMOS technologies.

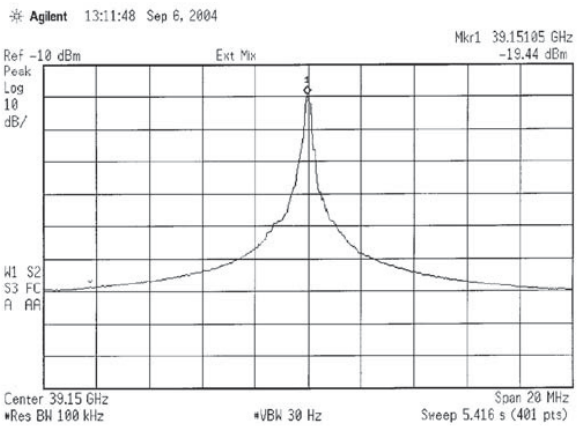


Figure 8: VCO output spectrum

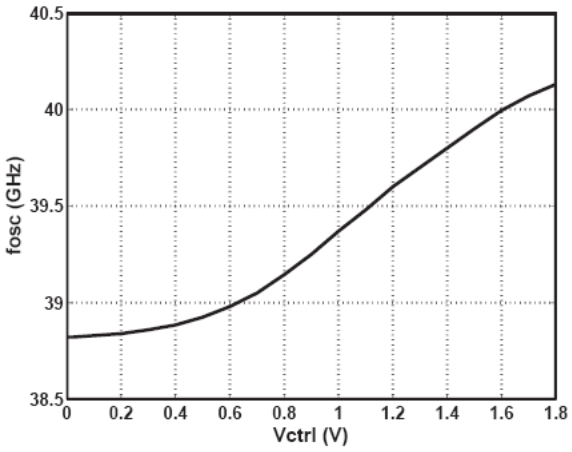


Figure 9: VCO tuning range

Parameter	[9]	[10]	[11]	This Work
Max. Output Data Rate	25 Gb/s	40 Gb/s	43 Gb/s	20 Gb/s
Function	2 : 1	2 : 1	2 : 1	2 : 1
Supply Voltage	1.5 V	1.5 V	1.8 V	1.8 V
Power Diss.	44 mW	100 mW	285 mW	22 mW
Technology	0.12–um CMOS	0.12–um CMOS	90–nm CMOS	0.18–um CMOS

(a)

Parameter	[12]	[13]	This Work
Frequency	43 Gb/s	51 Gb/s	40 Gb/s
Tunning Range	4.2 %	1.2 %	3.5 %
Phase Noise (@ 1–MHz offset)	–90 dBc/Hz	–85 dBc/Hz	–90 dBc/Hz
Supply Voltage	≥ 1 V	≥ 1 V	≥ 1 V
Power Diss.	7 mW	1 mW	1 mW
Chip Area	N/A	0.5 mm x 0.9 mm	0.3 mm x 0.45 mm
FOM	–174 dBc/Hz	–179 dBc/Hz	–182 dBc/Hz
Technology	0.13–um Standard CMOS	0.12–um Standard CMOS	0.18–um Standard CMOS

(b)

Table 1: Performance summary for (a) MUX(B) VCO

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