行政院國家科學委員會專題研究計畫 期中進度報告

可應用於軟性電子的TFT電路設計技術之開發--總計畫(1/3)
期中進度報告(完整版)

計 畫 類 別 ：整合型
計 畫 編 號 ：NSC 95-2220-E-002-017-
執 行 期 間 ：95年08月01日至96年07月31日
執 行 單 位 ：國立臺灣大學電子工程學研究所

計 畫 主 持 人：闕志達
共 同 主 持 人：汪重光、呂良鴻、黃俊郎、李泰成、李建模

處 理 方 式 ：期中報告不提供公開查詢

中 華 民 國 96年05月30日

行政院國家科學委員會專題研究計畫成果報告

可應用於軟性電子的TFT 電路設計技術之開發

Development of TFT Circuit Design Technology for Flexible Electronics Systems

計畫編號：NSC95-2220-E-002-017

執行期間：95 年 8 月 1 日 至 96 年 7 月 31 日

主持人：闕志達 台灣大學電子工程研究所教授

共同主持人：呂良鴻 台灣大學電子工程研究所教授

汪重光 台灣大學電子工程研究所教授

李泰成 台灣大學電子工程研究所教授

黃俊郎 台灣大學電子工程研究所教授

李建模 台灣大學電子工程研究所教授

簡韶逸 台灣大學電子工程研究所教授

計畫參與人員：王兆勳 白俊英 吳建翰 沈學聰 林正偉 林政校 姜俊宇 高瑋聰 張晏碩 陳邦釗 陳翰儒 鄭啟玄 譚亦荃

一、 中文摘要

本整合型計畫之主要目的是結合本研究團隊中的通訊射頻/類比/數位積體電路、電路測試與容錯技術等有關專長的研究人力，以軟性電子(flexible electronics)中 TFT 電晶體電路設計技術。軟性電子是將半導體電路製作於軟性基板上，其元件特性變異性大，且速度非常慢，因此利用軟性電子 TFT 電晶體設計電路時具有極高技術難度，所開發的電路與設計技術也具創新價值。

英文摘要

The objective of this group project is to leverage the specialty of members in the research team, including RF circuit design, analog circuit design, DSP circuit design, and built-in self test, fault-tolerant technique, in the design and implementation of key circuit components using a flexible electronics technology with amorphous-Si TFT device. Due to the great variation and low mobility of the flexible electronics device, circuit design and testing/fault tolerant techniques for this kind of process entail technical challenges as well as innovative endeavor.

二、計畫的緣由與目的

軟性電子(flexible electronics) 目前就像三十年前的矽半導體，雖然元件特性不夠好且有許多的缺點，但是卻充滿了無限發展潛力的未來。如同矽半導體一般，低價、多樣性且可大量生產的特性，具有無窮的市場潛力。因此，近幾年來有機電子元件引起許多世界一流研究單位的注意，競相投入此一領域。軟性電子的好處在於可撓曲性、可大面積製作和低廉簡單的製造。軟性電子是將電路製作於軟性的基板之上，例如塑膠基板，以軟

性電子製作的系統，將具有可撓曲的特性，也因此，對於某些特定的應用上會有其優點。此外，關於軟性電子的製程，目前國際上已有使用 roll-to-roll 的方式製造的軟性電子雛型，使用這種方法，將使得軟性電子的生產成品大減，而可用於一些低價大量的產品，此外，成品的大小也不再受限，也可以輕易地做出非常大型的電路。

軟性電子的相關研究目前仍在萌芽期，其具有幾個重要的關鍵元件：有機(organic)或是無機(inorganic)的半導體材料,微米或是奈米結構的材料，連線及電路的印製技術，薄膜電晶體(thin-film transistor, TFT)，大型軟體基板製程技術，軟性電路設計等。許多人發現軟性電子的元件和應用和顯示系統具有非常高的相關性，而目前一些常被用於製造顯示系統的一些材料，諸如非晶矽(amorphous Si)或是低溫多晶矽(low-temperature polysilicon)，還有有機半導體(organic semiconductor)等都是軟性電子非常可能使用的材料。

本整合型的計畫目標在於針對軟性電子的 TFT 元件進行電路設計相關技術的開發，其中包含軟性面板整合型系統(system on panel)所需的類比電路，電源電路，數位訊號處理電路，電路測試，容錯技術等等，涵蓋一個以新式軟性電子製程設計系統所需要的大多數技術。本整合型計畫所提出的電路主要係以國內目前軟性電子研究居於主導地位的工研院電子所 (ERSO)所提供的 a-Si TFT 製程為標的，研發其中的感測陣列與讀取電路、無線功率與資料傳輸電路、顯示驅動及其週邊電路、高效能數位信號處理器、TFT 陣列錯誤容忍技術、數位電路測試及容錯技術等。

三、方法及結果:

本計畫第一年的執行內容，主要為完成各子計畫所負責之多項電路進行設計模擬並完成佈局。以下就各子計畫的成果分別敘述。

子計畫一: 感測陣列與讀取電路

In this work, the OPAMP circuit in amorphous silicon process is designed. Meanwhile, several designs based on the OPAMP are developed as well such as inverting amplifier, non-inverting amplifier (optional), and charge amplifier etc.

Gain-Enhancement OPAMP

Because this process only has NTFT, we use the basic structure (Fig.1(a)), but we can't get enough voltage gain in this structure. Therefore, we must research and try if there are other methods which can improve gain. A new architecture, called Gain-Enhancement OPAMP (Fig. 1(b)), is proposed. We use the feedback technique that amplifies the small signal of V_{out} and feed it back to the gate of M2. If we look up from M2's source, we can find the equivalent impedance of small signal is $\frac{1}{g_{m2}(1-A)}$, and then we can get the voltage gain of $g_{m1}[\frac{1}{g_{m2}(1-A)} // r_{o1} // r_{o2}]$. If we make A more than one, we can obtain a negative resistance and it will make output impedance larger. Consequently, the voltage gain of the amplifier becomes larger. This concept is extended to a fully differential operational amplifier (Fig.2).

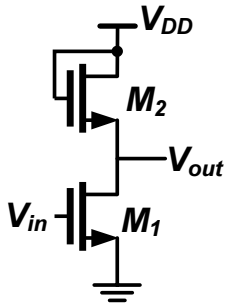

Fig. 1(a)

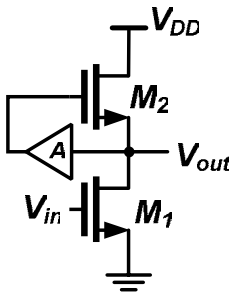

Fig. 1(b)

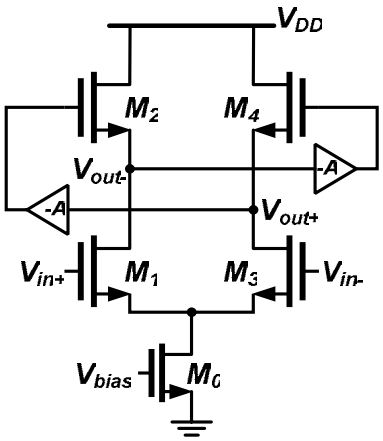

Fig. 2

Several different structures of single-ended output OPAMP are derived from the previous fully differential OPAMP:

a. Single-ended output OPAMP 1 (Fig.3)

b. Single-ended output OPAMP 2 (Fig.4)

c. Folded-Cascode OPAMP (Fig.5)

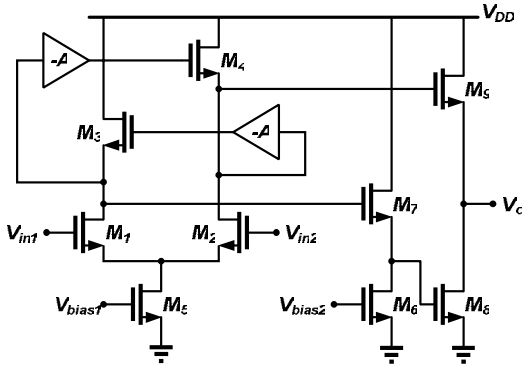

Fig. 3

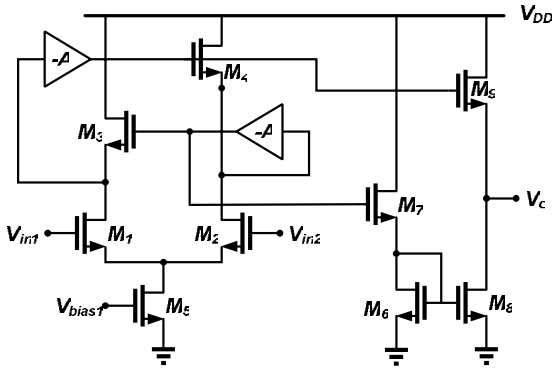

Fig. 4

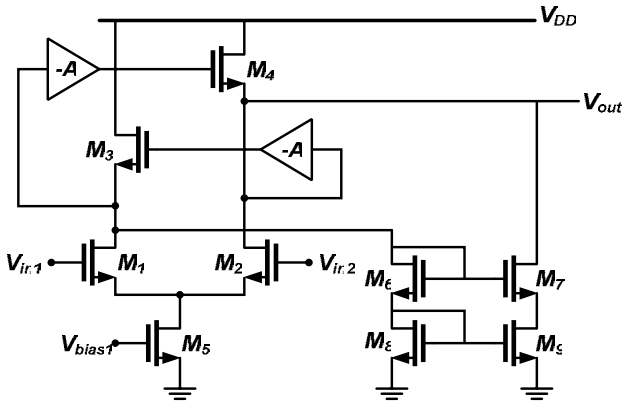

Fig. 5

We have implemented Unity Gain Buffer, inverting amplifier, and non-inverting amplifier using those amplifiers in Figs. 1—5. The topology of charge amplifier is illustrated in Fig. 6. The OPAMP utilized here is a folded-cascode architecture.

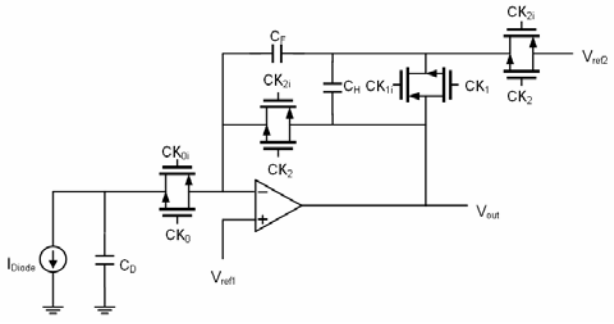

Fig. 6

We propose another structure of OPAMP to improve the problem of insufficient gain. As shown in Figure 7, I use only the source degeneration. For a single stage amplifier, if we

use a resistor R_S connecting to the source of the main TFT, then the total transconductance Gm is: $Gm = \frac{g_m}{1 + g_m R_s}$. Now, if we replace R_S with a negative resistor, thus the term of denominator $1 + g_m R_s$ becomes smaller so as to increase the Gm. As the Gm become larger, the gain of this circuit is also increase.

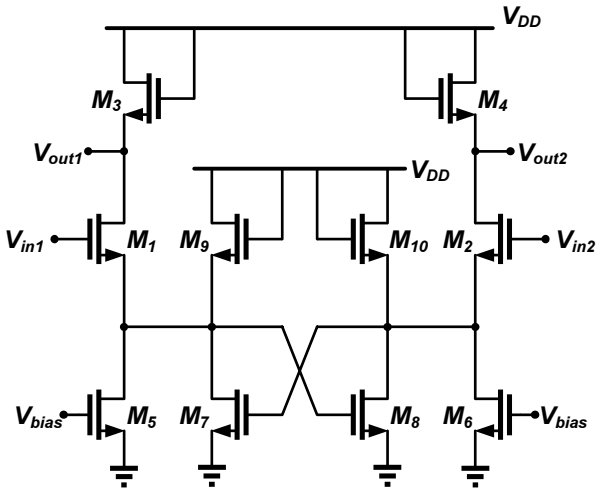

Fig. 7

This amplifier can be made single-ended as shown in Fig. 8.

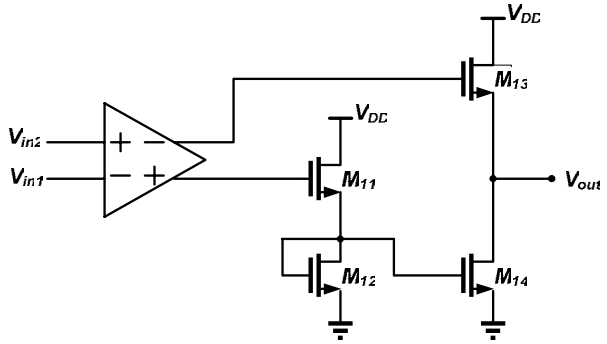

Fig. 8

All of the above circuits have been designed and simulated. The layouts have been checked against schematics and are now under fabrication through a foundry provided by ITRI (工研院).

子計畫二: 無線功率與資料傳輸電路設計

The goal of this subproject will focus on the circuit designs of power converter, ring oscillator and amplifier. Key macro components of the power converter will be developed by using the flexible technology. The analog design flow and integrated circuit techniques will also be investigated on flexible electronics circuit design. A ring oscillator and a gain amplifier will be demonstrated as a vehicle of design for reliability.

Cross-Coupled Charge Pump DC-DC Converter

The function of charge pumps is to generate a voltage larger than the supply voltage from which they operate at. In this circuit (Fig. 9), the cross coupled charge pump was implemented as a DC-DC converter to boost the clock signal from 10-Vpp up to 30-Vpp by using a-Si TFT technology. The adopted architecture uses two non-overlapping, anti-phase clocks with amplitude of V_{DD}. Transistors M1, M2 and M5, M6 are successively switched on and off in order to charge capacitors C1, C2 and C3, C4 to the voltage Vin. After a few clock cycles, the clock signals on the top plates of the capacitors will assume amplitude of Vin+VDD. The diode connected transistors M3, M4 and M7, M8 are timed so that Vout nodes only can see this voltage.

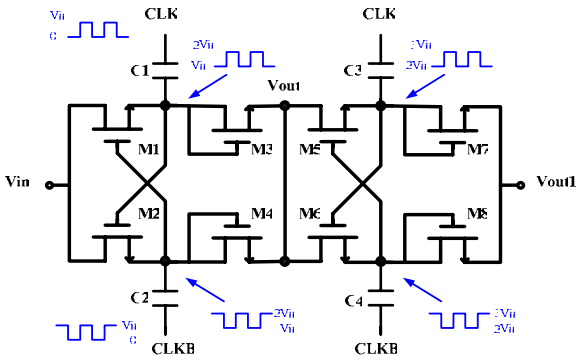

Fig. 9: Circuit diagram of the cross-coupled

charge-pump DC-DC converter

Ring Oscillator

The proposed ring oscillator consists of a number of gain stages in a loop. In the NMOS-only a-Si technology, a NMOS transistor operating in the deep triode region can serve as the load. The common mode DC voltage will varies in the cascaded multiple stages and thus, this variation will degrade the dynamic range of gain stage. The level shift block was adopted to maintain the output common mode level in each stage. But the additional circuit will limit the oscillator operation speed. This design has optimized stages between the gain stages and level shift blocks to achieve the maximum oscillation frequency by the a-Si technology. Fig. 10 is the circuit diagram of the Ring Oscillator. If the number of ring oscillator stages is n, the gain amplifier transfer function in each stage is A(s), the 3dB bandwidth in each stage is w_0. The maximum oscillation frequency can be described by the following equation:

$$w_{osc} = \tan\frac{180^\circ}{n} \cdot w_0$$

The minimum amplifier gain can be obtained by the following equation:

$$\frac{A_0^n}{\left(\sqrt{1+\left(w_{osc}/w_0\right)^2}\right)^n} = 1$$

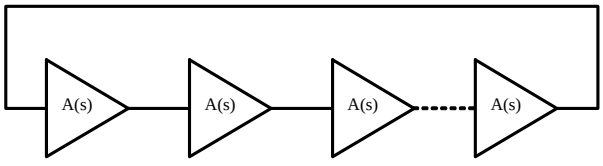

Fig.10: The schematic of the ring oscillator

In order to increase its operating frequency and reduce phase noise, the muti-feedback loop oscillator architecture was adopted in this design, as shown in Fig. 11. The NMOS transistors feed back the previous stage signals to the conventional ring oscillator to improve the phase noise and the operating frequency.

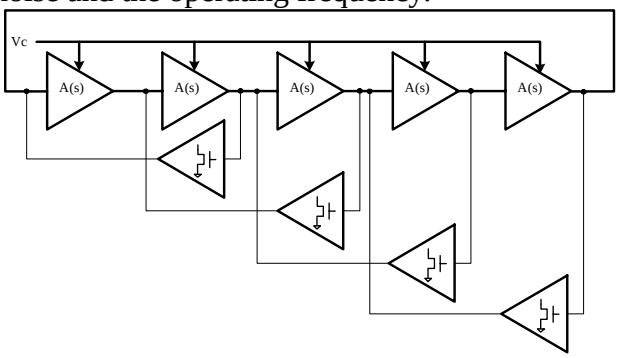

Fig.11: Multi-feedback ring oscillator

Gain Amplifier

The gain amplifier can amplify the input signal. However, it is very difficult to design a high gain amplifier by using the NMOS-only a-Si technology due to the insufficient electron mobility and low Gm value. In addition, the process variation also decreases the circuit reliability. In order to overcome the process variation in this design, the amplifier adopts the architecture shown in Fig. 12. The two stage cascade topology was adopted to increase the output impedance and the amplifier gain. The small signal transfer function can be derived as:

$$DC\ Gain \approx \frac{-g_{M1}g_{M3}}{g_{M4}g_{M1} - g_{M3}g_{M2}} = \frac{-1}{\frac{g_{M4}}{g_{M3}} - \frac{g_{M2}}{g_{M1}}}$$

From the question, it can be illustrated; the amplifier gain only depends on the devices size ratio when all of the NMOS transistors are operated in the saturation region. Therefore, the proposed amplifier can resist the process and threshold voltage variation. According the simulation, a 24dB voltage gain can be achieved by using the a-Si technology.

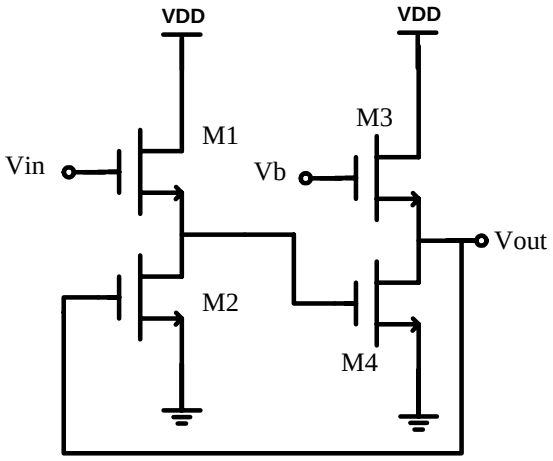

Fig. 12: Schematic of gain amplifier

子計畫三: 顯示驅動及其週邊電路

This subproject develops three circuits that are essential to drier circuits of display, namely 6-bit R-2R DAC, shift register, and analog buffer amplifier. We use R-2R ladder (Fig. 13) to implement binary-weighting, and use TFTs operate in the triode region to replace resistors.

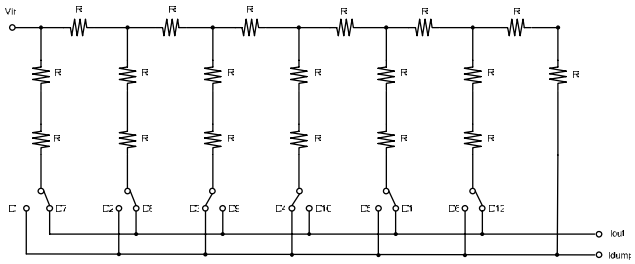

Fig. 13: R-2R ladder

Linear 6-bit R-2R ladder

Figure 14 is the circuit of linear 6-bit R-2R ladder, width-length ratio （W/L）of every TFT is 100um/8um. D1~D6 are 6 bit input signals （low：0V；high：25V）, D7~D12 are the inverse of D1~D6. Vg is the gate voltage of odd number TFT（25V）. Input voltage Vin use 15Vcan make sure that all TFTs operate in the triode region, and it can get about maximal 19uA current at Iout node.

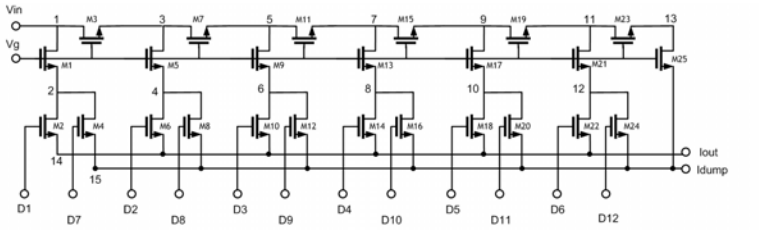

Fig. 14: Linear 6-bit R-2R ladder

Nonlinear 6-bit R-2R ladder

If we compare the current curve of linear 6-bit R-2R and the corresponding voltage wanted to express on the pixel electrode, we can observe linear property in middle part. So we must do trimming of piecewise in R-2R linear curve, and this has to change the slope of R-2R curve.

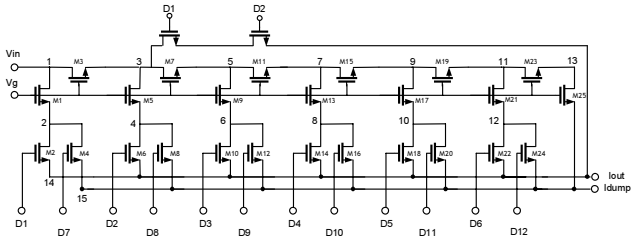

Fig. 15

Shift Register

The frequency of input control signals in liquid crystal display（LCD）are not too high, so we could use multiplexing to combine partial input signals to form a group of signals in order to decrease the number of pin-count. The basic circuit to convert signals from serial to parallel type is shift register, and consequently we use a-Si TFT to realize such a shift register. Figure 16 is the circuit diagram,

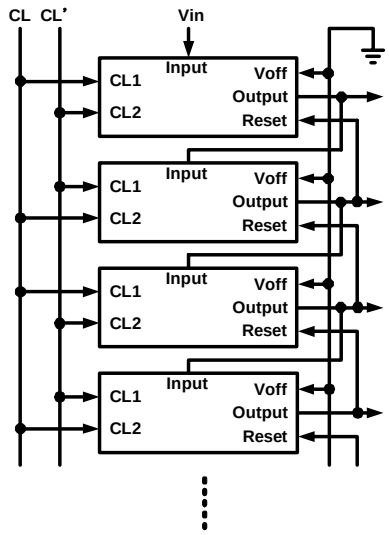

Fig. 16

子計畫四：軟性面板製程之高效能數位信號處理器之設計

The following is the architecture of MAC, where L1, L2, and L3 are asynchronous Latches.

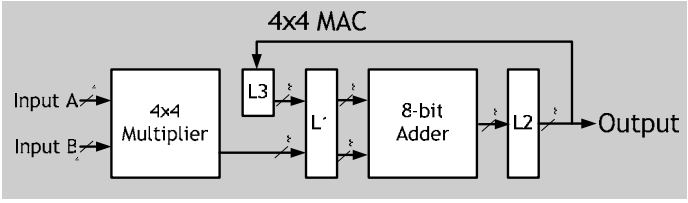

Fig. 17

Multiply-and-accumulator consists of three parts:
(a) Multiplier: Here we implement a 4x4 dual-rail signed multiplier. There are several methods to implement a multiplier. We use Wallace tree, which is based on carry-save adder. This kind of multiplier has shorter operation time to compute the product.
(b) Adder: Because we use handshake protocol, data will not transfer together at specific time. Thus it is not essential to implement the adder with some carry-look-ahead technique. Carry-ripple adder is enough here.
(c) Asynchronous latch: Dual-rail asynchronous latch consists of data and acknowledge signal. The datum has been received if one of the two wires is high. Then set acknowledge high to let the previous latch know that the datum has been received. If both the wires are low, this latch is ready to receive datum. Thus we set acknowledge low to inform the previous latch. The follow is the architecture of asynchronous latch.

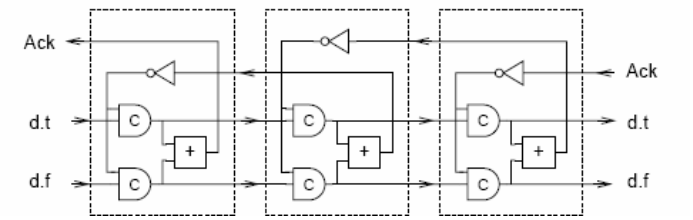

Fig. 18

Firgure_3 is the architecture of the asynchronous FIR filter.

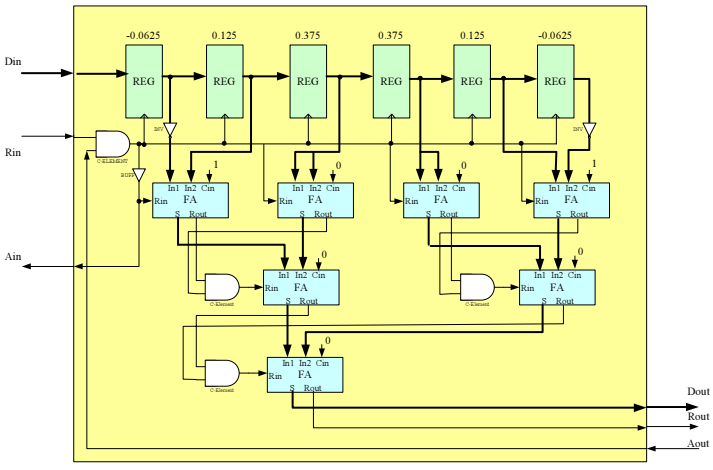

Fig. 19

Basically, the internal circuit are all combinational circuit, the multiplication and accumulation operation completed by the shift wire assign and adder tree. We use the 2-bit asynchronous full-adder, it is similar to the dynamic logic in the synchronous circuit, only when request is high, the FA can work, or it is always in the pre-charge state. Besides, because

of the process only have the NMOS, so all the PMOS for pre-charge are changed to always-on NMOS.

子計畫五: TFT陣列的具錯誤容忍技術之開發

A. The built-in charge sensing architecture

Figure 20 depicts the overall charge sensing architecture. It consists of the charge sensing capable buffers and the serial voltage readout circuitry. Both reuse the offset compensated analog buffers inside the source drivers.

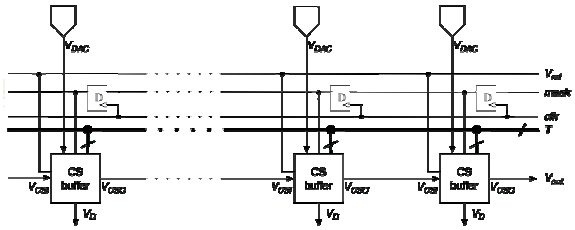

Fig. 20: Charge sensing architecture.

The proposed charge sensing architecture allows three operation modes: the functional mode, the charge sensing mode, and the serial readout mode. In the functional mode, the CS-buffers act the same an offset compensated buffer. In the charge sensing mode, the CS-buffers perform the charge-to-voltage conversion. Finally, the serial readout mode supports serial readout of the charge sensing results.

The signals are described below.

1. *T* is the CS-buffer control signal bus which is shared among all the CS-buffers.
2. V_{ref} is an analog bus shared among all the CS-buffers. Via this port, the external tester supplies the test voltage and the charge sensing base voltage V_{base}.
3. To support serial voltage readout, the CS-buffers must be divided into two groups that are configured differently. The *mask* signal is used to differentiate between these two groups. A D-type flip-flop (DFF) is added to each CS-buffer to store its own copy of mask value. The DFFs are connected as a shift register, and the desired mask values are delivered to the CS-buffers via the shift operation.
4. The V_{out} port is the analog readout port where the charge sensing results can be measured by external testers. To speed up the readout process, one may utilize multiple readout ports.
5. The CS-buffers are concatenated by connecting the V_{CSO} port of each CS-buffer to the V_{CSI} port of the CS-buffer at its right-hand side. V_{CSO} of the last CS-buffer is then connected to the array's V_{out} port.

B. The charge-sensing buffer design

The proposed charge sensing capable buffer is illustrated in Figure 21. Compared to the offset compensated analog buffer, four more switches are added. Among the switches, S_1 to S_6 facilitate the functional mode and charge sensing mode operations; the S_7 switch, on the other hand, is activated only during the serial readout mode.

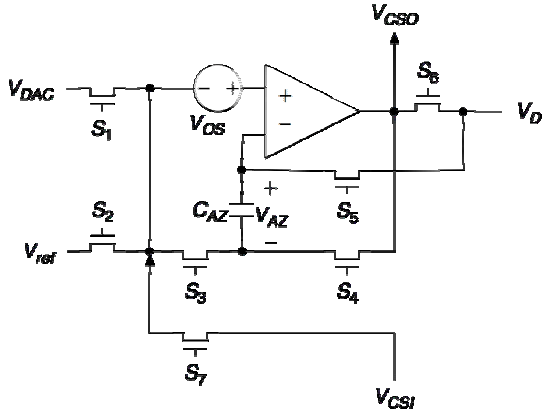

Fig. 21. Charge sensing capable buffer.

	functional		charge sensing			serial read out		
	AZ	WP	CWP	WDL	CTV	HV	RAZ	UB
S_1	1	1	0	0	0	0	0	0
S_2	0	0	1	1	1	1	0	0
S_3	1	0	0	1	0	0	1	0
S_4	0	1	1	0	1	1	0	1
S_5	1	0	0	1	1	0	1	0
S_6	1	1	1	1	0	0	1	0
S_7	0	0	0	0	0	0	1	1

Table 1: Control Signal Summary

The control signal values in different operations configurations are summarized in Table 1.

1. In the functional mode, the two configurations are auto-zero (AZ) and write-pixel (WP).
2. In the charge sensing mode, the CS-buffer performs the following operations: charge-sensing-write pixel (CWP), write-data-line (WDL), and charge-to-voltage (CTV). A complete charge sensing operation involves four configurations in the following order:

AZ => CWP => WDL => CTV

3. The basic idea of the serial readout operation is depicted in Figure 22. After the charge-to-voltage operation, the voltage is available at each CS-buffer's opamp output terminal. The output voltage V_1 can be directly read out from the V_{out} port. To read out V_2, we configure the first CS-buffer as a unit buffer and let its input be from the V_{CSI} terminal. This way, V_2 is made available at the V_{out} port for measurement. Note that offset compensation must be performed to compensate for the opamp offset voltage. Similarly, to read out V_3, we configure the first and second CS-buffers as unit buffers. To summarize, to transfer a CS-buffer's charge sensing result to V_{out}, all the CS-buffers between it and V_{out} are configured as unit buffers.

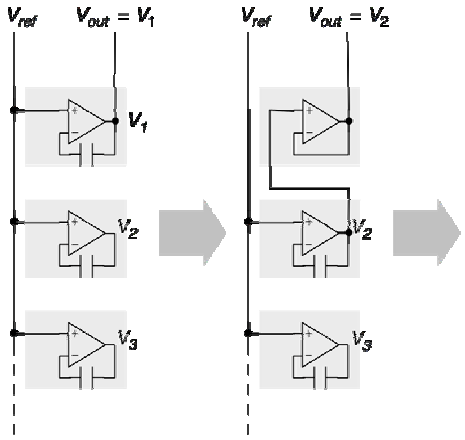

Fig.22: Serial voltage readout scheme.

子計畫六：軟性電子數位電路測試及容錯技術之開發

The scan chain block diagram for four-phase dual-rail asynchronous circuit is shown in Fig. 23.

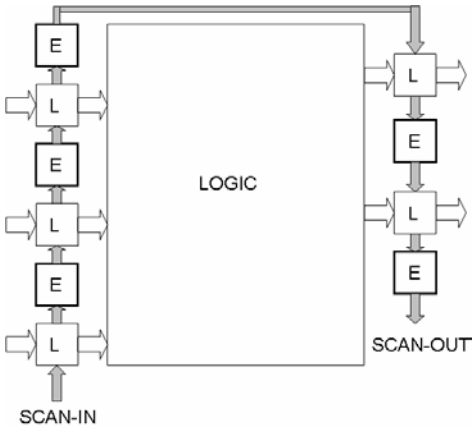

Fig. 23

The empty-cells have been inserted between every two latch-cells in the four-phase dual-rail asynchronous circuit. The original latch-cell and a new inserted empty-cell are combined to form one new scan-cell as shown in Fig. 24. All scan-cells are serial connected as a scan chain.

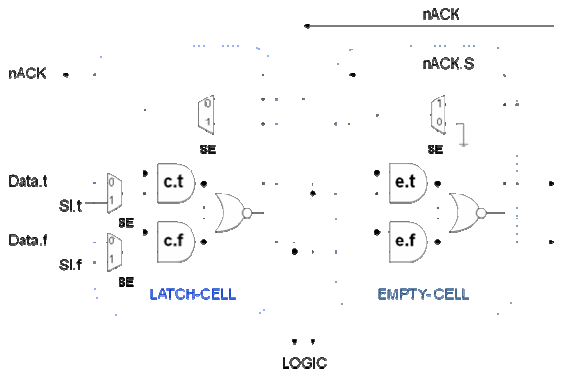

Fig. 24

In normal operation mode (SE=0), the control signals between latch-cell and empty-cell are opened by multiplexer and the values contain in empty-cells are locked to “empty” (e.t=e.f=0).

In test mode (SE=1), the control signals between latch-cell and empty-cell are connected. The Fig. 25 shows the equivalent circuit of scan-cell under test mode.

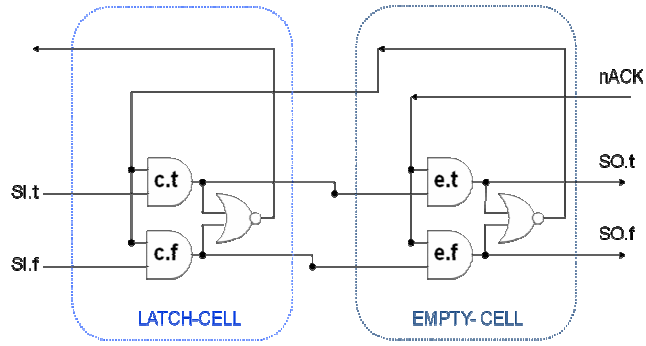

Fig. 25

The special blocks are Testkey and 4-bit full-adder with long inter-wire. Testkey (large transistor) is designed for measurement of destructed NMOS. This will be helpful to expect the folded element in TFT.

Full adder with long inter-wire is designed to measure its delay behavior. Because TFT has a special characteristic of large area, the measurement will be a good reference in TFT circuit delay expectation.

四、 結論與討論

During the first year of this project, the research group of professors in this project have meet every two weeks regularly and as such have a formed a strong team in SoC design, especially all groups have finalized their a-Si circuit and layout and the final layouts have been integrated and sent to ITRI for a-Si process fabrication. We expect to receive the fabricated circuits and have the preliminary test results in September, 2007.

五、參考文獻

[1] J. F. Dickson, “On-Chip High-Voltage Generation in MNOS Integrated Circuit using an Improved Voltage Multiplier Technique,” IEEE J. Solid-State Circuits, Vol. SC-11, No. 3, pp. 374-378, June, 1976.

[2] Yoshihiro Nonaka,, et al., *“A DC-DC Converter Circuit Integrated into a Poly-Si TFT LCD Containing a 6-bit DAC”* , *SID 2003* Digest, pp.1392-1395.

[3] Woo-Jin NAM, et al., “Low-Voltage Driven P-Type Polycrystalline Silicon Thin-Film Transistor Integrated Gate Driver Circuits for Low-Cost Chip-on-Glass Panel”, Japanese Journal of Applied Physics Vol. 45, No. 5B, 2006, pp. 4389–4391.

[4] C W Lin and Y M Tsai, “High-efficiency integrated charge pump circuits for poly-Si TFT-LCDs,” SID Symposium Digest Tech Papers 35, 1085–1087 (2004).

[5] Y. Nakagome et al., “An experimental 1.5V 64 Mb drain,” IEEE JSSC, Vol. 26, pp. 465-472.

[6] Lizhong Sun, and Kwasniewski, T.A. “ A 1.25-GHz 0.35-µm monolithic CMOS PLL based on a multiphasering oscillator,” IEEE J. Solid-State Circuits, vol. 36, pp. 910-916, June. 2001.

[7] Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, 2000

[8] Tetsuro Itakura, Hironori Minamizaki, Tetsuya Saito, and Tadashi Kuroda ,”A 402-Output TFT-LCD Driver IC With Power Control Based on the Number of Colors Selected”, IEEE Journal, Solid-State Circuits, ,Vol. 38, No. 3, pp. 503 – 510. March.2003.

[9] Klaas Bult and Govert J. G. M. Geelen,“An Inherently Linear and Compact MOST-OnlyCurrent Division Technique”, IEEE Journal of Solid-State Circuits, ,Vol. 21, No. 12, pp. 1730 – 1735, December.1992.

[10] Clemens M. Hammerschmied,Qiuting Huang,” Design and Implementation of an Untrimmed MOSFET-Only 10-Bit A/D Converter with 79-dB THD,” IEEE Journal of Solid-State Circuits, Vol. 33, No. 8,pp. 1148– 1157, August.1998.

[11] Po-Ming Lee, and Hung-Yi Chen,”Adjustable Gamma Correction Circuit for TFT LCD”, IEEE International Symposium, Circuits and Systems, pp. 780-783, May. 2005.

[12] Ya-Hsiang Tai, Design and Operation of TFT-LCD

Panels, Wu-Nan Book, the first edition ,Jun. 2006.
[13] Chun-Chieh. Chen, Nan-Ku. Lu ,"Color-Depth Improvement using Gamma Voltage Control", SID Symposium Digest of Technical Papers, pp. 351-354,June. 2006.
[14] Byung Seong Bae, Jae Won Choi, Jae Hwan Oh, and Jin Jang "Level Shifter Embedded in Drive Circuits With Amorphous Silicon TFTs", IEEE Trans. on Electronic Devices, Vol. 53, No.3, March 2006
[15] Kambiz K. Moez, "An integrated a–Si TFT demultiplexer for driving gate lines in active-matrix arrays", IEEE ISCAS, pp. 940– 943,2004
[16] A. Kumar, S. Sambandan, K. Sakariya, P. Servati, and A. Nathan, "Amorphous silicon shift registers for display drivers" American Vacuum Society, Technol A, Vol. 22, No. 3,pp. 981–986,May/Jun2004

六、計畫成果自評

本計劃於第一年度間主要工作進度為與工研院協調有關軟性電子 a-Si 製程，研究人員則致力於了解熟悉製程與其元件特性，於年度結束前二個月，我們已設計完成各種新式 TFT 電路與測試元件並已下線至工研院，預期將於 3-4 月後可以獲得完成的量測結果。有關研究成果發表論文則因電路尚待製作與量測，故目前尚無相關論文發表。