行政院國家科學委員會專題研究計畫 成果報告

晶片系統之信號與電源完整性問題
研究成果報告(精簡版)

計 畫 類 別 ：個別型
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執 行 期 間 ：96 年 01 月 01 日至 96 年 10 月 31 日
執 行 單 位 ：國立臺灣大學電子工程學研究所

計 畫 主 持 人：盧奕璋

計畫參與人員：碩士班研究生-兼任助理：陳建偉、鄭凱銘、郭仲宇、陳勝堯

報 告 附 件 ：出席國際會議研究心得報告及發表論文

處 理 方 式 ：本計畫可公開查詢

中 華 民 國 97 年 01 月 31 日

■ 成 果 報 告

行政院國家科學委員會補助專題研究計畫 □期中進度報告

晶片系統之信號與電源完整性問題

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成果報告類型(依經費核定清單規定繳交)：■精簡報告　□完整報告

本成果報告包括以下應繳交之附件：

□赴國外出差或研習心得報告一份

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■出席國際學術會議心得報告一份

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執行單位：國立台灣大學電子工程學研究所

中　　華　　民　　國　　97 年　1 月　31 日

中文摘要

對於系統晶片的設計來說，將易受干擾的電路與會產生大量雜訊的數位電路放在同一晶片上是一個很大的挑戰。數位電路同時切換造成的雜訊（SSN）會造成信號與電源完整性（SI/PI）的問題。本研究主要的工作為：(1)探討 SSN 對高速介面電路或時序模組造成的影響，(2)分析晶片上去耦合電容對 SSN 的抑制成效。

報告內容主要包括:：(1)已提交至國家晶片中心審查之測試晶片，(2)預計於二月中提交至國家晶片中心審查之測試晶片，(3)發表於 *IEEE Trans. on Instrumentation and Measurement* 之內容摘要，共三個部份。當量測工作結束時，將可提出有關 SI/PI 的設計準則。期望能幫助 SoC 設計工程師在設計初期就能將 SI/PI 問題納入考慮。

英文摘要

In SoC applications it is always a challenge to integrate sensitive components with noisy digital blocks on the same chip. Simultaneous switching noise (SSN) generated by digital blocks will cause signal and power integrity (SI/PI) issues. In this study, we will work on: (1) characterizing SSN and its impacts to high-speed I/Os and timing modules, and (2) study the effectiveness of on-chip de-coupling capacitors.

The contents in this report will include: (1) the I/O test chip in review by CIC, (2) the PLL test chip to be submitted to CIC in February, and (3) a summary regarding a noise sensor design paper, a joint work with Stanford University, published in *IEEE Trans. on Instrumentation and Measurement*, December 2007. Once the measurement results are obtained, the research team can deliver SI/PI-aware design guidelines to help SoC designers at the beginning of the design stages.

關鍵詞

信號完整性，電源完整性，系統晶片

Signal Integrity, Power Integrity, System-on-Chip(SoC)

前言

System-on-Chip (SoC) solutions hold promise in reducing the number of larger output buffers, lengths of connections between chips, cost of packaging and fabrication, thus leading to improved performance and reduced cost of products. However, as technology evolves, higher operating frequencies, lower power supply voltages, higher transistor density, and integration of different sub-systems on a single chip will complicate signal and power integrity (SI/PI) issues because of interactions between the blocks. There are several reports mentioning that extra effort must be applied to avoid SI/PI issues when integrating sensitive blocks with noisy systems. Since the driving force for a trade-off between how many resources should be allocated in the design and how much benefit can be achieved in realizing SOC applications. Novel approaches to solve SI/PI problems should receive more attentions as advocated in ITRS documents and research priorities proposed by SRC. Therefore, characteristics of noise and efficient noise suppression techniques should be studies more extensively in order to support high-performance system design.

研究目的

The study is to investigate signal integrity and power integrity (SI/PI) issues in SoC applications. The interactions between digital blocks and PLLs/LNAs have been studied at Stanford University in the late 1990s and early 2000s [1][2]. Following similar methodology, Simultaneous Switching Noise (SSN) and its impact to high speed I/Os and timing modules are studied in this project. In addition, the noise sensors are proposed jointly with researchers at Stanford University [3].

文獻探討

Test chips have also been fabricated and measured. Su [4] used an on-chip ring oscillator as the noise source and measured substrate noise using an NMOS transistor. Blalack [5] chose a shift register to generate digital noise, and studied how substrate noise impacts a Σ-Δ modulator in terms of SNR and SNDR. Xu [1] analyzed how an LNA is impacted by substrate noise. Larsson [6] gave a detailed survey about PLL jitter impacted by power grid/substrate noise under different power supply configurations. Distortion of the output waveform of an OPAMP due to substrate noise is discussed in Catrysse's work [7]. An 86 K-gate ASIC chip and a 12-bit I/Q up/down converter are implemented and investigated by van Heijningen in [8]. Nagata used a ripple-adder and shift registers [9], and a transition-controllable noise source [10] to investigate noise parameters, instead. In 2007 Symposium on VLSI circuits, there was a section dedicated to techniques for signal and power integrity [11].

研究方法

In the first test chip, the research team has implemented DDR3 compatible I/Os together with on-chip decoupling capacitors (joint work with Prof. H. S. Chen and T. L. Wu's group at National Taiwan University) to test how those I/Os perform under noisy environment (Fig.1). In addition, by changing the number of the decoupling capacitors attached to the power net using laser cuts, the researchers can alter cap values to evaluate the effectiveness of those caps as a function of their values and locations.

In the second test chip, a PLL running at 900 MHz with noise sensors is implemented, and the PLL is surrounded by noise injection points. By changing the noise patterns (including frequency, phase, amplitude), the students can observe how the designed PLL is effected by different noise characteristics (Fig 2). Besides, the test chip can be used to characterize how noise propagates in the substrate. The detailed methodology can be found in [2].

結果與討論

In the journal paper published [3], the Stanford-NTU team presents PMOS-based differential substrate and power-supply sensors and on-chip waveform sampler, which focus on wide bandwidth, reduced parasitic interactions, and compact size. PMOSs are used because they are less susceptible to substrate noise. The bandwidth of the proposed sensors, which is implemented with an IBM 0.13 μm CMOS technology, is from DC to 1.6 GHz. Linearity is better than 1.5% for substrate and 6% for power-supply sensors. Experimentally reconstructed waveforms with 20-ps time resolution allowed the measurement of amplitude, rise time, and overshoot of transition edges.

Design guidelines for solving SI/PI issues are carefully examined in this project, and test structures are designed to verify these guidelines. For example, locations of substrate contacts are critical; guard rings should be placed near injection points as well as sensitive blocks, if permitted; guard rings close to injection points could be more effective. The silicon data coming from the above mentioned test chips will help the research team to finalize good guidelines with quantitative evidences. Meanwhile, another test chip using flash ADCs as the test vehicle is being designed. Besides, an electromagnetic simulator, HFSS, is used to extract wire parasitics, which are included in circuit level simulations to study SSN on power grid and its impact to SRAM performance.

附圖（Please refer to the next page)

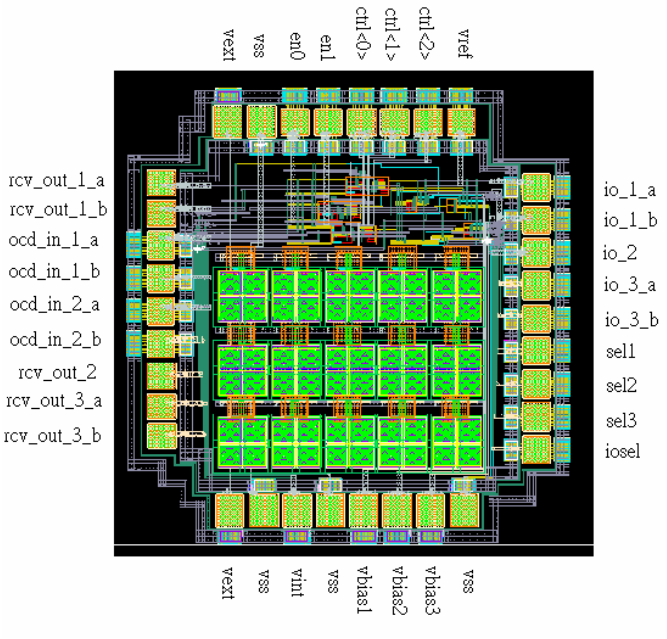

Fig. 1 Test chip (in review) for evaluating I/O performance and the effectiveness of on-chip de-coupling capacitors.

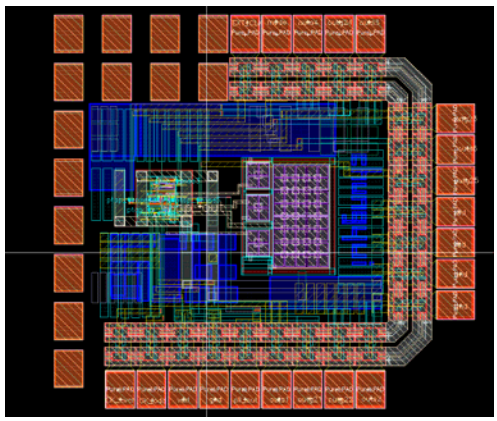

Fig. 2 Test chip (under revision, to be re-submitted to CIC in Feb, 2008) for evaluating SSN and PLL performance.

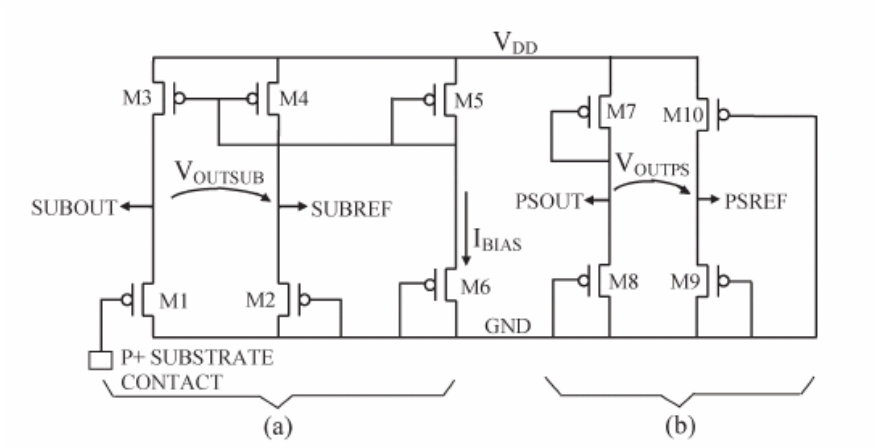

Fig. 3 (a) Substrate and (b) power grid sensors. [3]

計畫成果自評

The progress is a bit behind the schedule, since chip design takes longer than expected. Even so, the test chip for I/Os is in review, the test chip for a PLL is under revision. In addition, a test chip for flash ADCs is being designed. The simulation of SRAM performance impacted by SSN is in progress. A journal paper regarding substrate and power grid sensors is published jointly with the researchers at Stanford University. There should be solid results for publications or patterns once measurement data from the test chips are collected and analyzed.

參考文獻

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[11] http://www.vlsisymposium.org/2007/circuits/technical.html

出席國際學術會議心得報告

計畫編號	NSC 96-2218-E-002-018
計畫名稱	晶片系統之信號與電源完整性問題
出國人員姓名 服務機關及職稱	盧奕璋 助理教授
會議時間地點	June 14-16, 2007 Rihga Royal Hotel Kyoto, Kyoto, Japan
會議名稱	2007 Symposium on VLSI Circuits
發表論文題目	N/A

一、參加會議經過

在 2007 Symposium on VLSI Circuits 中整個 Session 12 是有關信號完整性與電源完整性技術的討論，共有四篇文章。包含 University of Minnesota 的”Silicon Odometer: An On-Chip Reliability Monitor for Measuring Frequency Degradation of Digital Circuits”和”A Switched Decoupling Capacitor Circuit for On-Chip Supply Resonance Damping”，University of Tokyo 的”An On-Chip Noise Canceller with High Voltage Supply Lines for Nanosecond-Range Power Supply Noise”，以及 Renases Technology 的”A 1.92ms-Wake-Up Time Thick-Gate-Oxide Power Switch Technique for Ultra Low-Power Single-Chip Mobile Porcessors”。其中 University of Minnesota 的兩篇同為 Prof. Chris H. Kim 所提出。第一篇是利用兩個 VCO 與一個比較器去偵測受 Stressed 與 Unstressed VCO 的頻率差，再用以推算電路可靠度的變化，第二篇則是利用 Switched Decoupling 電容做出 11 倍的等效電容，達成抑制 9.8dB 的共振雜訊。University of Tokyo 則是提出利用一組額外的高壓電源提供初始電流，減低原有電源的電流負載，以達到抑制原有電源上之 di/dt 雜訊。而 Renases Technology 則是探討控制 thick-gate-oxide power switch 的 slew rate 的方法，此項技術可以縮短 wake-up 的時間，但不會增加電流。個人認為第一篇(University of Minnesota)的內容相當有趣，值得作進一步的研究。

二、與會心得

除了信號完整性與電源完整性技術的討論外，大會也邀請到 Prof. Takao Someya 對軟性電子進行了深入淺出的介紹(題目是 Ambient Electronics with Organic Transistors)。在一個小時左右的演講裡，Prof. Someya 介紹了各種利用軟性電子技術的電路，包含壓力與溫度感測器組成的電子人工皮膚(electronic artificial skin)，利用電感特性的無線電力傳送裝置(wireless power transmission sheet)等。其它議程還包括最新的數位、類比、感測器、與記憶體等的電路設計。參加這個會議，除了可以了解最新的研究趨勢外，也提供了新的研究靈感。當然會議中也與來自美國、歐洲、日本及其他地區的學者與工程師進行交流，獲益很多。總結來說，參加 Symposium on VLSI Circuits 是一個很好的經驗，對日後的研究有非常正面的幫助。