CMOS Oversampling ΔΣ Magnetic to Digital Converters

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ABSTRACT

In this paper, a CMOS oversampling delta sigma (ΔΣ) magnetic to digital converter (MDC) is proposed. In the MDC, the magnetic operational amplifier (MOP) combines with the switched capacitor (SC) ΔΣ modulator, and converts the external magnetic field into digital form. Simulation and measurement results indicate that the average digital output versus the applied magnetic field is quite linear. The prototype circuit was fabricated in a 0.5um CMOS DPDM process. The circuit operates at a 5V supply voltage and the sampling rate of 2.5MHz. The maximum signal range of the converter is at least $\pm 100mT$ and the resolution can reach as small as 1mT. The gain error within $\pm 100mT$ is less than 3%. The conversion gain is 1.327mv/mT and the power consumption is 49.3mW.

1. Introduction

Due to the rapid development of technology, high efficiency and low cost of electronics can be reached easily. The collected information from environments prefers to be processed by means of electrical devices. Lots of physical quantities in life, such as the magnetic field, voice, light, pressure, temperature, etc. are converted to electrical signals with maximum possible accuracy and reliability [1]. For this reason, sensors play an important role in the micro-electrical-mechanical systems today. Magnetic sensors can be found in many applications [2-3], such as brushless motor controls, computer storage devices, security detectors, etc.

Signal processing becomes favorable in digital form due to its excellent anti-noise performance and easy design compared with its analog counterpart. The reliability and high speed of digital circuits can readily permit sensor systems to combine with other instruments for progressive processing. Oversampling analog to digital converters (ADCs) become popular recently because one can trade time for improvements of the resolution and SNR. The requirements on analog circuits can be greatly reduced compared with the Nyquist ADCs under the same performance demands.

In the paper, one ΔΣ MDC, whose output is proportional to the external magnetic field, is proposed. The architecture uses two op-amps to implement the MOP and the ΔΣ modulator. This paper is organized as follows: Section II introduces the operational principle of the magnetic MOSFET (MAGFET) and MOP. Section III describes the proposed ΔΣ MDC. Section IV shows the measurement results and the conclusion is given in Section V.

2. MAGFET and MOP

2.1 MAGFET

The operation of MAGFET is similar to that of the Hall sensor [4-5], except that the resulting output signals are different: the former is current, and the latter is voltage. Both of them output signals proportional to the corresponding excitations. The concave MAGFET device is utilized, whose physical structure has two split drains, as shown in Fig.1 [6-7].

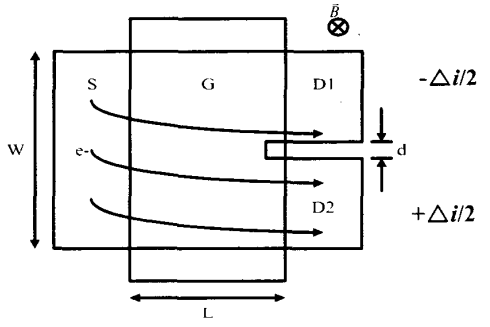

Fig.1 The concave MAGFET.

Under the condition of no external magnetic field imposed, it behaves likes two parallel MOSFET devices which have the same drain currents. The relative sensitivity of a split-drain MAGFET can be defined as

$$S_I = \left| \frac{1}{I_D} \frac{\Delta I_D}{B_\perp} \right| \qquad (1)$$

where I_D denotes the total current of two drains, ΔI_D denotes the quantity of current change in each drain due to the magnetic field $B_\perp$ which is perpendicular to the surface of the MOSFET. To take the layout mismatch problem and optimal sensitivity into account simultaneously, the aspect ratio of each MAGFET device in the following sections is chosen to be W/L=80um/40um and d=2um.

2.2 Magnetic Operational Amplifier (MOP)

The concept of the MOP is similar to that of a conventional op-amp [8]. The difference is that a magnetic field induced voltage, V_m, is added to the input of the MOP as shown in Fig.2. So the output voltage of the MOP is

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$$V_{out} = A \cdot (V_{in+} - V_{in-} + V_m) \quad (2)$$

Here A is the finite dc gain of this op-amp and V_m is the magnetically induced voltage, which is proportional to the applied magnetic field $B_\perp$, and can be expressed as the following equation:

$$V_m = S_m \cdot B_\perp \quad (3)$$

where S_m denotes the conversion gain from the magnetic field to the induced voltage. By connecting the MOP in a negative feedback configuration, the linearity can be improved and one can control the gain and sensitivity via resistor ratio.

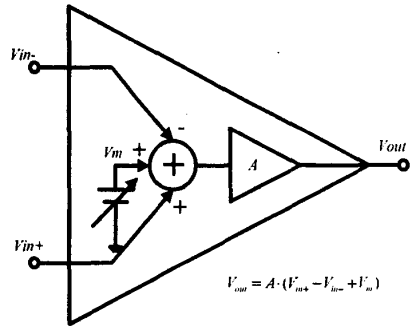


Fig.2 Concept of a magnetic operational amplifier.

A fully differential folded cascode op-amp is chosen as the MOP, which is shown in Fig.3. When no magnetic field is applied, the MOP works just like a general op-amp. When a magnetic field is applied, there will be a current imbalance between these two drains. The voltage difference between the differential outputs, V_{out+} and V_{out-}, will be generated. Two additional auxiliary input stage, mo1 and mo2 are introduced in order to compensate the offset inherently in a folded cascode op-amp due to process variation.

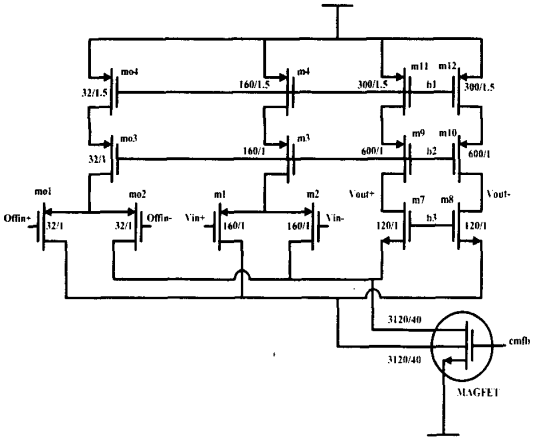


Fig.3 A fully differential folded cascode MOP.

The simulated and measured results of the MOP are shown in Fig.4. The solid and dash lines represent the simulated results and the dotted points indicate the experimental results. From Fig.4, one can observe that the measured results almost match with the simulated ones. The conversion gain is about 1.251mV/mT when the feedback resistor R2 is set to be 100kΩ, R1=1kΩ. When the feedback resistor R2 is up to 500kΩ, the conversion gain will reach 5.05mV/mT. The MOP has the higher conversion gains than those of the MAGFET devices merely.

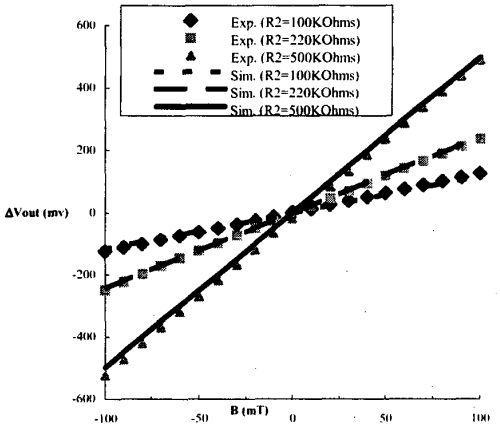


Fig.4 Simulated and experimental results of the inverting amplifier composed of a MOP and two resistors, R1=1K and R2=100kΩ, 220kΩ, and 500kΩ, respectively.

3. Magnetic to Digital Converters (MDCs)

A architecture for MDC is presented. It consists of a magnetic field readout circuit realized by the MOP and a first order ΔΣ modulator. The circuit of the MDC is described in detail as follows:

3.1 The MDC architecture

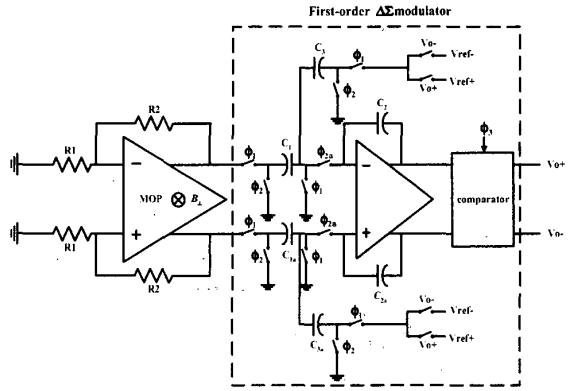
The circuit and timing diagram of the MDC are shown in Fig.5(a) and Fig.5(b) respectively. The linearized model is shown in Fig.5(c). From Fig5(c), the transfer function can be derived as follows:

$$Y = Vm \cdot (1 + \frac{R2}{R1}) \cdot \frac{C1}{C2} \cdot \frac{Z^{-1}}{1 + (\frac{C3}{C2} - 1)Z^{-1}} + E \cdot \frac{(1 - Z^{-1})}{1 + (\frac{C3}{C2} - 1)Z^{-1}} \quad (4)$$

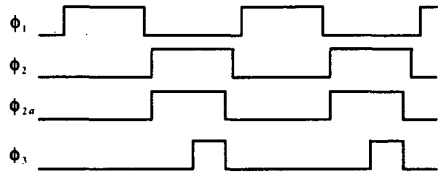
Where Y denotes the average digital output of the quantizer, and Vm is the magnetically induced offset voltage on the input of the MOP, which is proportional to the applied magnetic field $B_\perp$, and $(1 + \frac{R2}{R1})$ denotes the gain of the readout circuit realized by a MOP and two resistors, $R2$ and $R1$. The error E indicates the quantization noise. When choosing $C3$=$C2$, the expression will be simplified to:

$$Y = Vm \cdot (1 + \frac{R2}{R1}) \cdot (\frac{C1}{C2}) Z^{-1} + E(1 - Z^{-1}) \quad (5)$$

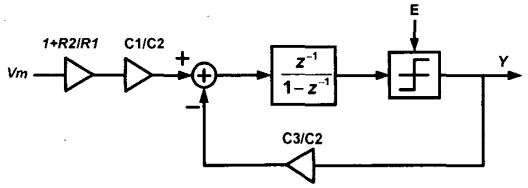
The signal is amplified by two stages, thus one can relax the amplification ratio requirement of each stage. Furthermore, from eq.(5), one can find that the quantization noise is first-orderly shaped as expected.



(a)



(b)



(c)

Fig.5 (a) Implementation and (b) timing diagram and (c) linearized model of the MDC.

4. Experimental Results

The chip has been encapsulated in a standard IC package and has been exposed to magnetic field in the range of $\pm 100mT$. The measurements are performed under a 5V power supply, and the sampling frequency of the ΔΣ modulator is 2.5 MHz. The number of samples is 65536 points which is large enough for average accuracy and still maintain a tolerable measurement time. Through a off-chip up-down counter, the digital average value of the comparator is obtained after shifting the bits of the output code depending on the sampled numbers. The average value is then fed into a D/A to return to an analog voltage which is used as our measurement result.

In the MDC architecture, off-chip resistors R1 and R2 are 1kΩ and 220kΩ, respectively. In the ΔΣ modulator, the capacitor values we choose are $C_1 = C_{1a} = 3pF$ and $C_2 = C_{2a} = 1pF$.

A layout microphotograph of the MDC scheme is shown in Fig.6. The circuit (without pad) occupies an area of 2.2mm × 0.85mm.

Measurement results are shown in Fig.7(a). The power consumption is 49.3mW. The conversion gain is 1.327mV/mT and the error between the measured points and the approximated line is under 3%. Further measurement is also performed, shown in Fig.7(b), where a smaller magnetic range, –10mT<B<10mT, is imposed on this system, and the linearity of the transfer curve is still maintained.

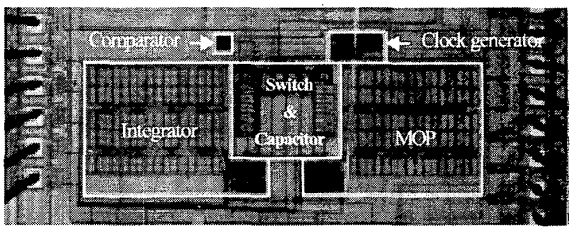
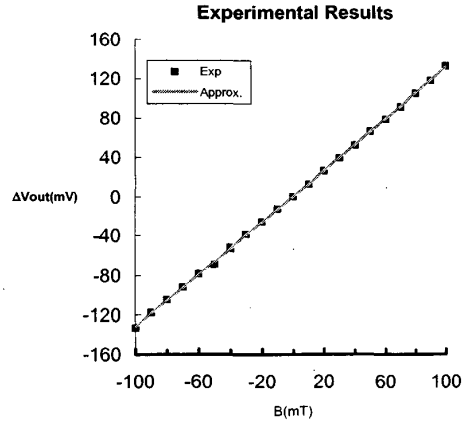
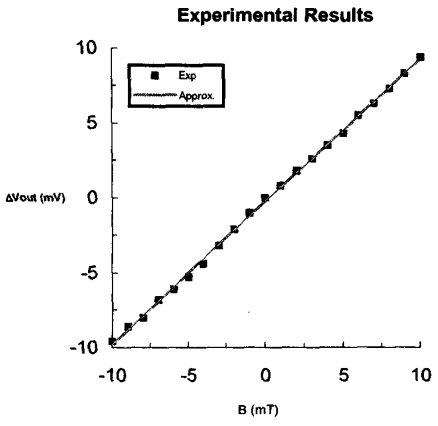


Fig.6 The layout microphotograph of the MDC.



(a)



(b)

Fig.7 (a) The average value of the comparator output from measurement (-100mT ≤ B ≤ 100mT). (b) The average value of the comparator output from measurement (-10mT ≤ B ≤ 10mT).

Note that the conversion gains obtained from the MDC are much smaller than that obtained from the MOP section. This is because the numbers of MAGFET array used in the MDC are reduced for chip area consideration. In summary, these results indicate that the average digital output of the MDC is proportional to the applied magnetic field.

5. Conclusions

In this paper, one architecture for MDC is presented. The magnetic field measured is a low-frequency signal, therefore a ΔΣ modulator is used hereby to transfer the magnetic signal into digital domain with its noise-shaping characteristic. The system structure of the MDC includes a fully differential MOP and a ΔΣ modulator. According to our experimental results, the conversion gain is 1.327mV/mT. The gain error is below 3%, and the linearity is acceptable in practical applications. The maximum magnetic field ranges of the MDC can be measured as large as 100mT.The minimum detectable magnetic field can reach as small as 1mT.In the future, more elaborate offset cancellation techniques and higher order ΔΣ modulation can be included to enhance the resolution of the MDC system.

6. References

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