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Multimedia ASIP SoC Codesign Based on Multicriteria Optimization

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ABSTRACT

This paper presents how to codesign a multimedia ASIP (Application Specific Integrated Processor) SoC (System-on-Chip) to achieve a low-power and high-throughput goal for a consumer device. The codesign methodology applies Pareto's Multicriteria Optimization technique to analyze and partition the software/hardware, the instruction set and the memory hierarchy of an ASIP to provide a flexible approach of finding the best trade-off between conflicting goals based on a given weight function.

INTRODUCTION

Mobile devices will play an important if not the dominant role in future consumer electronics. The best present example for this kind of device is the cellular phone. However in the future, those devices are expected to have significantly improved multimedia capabilities. In addition they must be small, flexible and consume little power. Therefore, application-specific integrated processors (ASIP) will be a key element of those devices. Unfortunately, the goal of concurrently minimizing power consumption and maximizing throughput cannot be achieved easily as both objectives may contradict each other. For example, the battery of the commercial handheld computer usually lasts for 15 hours but less than 3 hours when connecting to the Internet. In our paper we present a codesign methodology that uses multicriteria optimization to analyze and partition the software/hardware, the instruction set and the memory hierarchy of an ASIP to provide a flexible approach of finding the best trade-off between conflicting goals based on a given weight function.

Application-specific instruction set design is an important component of an embedded consumer device system [1] [2] [3]. It has always been addressed from the viewpoint of the ALU while the memory hierarchy was ignored. But comparing the ($P_{MU}D_{MU}/P_{ALU}D_{ALU}$) ratios in Table 1 with P and D denoting "power" and "delay" and being modeled in [5] and [4], respectively, it shows that the memory hierarchy features [4] dominate the final cost and performance. This paper proposes the eDLX architecture to implicitly embed the memory load/store instructions implicit into the instruction addressing modes, if possible. Then the approximate improvements (upper bounds) for six client multimedia applications [3] plus the web server "HTTPD_1.52a." are given.

MULTICRITERIA OPTIMIZATION

Pareto's MO (Multicriteria Optimization) technique maps the feasible domain in the design space into the criterion space, and computes the optimal design entry point based on the weighting objective function [7]. Two parameter groups are given for the two-level codesign MO process, see Table 1. They determine whether the process is backward compatible. The data of the first group extracted by the Sparc Architecture simulator (SAS) are analyzed for backward compatible ISA (Instruction Set Architecture), and the latter group, obtained by the GNU debugger, is for incompatible ISA. Three transformational strategies [5] are applied to the seven design candidates [3] shown in Table 2 and Fig. 1. The first is the MU optimization by RAM resource utilization such as using SRAM or embedded DRAM as main memory. The second is the ALU optimization by operation reduction and by operation substitution, e.g. SETHI (set high immediate) and emulated multiplier strategies. The final strategy is the large register memory exploited in the proposed eDLX structure. The results show that, in general, memory technology dominates the optimal trade-off. Further, ALU improvement has a significant impact on some applications, for example, Gsm requires 60% of the total execution time of multiplication. Group 2 exploits the mature on-chip SRAM technology, such as 4M bits CMOS SRAM with < 10 nanosecond access time [8], to incorporate three 512K-to-19 memory addressing encoding fields into one instruction. For all applications together an estimated average speedup of 1.74 and power saving of 78.21% is achieved.

THE PROPOSED eDLX SoC

Figure 2 presents the proposed eDLX architecture that constructs a large register file for the virtual (data+stack +execution) size and a library cache memory for the C library (libc.so.x). This design decodes the 512KB-register memory in every ALU instruction and eliminates unnecessary load/store instructions. It prevents pipelined load stalls while increasing the clock cycle time for large SRAM register file access. The result shows that the transferring application pair (wget and httpd) runs faster than the other encoding/decoding applications.

CONCLUSION

This paper provides an alternative method to design a future ASIP SoC suitable for multimedia applications. By incorporating the very compact embedded Linux OS, the whole multimedia system will achieve a low-power and high-throughput requirement.

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Table 1: Parameters for Codesign Analysis

Multimedia Application Benchmarks	Parameter Group #1 for Instruction Distribution				Parameter Group #2 for Memory Distribution			
	$\frac{P_{MU}D_{MU}}{P_{ALU}D_{ALU}}$	Mem%	Sethi%	Mul%	VmData	VmStk	VmExe	VmLib
Compress	177.3	36.27	7.66	0	424	8	12	1012
Gzip	549.3	46.03	4.35	0	336	8	44	1012
Wget	306.0	32.30	4.51	2.92	60	16	80	1240
Tar	362.8	35.32	5.50	0.52	60	20	104	1044
Gsm	49.7	20.27	3.06	60.4	20	8	44	1012
Mpeg	528.3	43.80	4.73	5.32	128	8	40	1120
Httpd	511.2	44.66	1.46	0	624	44	96	1176
Average	354.9	36.95	4.47	9.83	236	16	60	1088
Maximum	549.3	46.03	7.66	60.4	624	44	104	1240

p.s.: Mem%, Sethi% and Mul% indicates the percentages of the memory access, SETHI and multiply instructions.

Table 2: Transformation results for seven communication applications.

	compress		gzip		wget		tar		gsm		mpeg		httpd		Average	
	P(mW)	ΔD%	P(mW)	ΔD%	P(mW)	ΔD%	P(mW)	ΔD%	P(mW)	ΔD%	P(mW)	ΔD%	P(mW)	ΔD%	P(mW)	ΔD%
1	5.965	0	8.521	0	6.189	0	6.819	0	3.853	0	8.167	0	6.752	0	6.752	0
2	4.216	66.68	5.998	77.30	4.364	57.93	4.400	63.91	2.74	35.84	5.862	79.82	4.597	63.58	4.597	63.58
3	5.965	-18.14	8.521	-21.84	6.189	-15.97	6.819	-17.62	3.853	-9.8	8.167	-21.52	6.586	-17.48	6.586	-17.48
4	5.900	-8.29	8.515	-4.55	6.182	-4.72	6.811	-5.82	3.851	-3.16	8.160	-4.97	6.570	-5.25	6.570	-5.25
5	5.965	-8.29	8.521	-4.55	6.189	-4.72	6.819	-5.82	3.853	-3.16	8.167	-4.97	6.586	-5.25	6.586	-5.25
6	5.965	0	8.521	0	6.330	-3.28	6.846	-0.56	7.090	-120.2	8.511	-6.12	7.211	-21.71	7.211	-21.71
7	1.073	-36.27	1.493	-46.03	1.554	-32.3	1.465	-35.32	2.593	-20.27	1.735	-43.8	0.983	-44.66	1.56	-36.95

Group #1. 1: Original architecture(SPARC V7) 2: SRAM strategy
3: Embedded DRAM strategy 4: Word-length extension strategy (SETHI)
5: Half address space strategy (SETHI) 6: Multiplier strategy (SPARC V8)
Group #2 7: Large register-file strategy

Fig. 1: MO criterion space for seven multimedia applications.

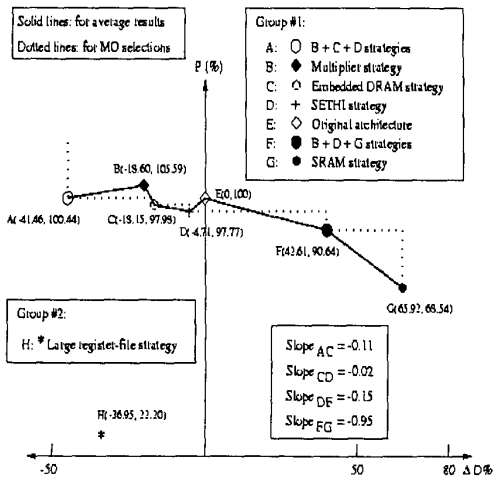

Fig. 2: Pipelined eDLX architecture design.