Analysis of On-Chip Spiral Inductors Using the Distributed Capacitance Model

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Abstract

The characteristics of on-chip inductors such as the S parameter, the quality factor (Q), and the self-resonant frequency (f_{SR}) can be determined by its series inductance, equivalent capacitance, and series resistance. In this paper, the distributed capacitance models have been developed to predict the equivalent capacitances of the on-chip spiral inductors such as planar and stacked inductor. Based on the equivalent capacitances formulas, a simple accurate methodology is proposed to build a compact model to predict the behaviors of on-chip inductors. A large amount of inductors have been implemented in 0.25-μm and 0.35-μm CMOS processes to demonstrate the prediction accuracy.

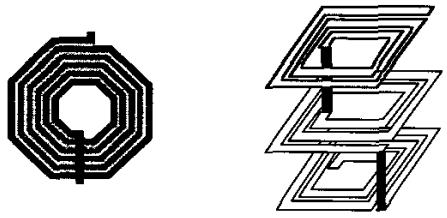
I. Introduction

Accurate inductor simulation enables accurate RF circuit simulations such as the noise figure of low-noise amplifiers [1], the phase noise of oscillators [2] or the power-added efficiency of power amplifiers. With more and more metal layers available, the stacked inductor, which consists of the series connected spiral inductors, is developed to reduce the area occupied by the planar inductors. Most of on-chip inductor simulators are electromagnetic field (EM) simulators to predict its behaviors such as S parameter and Q. Whatever the EM simulators are very time-consuming, and they don't have insight to optimize the inductor design.

Until now the on-chip inductor model given by the foundries still focus on the fitting equations of some parameters such as L_S. In this paper, the distributed capacitance models (DCM) [3] of on-chip inductors are developed to estimate the equivalent capacitances. For the series resistance R_S, the second order empirical expression is derived from test-keys or measured S parameter provided by the foundries to represent high-frequency magnetic effects. Based on the theoretical derivation of equivalent capacitances and empirical expression of R_S, the S parameter, the f_{SR} and the Q of the on-chip inductors can be predicted. Finally, the experimental results demonstrate the prediction accuracy. In Section II, the characteristics of the monolithic inductors such as Q and f_{SR} are briefly discussed. Section III introduces the distributed capacitance model to calculate the C_p, C_{sub}, and R_S in on-chip inductors. According to the calculations of C_p, C_{sub}, R_S, and L_S, the compact inductor model can be built to predict the behaviors of the on-chip inductors. In Section IV, equivalent capacitance formula validations are summarized. The predictions of the S parameter, the f_{SR} and the Q, which are simulated in accordance to the compact inductor model, are also demonstrated with measurement results in the section. Finally, conclusions are given in Section V.

II. Characteristics of On-Chip Inductor

The shapes of spiral inductors can be square, octagonal, or circular. These different shaped monolithic inductors can be implemented with a single metal layer or multi metal layers, as shown in Fig. 1 respectively. These monolithic inductors can be simply modeled as Fig. 2, where L_S is the inductance, R_S is the series resistance, C_p is the equivalent inter-winding capacitance, C_{sub} is the equivalent capacitance between the metal track and the substrate, and R_{sub} represent the substrate resistance.



(a) (b)

Fig. 1. (a) Planar (b) Stacked inductors.

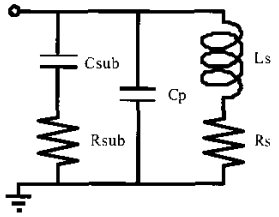


Fig. 2. Compact on-chip inductor model.

The one-port S parameter can be calculated as

$$S_{11,1-port} = \frac{Z_L - Z_0}{Z_L + Z_0} \quad (1)$$

, where Z_0 is given as the source impedance, which is usually 50 ohm, and Z_L is given as the impedance of the on-chip inductor.

The Q of an inductor is an important parameter, which significantly affects the performances of the RF circuits and systems, thus the Q is the most commonly quoted as performance parameter of an inductor. The f_{SR} can be defined as the frequency while the Q drops to zero, and the impedance of the inductor becomes capacitive if the operation frequency exceeds f_{SR}, The Q of the on-chip

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inductor can be defined as

$$Q = 2\pi \cdot \frac{peak\ magnetic\ energy - peak\ electric\ energy}{energy\ loss\ in\ one\ oscillation\ cycle} = \frac{\mathrm{Im}(Z_L)}{\mathrm{Re}(Z_L)} \quad (2)$$

III. Compact Inductor Model

Z_L can be determined by inductor parameters such as L_S, R_S, C_p, C_{sub}, and R_{sub}. The series inductance has been surveyed for a long time, and there are many methodologies to calculate L_S such as Greenhouse's formula, empirical expressions, electromagnetic field solvers, or *ASITIC* [4].

A. Equivalent Capacitance Formulas

In order to investigate the C_p and C_{sub} in on-chip inductors, we use the DCM to approximately estimate. For simplicity, the following assumptions are made:

1. Assume that the wiring metal width is much larger than the spacing, i.e. when one calculates inductor's area and length, one can ignore spacing.
2. Voltage distribution is proportional to the lengths of the metal tracks, i.e. if the metal track is longer, the voltage drop on the track is larger.
3. In the same turn, the voltage is equal and it is determined by averaging the beginning voltage and the ending voltage of the turn.

In order to generalize the equivalent capacitance formula, suppose that a planar inductor has inner radius r, metal width w, and n turns in m-th metal layer and a m-layer stacked inductor has inner radius r, metal width w, and n turns in each layer. The voltage profile across the m-th metal layer planar inductor is shown in Fig. 3.

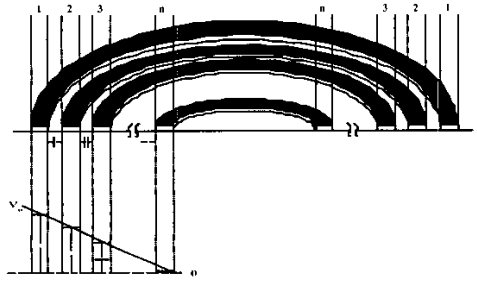

Fig. 3. Voltage profile of the n-turn planar inductor.

First the lengths of each turn are defined as l_1, $l_2 \ldots l_n$, respectively and the total length is defined as $l_{tot}=l_1+l_2+\ldots+l_n$. Each track area is defined as A_1, $A_2 \ldots A_n$, respectively, from 1st turn to n-th one.

For the planar inductor on the m-th metal layer, the beginning voltage $V(k)_{beg}$ and the ending voltage $V(k)_{end}$ of the k-th turn can be expressed as

$$V(k)_{beg} = V_0(1 - (h_1 + h_2 + \ldots + h_{k-1})) \quad (3)$$

$$V(k)_{end} = V_0(1 - (h_1 + h_2 + \ldots + h_{k-1} + h_k)) \quad (4)$$

, where $h_k \equiv (l_k / l_{tot})$.

According to the assumption *3*, the voltage of the k-th turn in the m-th metal layer can be derived as

$$\begin{aligned} V(k) &= \frac{1}{2}[V(k)_{beg} + V(k)_{end}] \\ &= \frac{1}{2}V_0[2 - (h_1 + h_2 + \ldots + h_{k-1}) - (h_1 + h_2 + \ldots + h_k)] \\ &= \frac{1}{2}V_0[2 - d(k-1) - d(k)] \end{aligned} \quad (5)$$

, where $d(k) \equiv h_1 + h_2 + \ldots + h_{k-1} + h_k$.

So, the electrical energy stored in the capacitor between the m-th metal layer and the substrate of the k-th turn can be expressed as

$$\begin{aligned} E_{c,ms}(k) &= \frac{1}{2}C(k) \cdot V(k)^2 \\ &= \frac{1}{2}C_{ms}A_k \cdot V(k)^2 \end{aligned} \quad (6)$$

, where C_{ms} represents the capacitance per unit area between the m-th metal layer and the substrate. The voltage drop between the k-th and $(k+1)$-th turn can be expressed as

$$\begin{aligned} \Delta V(k,k+1) &= V(k) - V(k+1) \\ &= \frac{1}{2}V_0[d(k+1) - d(k-1)] \end{aligned} \quad (7)$$

Thus the electrical energy stored in the capacitor between the k-th and $(k+1)$-th turn can be expressed as

$$\begin{aligned} E_{c,mm}(k) &= \frac{1}{2}C(k) \cdot \Delta V(k,k+1)^2 \\ &= \frac{1}{2}C_{mm}l_k \cdot \Delta V(k,k+1)^2 \end{aligned} \quad (8)$$

, where C_{mm} represents the capacitance per unit length between adjacent metal layers. The electrical energy stored in the equivalent capacitor of the inductor is simply divided into two parts: one is in metal-to-metal capacitor and the other is in metal-to-substrate capacitor, and it can be shown as

$$\begin{aligned} E_{c,total} &= \frac{1}{2}C_{eq}V_0^2 \\ &= \frac{1}{2}C_pV_0^2 + \frac{1}{2}C_{sub}V_0^2 \\ &= E_{c,metal-metal} + E_{c,metal-sub} \\ &= \sum_{k=1}^{n-1} E_{c,mm}(k) + \sum_{k=1}^{n} E_{c,ms}(k) \end{aligned} \quad (9)$$

Based on eq. (9), the equivalent capacitance, C_p and C_{sub}, of the planar inductor can finally be expressed as

$$\begin{aligned} C_p &= \sum_{k=1}^{n-1}\frac{1}{4}C_{mm}l_k[d(k+1) - d(k-1)]^2 \\ C_{sub} &= \sum_{k=1}^{n}\frac{1}{4}C_{ms}A_k[2 - d(k-1) - d(k)]^2 \end{aligned} \quad (10)$$

Referring to eq. (9), the total equivalent capacitance of the

planar inductor can be expressed as

$$C_{eq}=\sum_{k=1}^{n-1}\frac{1}{4}C_{mm}l_k[d(k+1)-d(k-1)]^2+\sum_{k=1}^{n}\frac{1}{4}C_{mx}A_k[2-d(k-1)-d(k)]^2 \tag{11}$$

Applying the same concepts to m-layer stacked inductor and referring to Fig. 1(b), the voltage profile across the stacked inductor is shown in Fig. 4, and the equivalent capacitance, C_p and C_{sub}, can be calculated as:

$$\begin{aligned}C_p&=\sum_{k=1}^{n}\frac{1}{4}\{C_{m,m-1}+C_{m-2,m-3}+\ldots+C_{3,2}\}A_k[\frac{4}{m}-\frac{2}{m}d(k)-\frac{2}{m}d(k-1)]^2\\&+\sum_{k=1}^{n}\frac{1}{4}\{C_{m-1,m-2}+C_{m-3,m-4}+\ldots+C_{2,1}\}A_k[\frac{2}{m}d(k)+\frac{2}{m}d(k-1)]^2\\C_{sub}&=\sum_{k=1}^{n}\frac{1}{4}C_{1,x}A_k[\frac{1}{m}d(k-1)+\frac{1}{m}d(k)]^2\end{aligned} \tag{12}$$

Thus the total equivalent capacitance of the m-layer stacked inductor can be given as

$$\begin{aligned}C_{eq}&=\sum_{k=1}^{n}\frac{1}{4}\{C_{m,m-1}+C_{m-2,m-3}+\ldots+C_{3,2}\}A_k[\frac{4}{m}-\frac{2}{m}d(k)-\frac{2}{m}d(k-1)]^2\\&+\sum_{k=1}^{n}\frac{1}{4}\{C_{m-1,m-2}+C_{m-3,m-4}+\ldots+C_{2,1}\}A_k[\frac{2}{m}d(k)+\frac{2}{m}d(k-1)]^2\\&+\sum_{k=1}^{n}\frac{1}{4}C_{1,x}A_k[\frac{1}{m}d(k-1)+\frac{1}{m}d(k)]^2\end{aligned} \tag{13}$$

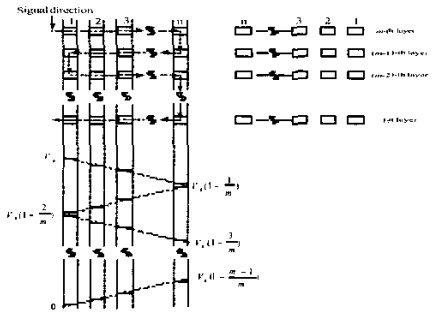

Fig. 4. Voltage profile of the m-layer n-turn stacked inductor.

B. Series Resistance Formula

Series resistance, R_S, involves in many complicated effects such skin effect, magnetic substrate coupling, and eddy currents in the inner tracks. The interactions of these magnetic effects are too complex to be analyzed analytically, therefore the possible solutions to predict the high-frequency series resistance are EM simulation or empirical equation. In this paper, we make use of the empirical equation to express these magnetic effects on series resistance. The empirical equation can be given as

$$R_S = R_{DC}(1 + A \cdot f + B \cdot f^2) \tag{14}$$

, where R_{DC} is dc resistance, A, B are process-dependent parameters, and $f$represents the frequency in GHz. Now the foundries have been provided measured inductor data with different configurations, and the empirical parameters, A and B, can be extracted from the measured data. Table I shows the empirical parameters with different processes and configurations.

TABLE I.

Empirical parameters with different processes and configurations

Process	Configuration	A	B
0.35-μm	octagonal, planar	0.100	0.010
0.35-μm	circular, stacked	0.160	0
0.25-μm	16-sided, planar	0.155	0.135

IV. Model Validation

In order to verify the accuracy of the compact model, the behaviors of the compact model are compared to measurement data. A large amount of planar and stacked inductors have been fabricated in a 0.35-μm 1P4M and 0.25-μm 1P5M CMOS processes. The prototype chips also include the de-embed pads to calibrate the pad parasitic capacitance.

A. Equivalent Capacitance Formula Validation

The self-resonant frequency of an inductor can be determined as $f_{SR}=(2\pi\sqrt{L_S C_{eq}})^{-1}$. In corporation with inductance calculation methodology provided by foundry or simulator such as *ASITIC*, eqs. (11) and (13) can be applied to predict the f_{SR}. Table II shows the measured equivalent capacitance and simulated equivalent capacitance of planar and stacked inductors to demonstrate the accuracy of eqs. (11) and (13). The C_{eq} prediction error is less than 8%. The f_{SR} prediction error is less than 5%.

B. S parameters Validation

For 0.35-μm and 0.25-μm CMOS processes, as examples, the substrate resistance is about 200 ohms. Fig. 5 shows the simulated and measured S11 of the 0.35-μm planar inductor with r=70μm, w=10μm, and n=3. Fig. 6 shows the simulated and measured S11 of the 0.35-μm stacked inductor with r=30μm, w=10μm, and n=2. The other simulated S11, whose equivalent capacitance is directly calculated without DCM, shows significant deviation from measured one.

TABLE II.

The C_{eq} and f_{SR} of planar and stacked inductors in 0.35-μm (w = 10μm, $sp.$ = 1μm) and 0.25-μm CMOS processes. (w = 15μm, $sp.$ = 2.2μm)

Ind. Configuration	L(nH)	Inner r	Turns	Mea. C_{eq} (fF)	Sim. C_{eq}(fF)	C_{eq} Error	Mea. f_{SR} (GHz)	Sim. f_{SR} (GHz)	f_{SR} Error
0.35-μm Planar	3.4	70	3	47.6	44.1	7.3%	12.5	13.0	4.0%
0.35-μm Planar	4.0	50	4	47.9	45.8	4.5%	11.5	11.7	2.1%
0.25-μm Planar	3.6	90	3	31.7	30.8	2.8%	14.9	15.1	1.3%
0.25-μm Planar	4.3	100	3	35.4	34.3	3.1%	12.9	13.1	1.6%
0.35-μm Stacked	7.3	30	2	54.2	52.4	3.3%	7.8	8.2	5.1%

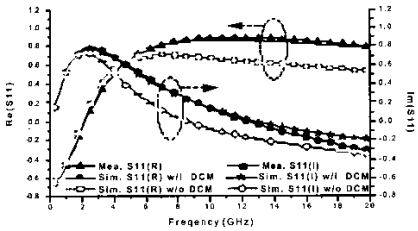

Fig. 5. Measured S parameter and simulated ones with/without DCM of the 0.35-μm 3.4nH planar inductor.

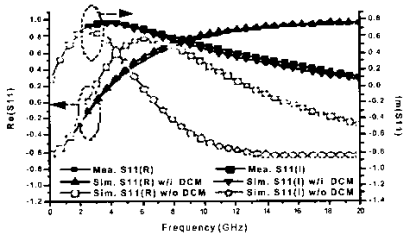

Fig. 6. Measured S parameter and simulated ones with/without DCM of the 0.35-μm 4.9nH stacked inductor.

C. Q-Factor Computation and Comparison

Traditionally Q can be computed by EM simulator, but it will take long time while sweeping frequency and the result is different from the measured Q significantly. According to the compact inductor model and eq. (2), the Q of the compact model such as planar or stacked inductor can be computed and are compared to the measured one. Fig. 7 shows the simulated and measured Q of the 0.35-μm planar inductor with r=70μm, w=10μm, and n=3. Fig. 8 shows the simulated and measured Q of the 0.35-μm stacked inductor with r=30μm, w=10μm, and n=2. It shows good agreements between the measured and simulated Q based on the distributed capacitance model, and the other simulated Q, whose equivalent capacitance is directly calculated, shows significant deviation from measured one. Table III shows the measured Q and simulated ones with/without the distributed capacitance model of planar and stacked inductors to demonstrate the accuracy.

V. Conclusion

In this paper, analytical equations to predict the equivalent capacitance in on-chip inductors such as planar and stacked inductors are derived. The C_{eq} prediction error is less than 8%. In corporation with inductance calculation, the self-resonant frequency can be predicted and the f_{SR} prediction error is less than. 5%.

Based on the analytical equations, a general approach to modeling on-chip inductors is proposed. The predictions of the models such S parameters and Q factor agree well with the measured ones. The Q prediction error is less than 7% @2.4GHz. The simple methodology not only provides accurate inductor simulation but also saves design time.

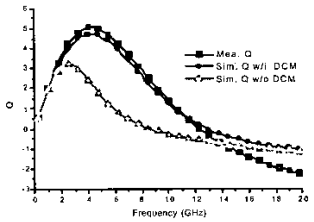

Fig. 7. Measured Q and simulated ones with/without DCM of the 0.35-μm 3.4nH planar inductor

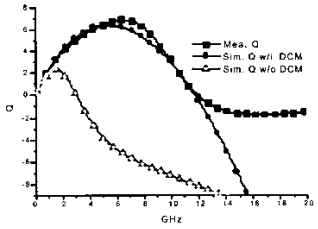

Fig. 8. Measured Q and simulated ones with/without DCM of the 0.35-μm 4.9nH stacked inductor

VI. References

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TABLE III.

The mea. and sim. Q of planar and stacked inductors in 0.35-μm (w = 10μm, $sp.$ = 1μm) and 0.25-μm CMOS processes (w = 15μm, $sp.$ = 2.2μm) @2.4GHz.

Ind. Configuration	L(nH)	Inner r	Turns	Mea. Q	Sim. Q w/i DCM	Error	Sim. Q w/o DCM	Error
0.35-μm Planar	3.4	70	3	4.23	3.95	6.6%	3.19	24.6%
0.25-μm Planar	4.3	100	3	8.25	8.34	1.1%	6.47	21.5%
0.35-μm Stacked	7.3	20	2	4.42	4.70	6.3%	1.43	67.6%