DESIGN OF A DMT-BASED BASEBAND TRANSCEIVER FOR VERY-HIGH-SPEED DIGITAL SUBSCRIBER LINES

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ABSTRACT

In this paper, we propose a transceiver design for the ETSI VDSL standard that uses the discrete multi-tone (DMT) modulation. Algorithms for channel estimation/equalization, symbol synchronization, sampling clock tracking are designed and integrated into the receiver architecture. Fixed-point simulation of the whole system shows that the proposed receiver architecture is capable of very high-rate transmission in digital subscriber loop channels.

1. INTRODUCTION

With rapidly growing demand for high-speed data transmission, especially in the application of net-meeting, video on demand, video phone, etc, the digital subscriber lines (DSL) technology is proposed to achieve broadband access by transmitting data over existing telephone network instead of using fiber all the way to the customers' residence. There have been many research efforts on providing efficient and reliable high-data-rate access services by subscriber lines, such as ADSL and HDSL, which provide a download data rate of no more than 6 Mbps. Recently, the European Telecommunication Standard Institute (ETSI) finalized the Very-high-rate DSL (VDSL) standard to provide high-speed transmission over digital subscriber lines [1]. There are two possible modulation schemes, single-carrier based and multi-carrier based. The data rates of the VDSL are ten times that of the ADSL and therefore this new standard is capable of providing almost all multimedia communication services.

The paper first introduces the basic idea of discrete muti-tone (DMT) and some important parameters defined in the ETSI VDSL standard. Next, the proposed receiver architecture will be described. All the impairments in typical subscriber lines defined in standard are properly dealt with to minimize the degradation they may be brought to system performance. A system made up of a standard-compatible transmitter model, a subscriber line channel model, and the proposed receiver model is designed and simulated. Whole system performance is evaluated in terms of simulated bit error rate (BER), as specified in the standard. Integrated circuit (IC) implementation will be shown in Section 6. Finally, Section 7 concludes this paper.

2. DMT-BASED VDSL OVERVIEW

Recently, multi-carrier modulation (MCM) has received a great deal of attention. One promnent MCM scheme is orthogonal frequency division multiplexing (OFDM) which has been adopted in many new-generation wideband data wireless communication systems, such as digital audio broadcasting (DAB), digital video broadcasting (DVB), high-speed wireless LAN (IEEE 802.11a). Discrete muti-tone differs from OFDM only in that different constellation sizes can adopted in each sub-carrier. The basic principle of DMT is to split the transmission binary data into several parallel data streams and transmit each of them on a separate subchannel using different constellation to optimize utilization of the spectrum. Each subchannel uses a sub-carrier overlapping but orthogonal to the others to reduce inter-carrier interference (ICI). A DMT symbol usually lasts longer than channel impulse response, therefore inter-symbol interference (ISI) can be dealt with by inserting a guard interval between two consecutive DMT symbols. The equalization effort is manageably simple since each subchannel is narrowband.

Table 1 lists several key parameters in the ETSI VDSL standard. The guard Interval duration is 20 μs, which is long enough to cover ISI in subscriber lines less than 1500 meters. In the beginning of system initialization, there are O-P-TRAINING type symbols for symbol synchronization, timing offset estimation/ compensation, one O-P-SYNCHRO type symbol to start channel estimation, and O-P-MEDLEY type symbols provides sufficient information for channel estimation.The receiver exploits these predetermined sequences to conduct channel estimation and achieve proper initialization. Among the 4096 used subchannels, there are 2 pilot subchannels used to assist the timing tracking task during normal data transmission. To avoid near-end crosstalk, which is hard to eliminate, the VDSL standard adopts a frequency-division multiplexing (FDD) method. Figure 1 illustrates the VDSL band allocation [1]. There are two possible band allocation schemes and they are listed in Table 2.

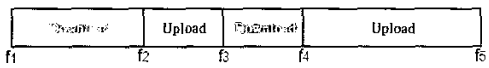

Figure 1: VDSL band allocation.

3. TRANSMITTER ARCHITECTURE

Figure 2 shows a VDSL transmitter architecture. The scrambler is used to reduce the likelihood of a long sequence of zeros or ones. The convolutional interleaver makes burst errors distributed among different Reed-Solomon codewords so as to enhance error-

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Table 1: Parameters in ETSI VDSL standard.

Number of Sub-carrier	256, 512, 1024, 2048, 4096
Cyclic Prefix Length	40, 80, 160, 320, 640
Sub-carrier Spcaing	4.3125 kHz
Constellation	BPSK up to 32768 QAM
Symbol Duration	250 μs
Guard interval	19.5 μs
Duplex Scheme	FDD
Signal Bandwidth	12 MHz
FEC	Reed-Solomon code should support (N,k)= (144,128) and (240,224)
Required BER	$< 10^{-7}$

Table 2: Band transition frequencies.

Band transition frequencies(kHz)	f1	f2	f3	f4	f5
VDSL bands	138	3000	5100	7050	12000
Optional region-specific bands	138	3750	5200	8500	12000

correcting capability. At initialization, control information is transmitted in the lower data path. The pseudo-random bit generator and rotator reduce the time-domain peak-to-average-power problem in the training sequence and thus make channel estimation more robust.

4. RECEIVER ARCHITECTURE

In a DMT receiver, in addition to the FFT operation that transforms the received time-domain signal to the frequency domain, channel impairments must also be estimated and properly dealt with. The DSL channels suffer from crosstalk, additive noise, and radio frequency interference (RFI) including broadcast RF interference and amateur RF interference [2, 1, 5]. The receiver also suffers from the timing offset due to oscillator mismatch. Figure 3 shows the proposed receiver architecture. In the following, several signal processing techniques used in the proposed receiver will be discussed.

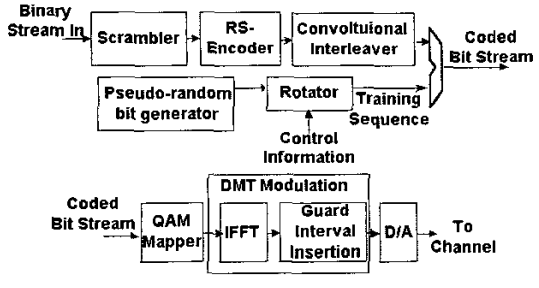

Figure 2: Transmitter architecture.

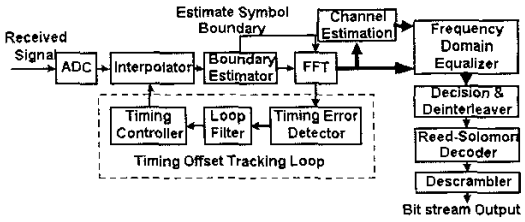

Figure 3: Receiver architecture.

4.1. Symbol Boundary Estimation

Since the cyclic prefix of each DMT symbol is an interval of repeated signal from previous time, a delay correlator is employed to estimate the symbol boundary. This correlator correlates the received signal with itself delayed by some times. The correlator output can be formulated as

$$CS(i) = \sum_{n=0}^{Ng-1} r_{i+n}\, r_{i+n+N}, \qquad (1)$$

where r_i are the received signal samples, N is the size of FFT, and Ng is the cyclic prexfix length. Once the correlator output exceeds a pre-defined threshold, the receiver announces detection of an incoming DMT symbol. The point where the maximum in the correlator output occurs is a coarse index of the symbol boundary. With other sophisticated algorithms, the actual symbol boundary can be estimated.

4.2. Timing Offset Estimation and Compensation

After locating symbol boundary, the next task is to estimate the timing offset and compensate for it. Since the ADC is running freely, there are two problems that need be addressed. At First, the sampling clock phase in the receiver is different from that in the transmitter, which causes additional constant phase rotation. Secondly, the sampling frequency is different between the transmitter and the receiver due to oscillator mismatch and this may cause a fix-rate phase rotation.

To recover the sampling clock offset, a digital timing recovery loop, which consists of a timing error detector, a loop filter, a timing controller, and an interpolator, is employed in the proposed receiver. There are two pilot subcarriers for sampling clock offset estimation during normal data transmission. The estimated timing error in the nth symbol is given by [6]

$$e_l(n) = \sum_{k,\,l} (\angle \hat{X}_{n,\,k} - \angle \hat{X}_{n,\,l}) - (\angle \hat{X}_{n-1,\,k} - \angle \hat{X}_{n-1,\,l}), \qquad (2)$$

where the primary pilot tone (k) is chosen as 600 due to robustness through all channel scenarios and the secondary tone (l) is adjustable to get better result in different channels. The two dominant factors of performance are loop parameters and robustness of the pilot. The loop parameters need to be tuned carefully. Robustness of the pilot can be guaranteed by using pilot tone 600 and a monitoring device that decides the secondary pilot according to channel conditions.

4.3. Channel Estimation

One of the advantages of OFDM lies in its flexibility to adopt either time-domain equalizer (TEQ), or frequency-domain equalizer (FEQ), or a combination of both [4, 7]. The time-domain equalizer (TEQ) is not necessary in the VDSL due to the long gard interval. According to our simulation, eliminating TEQ causes only trifling increase of BER but remarkable complexity reduction. Therefore, instead of performing equalization in the time domain, the proposed receiver compensates the channel response in the frequency domain, which requires less computation.

During the initialization procedure, the training sequence carries predetermined QPSK modulated signals on the 4096 subcarriers, which can be used for estimating the channel frequency response. Channel estimation and correction can be modeled as

$$Y_k = H_k \cdot X_k + I_k, \tag{3}$$

where X_k is the known kth subcarrier signal; Y_k is the received kth subcarrier signal. H_k is the channel frequency response on the kth subcarrier; and I_k is the channel impairments on the kth subcarrier. Then, the inverse channel frequency response estimation on subcarrierl k is given by

$$\hat{G}_k = \frac{X_k}{Y_k}. \tag{4}$$

It requires more accurate channel estimation to transmit complicated constellation. An adaptive FEQ is adopted in the proposed receiver architecture. The coefficient updating procedure is based on the least mean squared-error (LMS) algorithm, formulated as

$$\hat{G}_{n+1,k} = \hat{G}_{n,k} + \mu Y_{n,k} \cdot e_{n,k}. \tag{5}$$

where $Y_{n,k}$ is the error between actual signals $X_{n,k}$ and the equalized signals $\hat{X}_{n,k}$.

$$e_{n,k} = X_{n,k} - \hat{X}_{n,k} = X_{n,k} - \hat{G}_{n,k} \cdot Y_{n,k}. \tag{6}$$

4.4. Bit allocation

The other advantage of the DMT system is flexible bit allocation in different subcarriers to make optimized utilization of channel spectrum. For a fixed bit rate, the best bit allocation can be derived using the water-pouring algorithm. Since the channel response can be estimated, this information can be used to decide bit allocation by a table look up operation or more complicated algorithms to squeeze more bits.

5. FIXED POINT SIMULATION RESULTS

A system made up of the proposed transceiver architecture and DSL channel model specified in the ETSI VDSL standard [2] is built. Figure 4 illustrates the simulation model. Note that sampling clock offset is set as 100 ppm of the sampling clock frequency.

Whole system simulation using fixed-point arithmetic was conducted. An example of equalized 2048-point constellation extracted from simulation is plotted in Figure 5. The bit error rate (BER) under different channel conditions is also evaluated. The required bit rate and BER can be achieved in all cases simulated. The optimal bit allocation and achieved bit rate and BER are listed in Table 3. The BER settles down to below the required BER after 0.2s of normal data transmission, during which interval the FEQ adapt to the optimal coefficient setting. The * in the table means optional regional-specific bands. The BER are calculated from the first time block average BER below 10^{-7} (the required BER). The total number of transmitted bits is 10^9, and no error can be detected once the FEQ has converged to its final state.

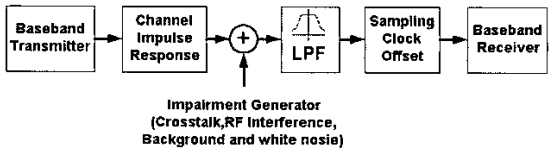

Figure 4: Model used in system simulation.

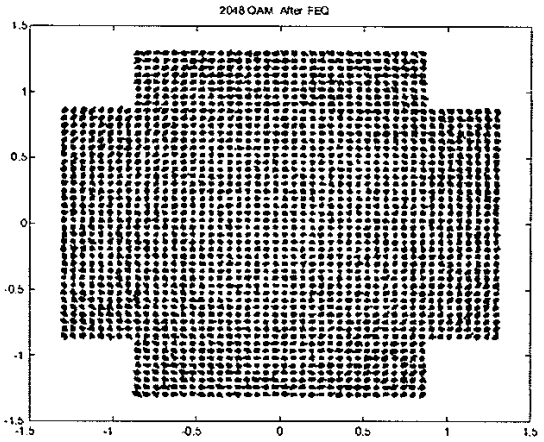

Figure 5: Equalized 2048 QAM constellation.

Table 3: Fixed Point Simulation Results.

Channel (meters)	Uncoded bit rate(Mbps)	Coded bit rate(Mbps)	BER
1500	16.2	14.4	$< 10^{-8}$
1000	25.2	22.4	$< 10^{-8}$
500	35.6	31.7	$< 10^{-8}$
300	40.9	36.5	$< 10^{-8}$
300 *	56.2	50.1	$< 10^{-8}$

6. ASIC IMPLEMENTATION

Figure 6 shows the block diagram of the proposed VDSL receiver. Due to their huge hardware complexity, the FFT block and several delay lines are not implemented in the chip. The VDSL receiver IC consists of baseband signal processing circuits including the symbol boundary estimation block, the digital timing recovery loop, the channel estimation and adaptive FEQ block. Figure 7 illustrates the diagram of the channel estimation and adaptive FEQ circuit. Verilog simulation results agree with those of the previous fixed-point C simulation.

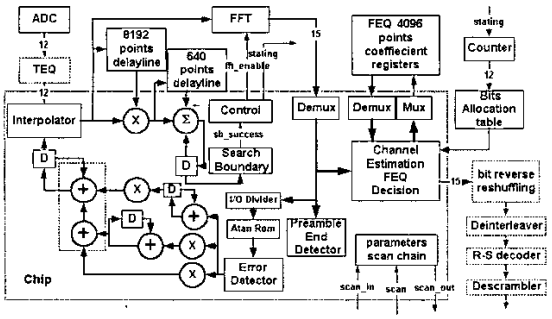

Figure 6: Block diagram of the proposed VDSL baseband receiver.

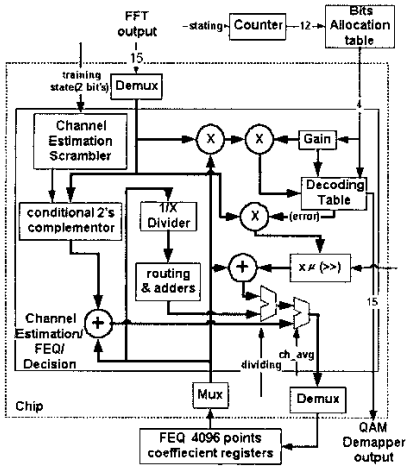

Figure 7: Diagram of the channel estimation and adaptive FEQ circuit.

Using a standard-cell design style and the gate-level design of the receiver in Figure 6, we have completed the physical design of the ASIC. The layout of the VDSL baseband receiver implemented in a 0.35-micron 1P4M CMOS technology is depicted in Figure 8. This IC has a core size of about 3mm x 3mm and contains about 238000 transistor and is expected to run at 35 MHz while consuming less than 300 mW from a 3.3V supply voltage.

7. CONCLUSION

In this paper, a DMT receiver architecture for VDSL is proposed. Many techniques, such as channel coding, channel estimation, and digital timing recovery are adopted to ensure functionality of the proposed receiver in the DSL environments. System performance of the proposed receiver is evaluated and it meets the BER specification in the ETSI VDSL standard. Circuit and physical layout design of the proposed receiver is completed and the IC will be fabricated in the near future.

Acknowledgements

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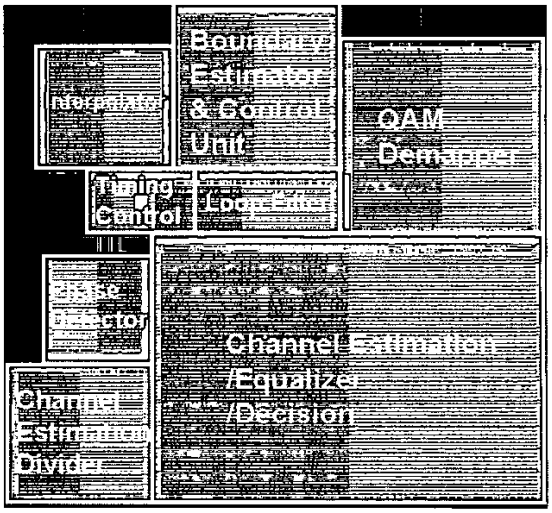

Figure 8: Layout of the proposed VDSL receiver IC.

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