

# CMOS 2.4 GHz receiver front end with area-efficient inductors and digitally calibrated 90° delay network

C.-H. Wu, C.-C. Tang, K.-H. Li and S.-I. Liu

**Abstract:** A 2.4 GHz CMOS Hartley image-reject receiver utilising the area-efficient inductors and a digitally calibrated 90° delay network is proposed. Compared with the conventional planar inductor, the proposed area-efficient inductor saves 80% of the silicon area without degrading the quality factor. In addition, employing the digitally calibrated 90° delay network rather than the RC–CR network can make the traditional Hartley receiver tolerant to temperature and process variations. A prototype chip with a fully integrated low-noise amplifier followed by the proposed image-reject mixer has been fabricated in a 0.35 μm single-poly–four-metal standard CMOS technology and the active area is 3.13 mm<sup>2</sup>. While operating at 2.4 GHz, this receiver achieves a 30 dB image-rejection ratio, a –3 dB third-order input intermodulation intercept point, and an 11 dB noise figure with 54 mW power consumption from a 3.3 V supply.

## 1 Introduction

Due to the tremendous demands of portable wireless devices, providing a low cost solution is becoming increasingly more important. For non-zero IF receiver systems, the image signal may corrupt the desired signal. Several new techniques and receiver architectures [1, 2] have been proposed to suppress the image signal.

In this work, the Hartley receiver [3] is studied because of its simpler architecture and lack of second image problem. Two main nonidealities cause the incomplete image cancellation. One is the gain and phase imbalances due to the inaccurate quadrature LO signals and mismatched I/Q signal paths. The other originates from the imperfect 90° shift network, which is implemented by a RC–CR network in practice. Due to process variations, the absolute values of resistors and capacitors in the RC–CR network cannot be well controlled by using only the simple circuit technique. Hence, we wished to develop an accurate shift-by-90° stage to replace the RC–CR network in the Hartley image-reject receiver.

Besides the architecture passive devices, such as the inductors, on the lossy substrate also significantly influence the performance of the receiver. Much effort has been put into increasing the quality factors of the on-chip inductors [4–6]. To reduce the on-chip inductor area, we propose a new configuration inductor, which is not only small in size but also has a quality factor comparable to that of the planar inductor.

## 2 Architecture

The Hartley image-reject receiver is shown in Fig. 1. This topology mixes the RF input signal with the quadrature LO signals and shifts the down-converted signal in one branch by 90°. The signals in these two branches are then added together to obtain the desired signal and cancel the image signal. In this technique, the amplitude and the phase mismatches between the quadrature LO signals cause the incomplete image cancellation. Given that the phase error is  $\phi$ , the image-rejection ratio (IRR) can be derived as [7]

$$IRR = \frac{(\Delta A_{LO}/A_{LO})^2 + \phi^2}{4} \quad (1)$$

where  $A_{LO}$  is the amplitude of the LO signal and  $\Delta A_{LO}$  is the amplitude difference between the quadrature LO signals. It should be noted that (1) is true only when the phase difference between these two signals (at points B and C) is 90°. In the traditional Hartley image-reject receiver, a RC–CR network is implemented to provide the 90° phase difference between the two signal paths. The simulation indicates that the magnitude responses of the two signal paths are equal only at the one frequency, which is specified by the RC constant. However, the on-chip passive devices, especially the resistors, often suffer from mismatches and inaccurate values due to the process variations. The mismatches of the resistors and capacitors between two signal paths introduce the magnitude and phase errors. It has been proved that slight deviations of resistance and capacitance will dramatically degrade the IRR [7].

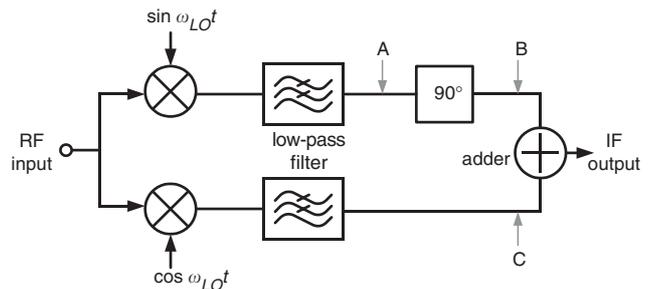


Fig. 1 Architecture of Hartley image-reject receiver

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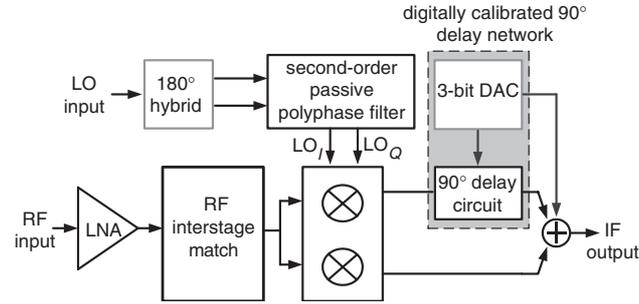
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Our proposed modified Hartley image-reject receiver architecture is shown in Fig. 2. It includes a low-noise amplifier, mixer, and the digitally calibrated 90° delay network, which consists of a 90° delay circuit and an off-chip 3-bit digital-to-analogue converter (DAC). This proposed circuit allows the system to adjust the 90° delay network to compensate for inaccurate delay results from the process variations.



**Fig. 2** Proposed image-reject receiver architecture with digitally calibrated 90° delay network

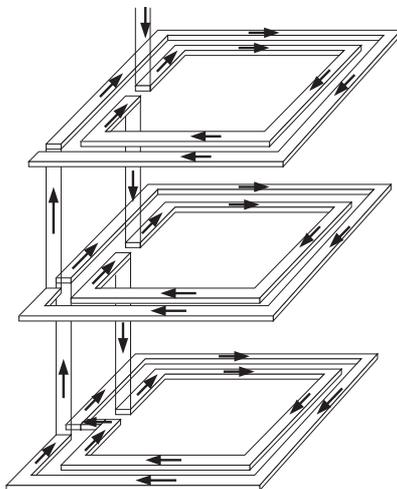
### 3 Circuit designs

#### 3.1 Area-efficient inductor

On-chip inductors usually occupy an enormous die area resulting in increased cost. An area-efficient inductor structure has been proposed to significantly minimise the size of the inductor without degrading its quality factor.

The conventional stacked inductor [8] consists of the series connected spiral inductors in the different metal layers. Every spiral inductor in the different metal layers may have the same or different turns. The wires wind downward from the top metal layer to the bottom one. Our proposed area-efficient inductor consists of at least two stacked inductors with series connections and every stacked inductor has only one turn in every metal layer. Figure 3 shows the structure of the proposed area-efficient inductor [9]. There are two advantages of this proposed area-efficient inductor: one is the small area, and the other is the higher self-resonance frequency  $f_{SR}$ . Compared with the planar inductor, the area-efficient inductor saves 80% of the die area without degrading the inductance and the quality factor. The  $f_{SR}$  of the area-efficient inductor is higher than that of a conventional stacked inductor [9].

To predict the performances, such as the quality factor ( $Q$ ) and the  $f_{SR}$ , of the area-efficient inductor, the equivalent



**Fig. 3** Architecture of the area-efficient inductor

capacitance and the series resistance have to be obtained. For simplicity, the following assumptions are made:

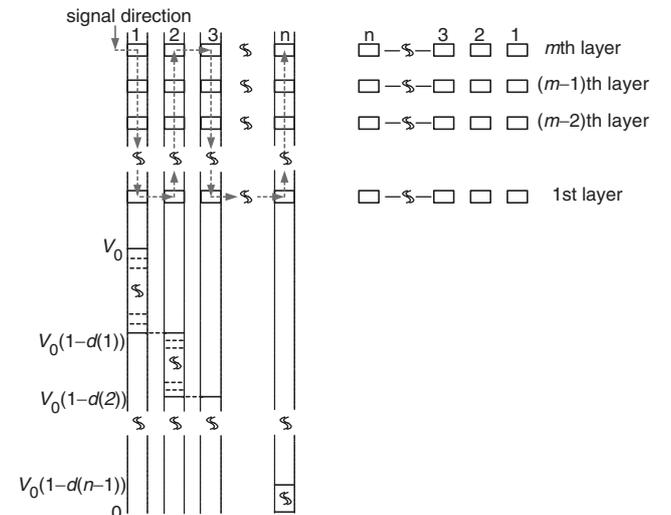
- (i) Assume the spacing between metal lines can be ignored because it is much smaller than the metal width;
- (ii) Voltage is constant in the same turn and it is determined by averaging the voltage of the previous and the next turn;
- (iii) Voltage drop is proportional to the length of the metal line.

Suppose we have an area-efficient inductor with inner radius  $r$ , metal width  $w$ , with  $n$  turns, and  $m$  layers. The lengths of turns  $1 \dots n$  are  $l_1, l_2, \dots, l_n$ , respectively, and the total length is  $l_{tot}$ .  $A_1, A_2, \dots, A_n$  represent the areas of the tracks from the first to the  $n$ th turn, respectively. The voltage profile of an  $m$ -layer  $n$ -turn area-efficient inductor is shown in Fig. 4. With tedious evaluation, the total equivalent capacitance of the area-efficient inductor can be obtained as

$$C_{eq} = \sum_{k=1}^n \{C_{m,m-1} + C_{m-1,m-2} + \dots + C_{2,1}\} A_k \left(\frac{l_k}{m}\right)^2 + C_{1,s} \{A_1(1 - l_1 + \frac{1}{2m}l_1)^2 + A_2(1 - l_1 - \frac{1}{2m}l_2)^2 + A_3(1 - l_1 - l_2 - l_3 + \frac{1}{2m}l_3)^2 + \dots\} \quad (2)$$

where  $C_{m,m-1}$  represents the capacitance per unit area between the  $m$ th and the  $(m-1)$ th layers and  $C_{1,s}$  is the capacitance per unit area between the lowest metal layer (metal layer 1) and the substrate. In the same manner, to analyse an  $m$ -layer  $n$ -turn conventional stacked inductor, the total equivalent capacitance is derived as

$$C_{eq,stacked} = \sum_{k=1}^n \frac{1}{4} \{C_{m,m-1} + C_{m-2,m-3} + \dots + C_{3,2}\} \times A_k \left[ \frac{4}{m} - \frac{2}{m}d(k) - \frac{2}{m} \right]^2 + \sum_{k=1}^n \frac{1}{4} \{C_{m-1,m-2} + C_{m-3,m-4} + \dots + C_{2,1}\} \times A_k \left[ \frac{2}{m}d(k) + \frac{2}{m}d(k-1) \right]^2 + \sum_{k=1}^n \frac{1}{4} C_{1,s} A_k \left[ \frac{1}{m}d(k-1) + \frac{1}{m}d(k) \right]^2 \quad (3)$$



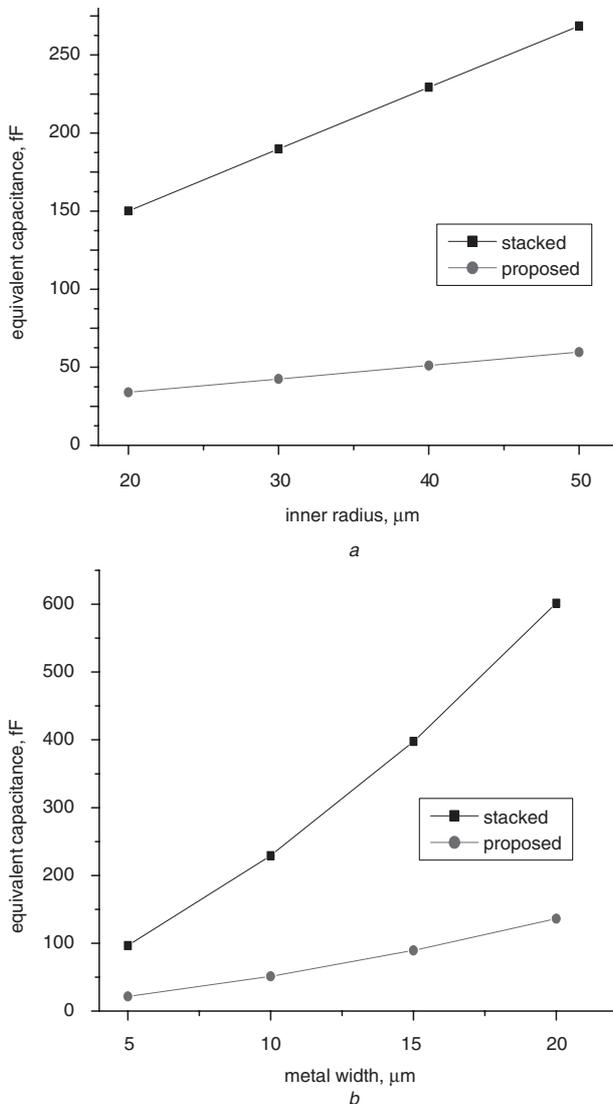
**Fig. 4** Voltage profile of  $n$ -turn  $m$ -layer proposed area-efficient inductor

After deriving the equivalent capacitance, the series resistance is also studied. Unlike the equivalent capacitance, the series resistance is a complex combination of many effects, such as the skin effect, eddy current effect, and the magnetic coupling effect. Hence, it is difficult to obtain the general analytical form. In our work, an empirical equation, given as (4), is adopted to estimate the series resistance of the area-efficient inductor

$$R_s = R_{DC}(1 + 0.17f + Bf^2) \quad (4)$$

In (4),  $R_{DC}$  is the resistance at DC,  $f$  is the operating frequency in GHz, and the coefficient  $B$  is very small and can be ignored in this case. It should be noted that (3) is process- and geometry-dependent.

Using an inductance simulator, such as ASITIC [10] or SONNET, the  $Q$  and  $f_{SR}$  can easily be predicted. Based on (2)–(4) and TSMC 0.35  $\mu\text{m}$  CMOS single-poly-four-metal (1P4M) CMOS process parameters, the equivalent capacitance of the 4-turn 2-layer conventional stacked inductor and proposed area-efficient inductor with different inner radius ( $r$ ) and metal width ( $w$ ) are shown in Figs. 5a and Fig. 5b respectively. The analytic simulation reveals that the equivalent capacitance of the area-efficient inductor is much lower than that of conventional stacked inductor for all geometrical parameters.



**Fig. 5** Equivalent capacitance

a Different inner radii with  $w = 10 \mu\text{m}$ ,  $m = 2$

b Different metal widths with  $r = 40 \mu\text{m}$ ,  $m = 2$

To verify the predicted performances, which are calculated from (2)–(4), Table 1 shows the predicted and measured  $C_{eq}$ ,  $Q$  and  $f_{SR}$  of the area-efficient and conventional stacked inductors in a 0.35  $\mu\text{m}$  1P4M CMOS process. It can be observed that predicted performances quite coincide with the measurement results irrespective of the area-efficiency or the stacked inductors.

### 3.2 Low-noise amplifier and down-conversion mixer

The two-stage common source low-noise amplifier (LNA), as shown in Fig. 6, with the fully on-chip LC-matching is employed in this receiver. A stand-alone LNA test-key was fabricated in a 0.35  $\mu\text{m}$  1P4M CMOS technology and its active area is  $280 \times 640 \mu\text{m}^2$ . By virtue of the area-efficient inductors, the die size of this LNA is very small compared with the other LNAs [11, 12]. Experimental results show that S11, S22 and S21 at 2.4 GHz are  $-14 \text{ dB}$ ,  $-13 \text{ dB}$  and  $10 \text{ dB}$ , respectively. The measured  $\text{NF}_{50}$  is 4.8 dB.

Two identical Gilbert-cell double-balance mixers [13] are chosen to down-convert 2.4 GHz RF to 1.5 MHz IF in the quadrature phase. At the RF port, a series capacitor performs AC coupling and a shunt inductor acts as an RF choke to give the bias voltage. Quadrature LO signals are generated by passing the differential LO signals through an on-chip second-order passive polyphase filter, whose schematic is shown in Fig. 7. An off-chip  $180^\circ$  hybrid is used to generate the differential LO signals.

### 3.3 $90^\circ$ delay network and combiner

The  $90^\circ$  delay circuit consists of two cascaded delay cells. Based on the conventional delay cell circuit [14], two additional MOS capacitors are added at the output terminals symmetrically, as shown in Fig. 8, to achieve the desired phase delay at 1.5 MHz. An off-chip control circuit, which includes the 3-bit DAC, fine tunes the delay phase by adjusting the voltage of the terminal  $V_{bp}$ . Figure 9 shows the simulated transient response of the digitally calibrated  $90^\circ$  delayed network. It demonstrates that the output signal, which passes through the delay network, is  $90^\circ$  phase shifted to the input signal.

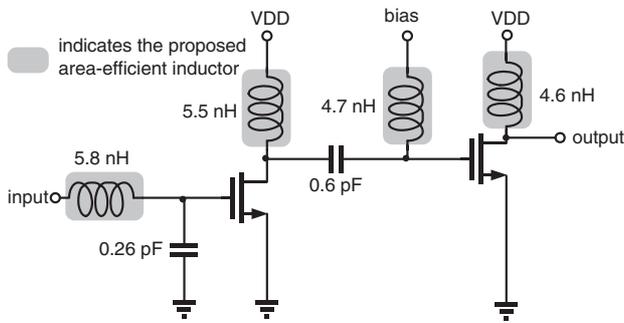
After passing through the  $90^\circ$  delay circuit, the desired signals in the I and Q channels are in phase but the image signals are out of phase. A combiner, shown in Fig. 10, adds the signals from the I and Q channels together to cancel the image signal. MC1 and MC2 are added to control the bias current to adjust the amplitude balance, and the control signal comes from the off-chip control circuit. For example, if tuning the voltage of the control terminal, say  $bbc1$ , then the amplitude of the signal at  $out+$  can be adjusted as shown in Fig. 11.

## 4 Experimental results

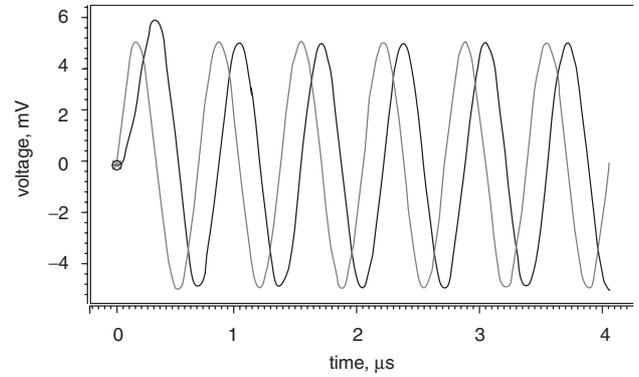
The proposed image-reject receiver was fabricated in a 0.35  $\mu\text{m}$  1P4M CMOS technology. The total active area is  $3.13 \text{ mm}^2$  without the test-keys, and the die photo is shown in Fig. 12. The circuits have been tested in a chip-on-board assembly while operating under a 3.3 V power supply. Figure 13 shows the measured transient response of the  $90^\circ$  delayed network test-key. It shows that the phase difference between the input and output signals is adjusted to  $90^\circ$  by the delayed network with conjugation of an off-chip 3-bit DAC. Applying a  $-40 \text{ dBm}$  2.4 GHz RF signal, a  $-40 \text{ dBm}$  2.397 GHz RF image signal and a  $-10 \text{ dBm}$  2.3985 GHz LO signal, the signal gain at 1.5 MHz IF is 0 dB and the image rejection ratio is 30 dB without an off-chip preselect filter. The measured gain is low because no amplifiers

**Table 1: Predicted and measured  $Q$  and  $f_{SR}$  at 2.4 GHz of 4-layer area-efficient and stacked inductors with 1  $\mu\text{m}$  spacing and 10  $\mu\text{m}$  (\* = 15  $\mu\text{m}$ ) metal width**

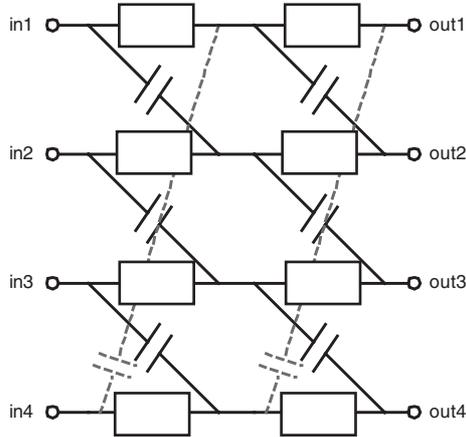
Inductors	L (nH)	Inner radius ( $\mu\text{m}$ )	Turns	Sim. $C_{eq}$ (fF)	Meas. $C_{eq}$ (fF)	Sim. $f_{SR}$ (GHz)	Meas. $f_{SR}$ (GHz)	Sim. $Q$	Meas. $Q$
Stacked 1	7.3	30	2	52.4	54.2	8.2	7.8	5.24	5.23
Area-efficient 1	9.7	40	2	37.8	35.3	8	8.6	1.85	2.03
Area-efficient 2*	7.5	30	2	32.5	31.2	10	10.4	3.58	3.5



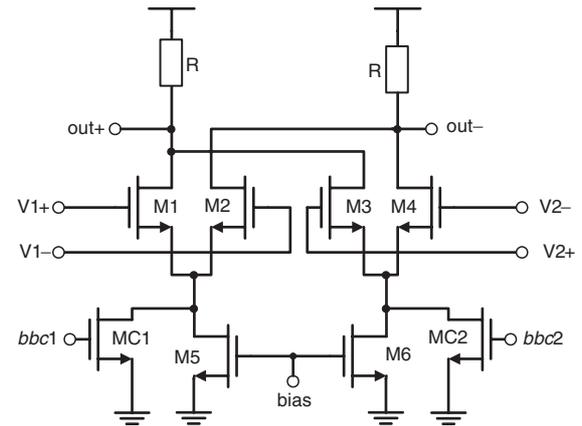
**Fig. 6** Schematic of the single-ended double-stage LNA



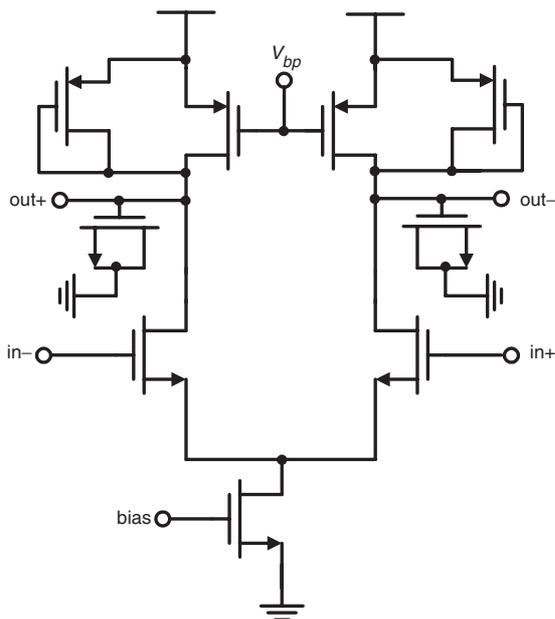
**Fig. 9** Simulated transient response of the 90° delayed network  
— input signal  
- - - output signal



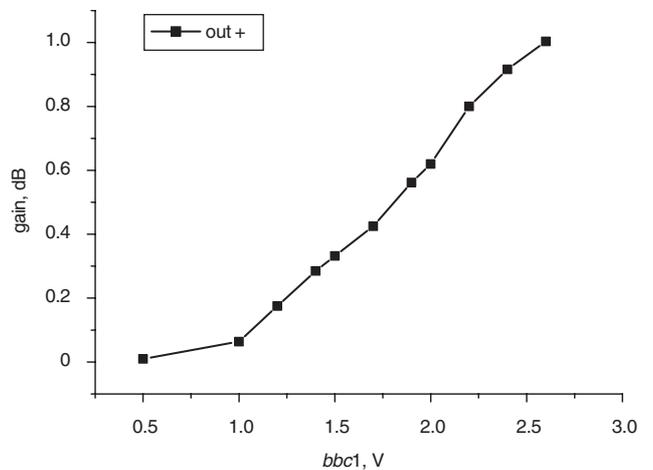
**Fig. 7** Two-stage passive poly-phase filter



**Fig. 10** Schematic of the combiner



**Fig. 8** Schematic of the delay cell



**Fig. 11** Relationship between the control voltage and output voltage in the combiner

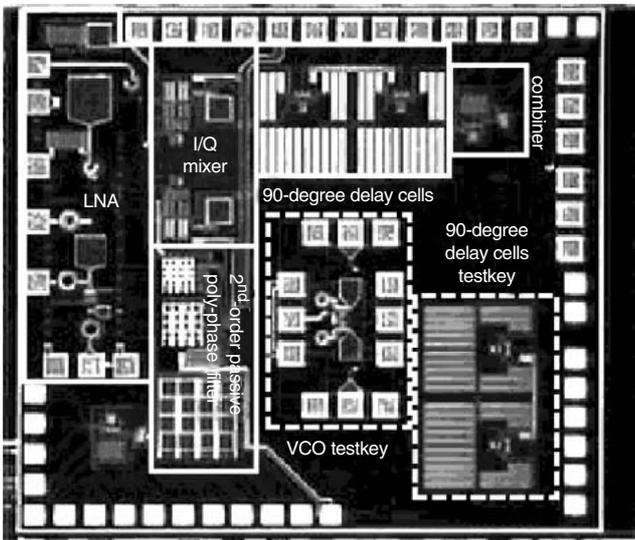


Fig. 12 Die photo of the test chip

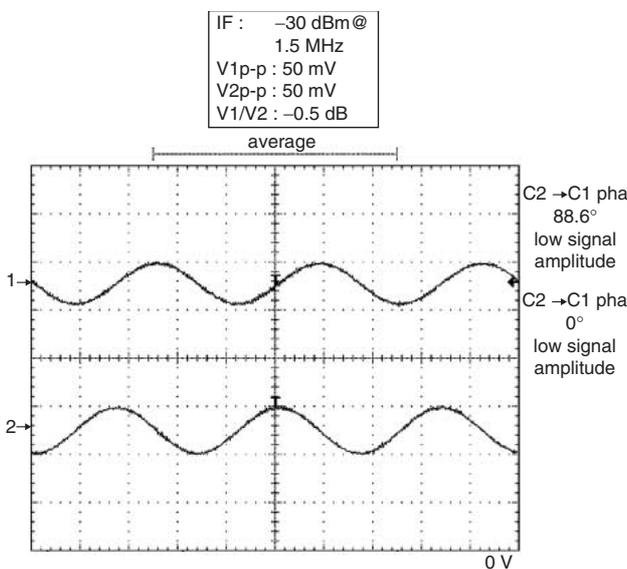


Fig. 13 Measured transient waveform of the 90° delayed network test-key

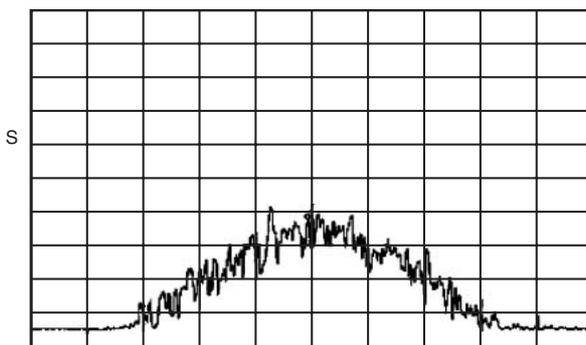


Fig. 14 GFSK output spectrum at IF  
Centre frequency: 1.5 MHz  
Span: 2 MHz  
Marker: -1.483 MHz, -62.50 dBm

compensate for the loss of the delay cells and the combiner. In spite of the gain, this circuit indeed performs the image-rejection function. The measured intermodulation intercept

Table 2: Performances summary of the test chip

	Value
RF	2.4 GHz
LO	-10 dBm at 2.3985 GHz
IF	1.5 MHz
IF gain	0 dB
IIP3	-3 dBm
IRR	30 dB
NF	11 dB
Sensitivity	-80 dBm
Power consumption	54 mW @ 3.3 V
Process	TSMC 0.35 μm 1P4M CMOS
Area	3.13 mm <sup>2</sup>

point is -3 dBm and the total noise figure (NF) is 11 dB with 54 mW power consumption. This receiver can correctly down-convert a 2.4 GHz GFSK signal to 1.5 MHz IF band. The GFSK signal emulates a Bluetooth RF signal with a modulation index of 0.35, 200 kHz frequency deviation, and 1 MHz symbol rate. Figure 14 shows the GFSK spectrum at intermediate frequency. Table 2 summarises the characteristics of this 2.4 GHz receiver.

## 5 Conclusions

An image-reject receiver has been proposed. Inaccurate delay resulting from the temperature and process variations can be mitigated by the digitally calibrated 90° delay network. In addition, the chip also adopts the proposed area-efficient inductor to significantly save the silicon area. Furthermore, the proposed method can predict the  $Q$  and  $f_{SR}$  of various inductors, such as the stacked and the area-efficient inductors. According to the experimental results, this receiver can meet the Bluetooth in-band image rejection specification.

## 6 Acknowledgment

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## 7 References

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