A Low-Cost Jitter Measurement Technique for BIST Applications *

Jui-Jer Huang, and Jiun-Lang Huang
Graduate Institute of Electronics Engineering / Department of Electrical Engineering
National Taiwan University
Taipei 106, Taiwan

Abstract

In this paper, we present a technique to measure the RMS period jitter of the signal under test. In the proposed approach, the lead/lag relationships between the signal under test and two delayed versions of itself are compared. The collected information corresponds to two points along the jitter's cumulative distribution function (CDF) curve from which the RMS period jitter value can be derived. Currently, SPICE simulation results show less than 5% error for RMS jitter values ranging from 40 to 60 ps.

1. Introduction

Measuring high-speed clock jitters is a difficult task. It usually relies on expensive ATE (automatic test equipment) and can easily consume long test time. Furthermore, the situation is getting worse as the trend of system integration onto a single chip continues. One promising solution to alleviate these problems is built-in self-test (BIST). Since on-chip BIST circuitry can be made close to the signal sources under test, accessing embedded signals becomes much easier and not limited by the bandwidth of the I/O pins. The main concern of BIST is the incurred area/performance overhead and the achievable test accuracy.

Many research efforts have been devoted to jitter testing. In [5], the authors employ a variable delay line to record the 15.9% and 84.1% points of the jitter's cumulative distribution function (CDF) curve from which the RMS jitter value can be derived. (The jitter is assumed to be a gaussian random variable.) The main advantage is that the BIST circuit is fully digital. The main limitation, on the other hand, is that the measurable jitter is limited by the gate delay available in the IC technology. High-resolution time-to-digital techniques can also be used for jitter measurement. For example, the work in [3] achieves high-resolution jitter measurement with a vernier delay line. The drawback is the large hardware overhead and the stringent delay line linearity requirement. In [8] and [7], an analytic signal method to extract peak-to-peak and RMS jitter is proposed and validated with commercial processors. The technique can reduce the test time significantly, but is not suitable for BIST applications. The method is further extended in [9]. In [2], the authors propose to use the jittery signal as the clock signal to an ADC which samples a sinusoidal signal. This way, the jitter information can be extracted from the ADC outputs. The technique reported in [1] intends to solve the linearity problem in [3] by using a component-invariant vernier delay line. The main limitation is the associated long test time. To resolve this problem, the authors also propose a test time reduction method at the expense of more hardware. In [6], the authors solve the delay line linearity problem by characterizing the non-linearity and incorporating this information during the analysis phase, which may lead to long test time.

In this paper, we propose an RMS period jitter measurement technique for BIST applications. Assuming that the jitter is a gaussian random variable, RMS jitter is characterized by comparing the phase relationships (lead or lag) between the signal under test and two delay versions of itself. This way, two points on the jitter's CDF curve are obtained from which the RMS jitter value is derived. The proposed jitter measurement circuitry is quite simple. It consists mainly of a variable delay with two delay values, a sense-amplifier based phase comparator, and an inverter for delay measurement. Currently, SPICE simulation shows promising results: an average error of less than 5% for 40-50 ps RMS jitter. We will implement a prototype chip to further validate the proposed technique.

This paper is organized as follows. In Section 2, we introduce the proposed technique, including the basic idea and the corresponding circuit implementation. In Section 3 we will present the simulation results. Implementation issues are discussed in Section 4, and we conclude this paper in Section 5.

*This work was partially supported by the National Science Council of Taiwan, R.O.C., under Grant No. NSC91-2215-E-002-040.

Proceedings of the 12th Asian Test Symposium (ATS'03)
1081-7735/03 $17.00 © 2003 **IEEE**

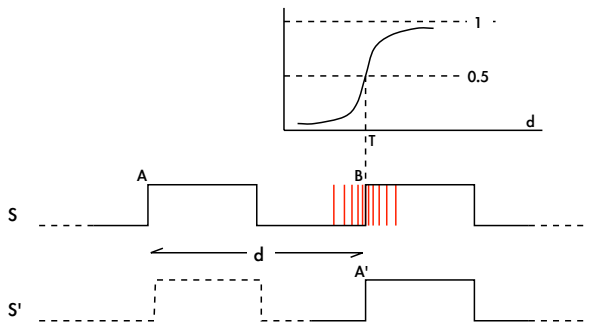

Figure 1. The basic idea.

2. The proposed technique

Assuming that the period jitter associated with the signal under test is a gaussian random variable, the objective of the proposed technique is to derive the period jitter's RMS value. (The gaussian distribution assumption is in general true for a mature design.) In the following discussion, for convenience, the term "jitter" will correspond to "period jitter."

2.1. The basic idea

Denote by S the signal under test, and J the associated jitter. To obtain the statistical information of J, our idea is to compare the phase relationships (lead or lag) between S and two delayed versions of itself. For each delay amount, the probability that S leads depends on two factors: the amount of delay and J. In fact, as will be seen later, the two probabilities correspond to two points on J's CDF curve, from which RMS_J, the RMS value of J, can be derived.

In Fig. 1, S is the signal under test, S' is a delayed version of S by d, and A, B, A' are all rising edges. (A' corresponds to A delayed by d.) Clearly, if S is jitter free, then the phase relationship between A' and B depends sorely on the value of d, i.e., A' will always lead/lag B if d is chosen to be less/greater than T, the ideal period of S.

However, in the existence of J, B will deviate from its ideal position (relative to A). As a result, the relationship between A' and B is no longer invariant—B may lead or lag A' depending on the jitter value associated with the period $[A, B]$. The probability p that B leads A' is a function of d and RMS_J (J is assumed to be gaussian). This can be seen from the CDF curve (top of Fig. 1). For example,if d equals T, p will be 0.5, and as d increases/decreases, p approaches one/zero. Also, when RMS_J increases, the CDF curve becomes flatter and p increases for $d < T$ and decreases for $d > T$.

In the proposed technique, this probability is measured twice for two different values of d. From the two probabilities and the difference of the two d's, RMS_J can be derived.

2.2. Deriving the RMS jitter value

Let d_1 and d_2 be the two delays we use, and p_1 and p_2 the measured probabilities. d_1, d_2 and the jitter values, j_1 and j_2, they map to on the jitter's CDF curve satisfy the following relationship:

$$j_i = d_i - T$$

Knowing $\Delta d = d_1 - d_2$, p_1, and p_2, RMS_J can be derived in the following way. (Note that actual values of d_1 and d_2 need not be known.)

1. Solve for x_1 and x_2 that satisfy $F_X(x_1) = p_1$ and $F_X(x_2) = p_2$ where $F_X(x)$ is the normalized gaussian CDF.
2. Since $\Delta j = \Delta d$, $RMS_J = \frac{\Delta d}{x_1 - x_2}$.

Because $F_X(x)$ has no known closed-form solution, x_1 and x_2 may be obtained by using a lookup table or the approximation function which is due to Brjesson and Sundberg, 1979 [4]. The maximum absolute error in the approximation is given as 0.27% for any $x \geq 0$. In BIST applications, if on-chip resources are insufficient for such complicated computation, one may rely on external ATE to solve for x_1 and x_2. It should be noted that the choices of j_1 and j_2 values affect the achievable measurement accuracy.

To determine the proper j_1 and j_2 values, Matlab simulations are performed for different combinations of j_1 and j_2. Based on the results, we choose $j_1 = -RMS_J$ and $j_2 = RMS_J$ which correspond to $d_1 = T - RMS_J$, and $d_2 = T + RMS_J$. The Matlab simulation results also show that, for 1 GHz signal, the allowable deviations of d_1 and d_2 are about 100 ps for 5% measurement error. The allowable deviations increase if one increases the numbers of phase comparisons.

In [5], the authors also derive the RMS jitter value from the CDF curve. Compared to their method, ours only need to sample two points along the distribution function curve. This way, the jitter measurement circuit can be made simpler; however, it also incurs higher post-processing efforts, i.e., solving the inverse of the normalized CDF.

2.3. The BIST circuitry implementation

The proposed jitter measurement circuitry is shown in Fig. 2. The main components are:

Variable delay d. The variable delay d has two different delay values, d_1 and d_2, controlled by the signal "delay_ctrl."

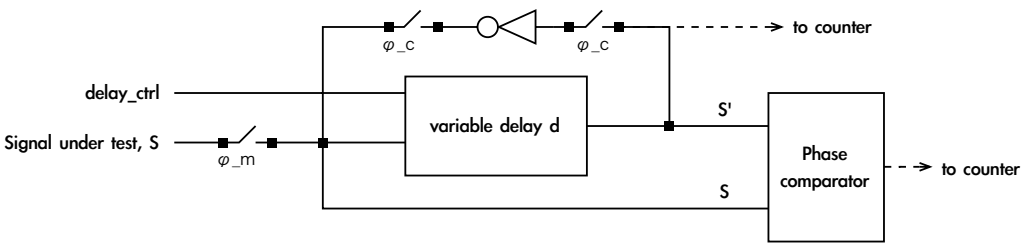

Figure 2. The proposed BIST circuitry.

Inverter. In the calibration mode, the inverter together with the variable delay forms a ring oscillator whose oscillation period can be measured using a counter.

Phase comparator. The phase comparator determines whether the rising edge of S leads or lags that of S'. Its output is high if S leads S', and low otherwise.

Counter. The counter serves two purposes. During the calibration mode, it facilitates the measurement of Δd. During the measurement mode, it keeps track of the number of times S leads S' after a number of comparisons.

Control switches. The control switches are properly opened or closed to set the BIST circuitry into different operation modes.

2.4. The BIST circuitry operation modes

The BIST circuitry has two operation modes: the calibration mode and the measurement mode.

Calibration mode. In the calibration mode, ϕ_m is low and ϕ_c is high. This way, the inverter together with the variable delay forms a ring oscillator. Let the inverter delay be d_{inv}. The "delay_ctrl" signal is set to low and high to measure the corresponding oscillation periods $(d_1 + d_{inv})$ and $(d_2 + d_{inv})$, respectively. Thus, Δd is simply the difference of the two measurements.

Measurement mode. In the measurement mode, ϕ_m is high and ϕ_c is low. The phases of S and S' are compared N times for low and high "delay_ctrl" values, and the number of times S leads S', denoted by n_1 and n_2 respectively, are counted and stored for later analysis.

2.5. The measurement flow

The jitter measurement flow consists of the two BIST circuitry modes and a following analysis phase. In the analysis phase, Δd, p_1, and p_2 are first derived:

$$\Delta d = (d_1 + d_{inv}) - (d_2 + d_{inv}), \text{ and}$$

$$p_1 = \frac{n_1}{N}, p_2 = \frac{n_2}{N}$$

x_1 and x_2 are then derived using the approximation function. Finally, RMS_J is computed:

$$RMS_J = \frac{\Delta d}{x_1 - x_2}$$

3. Experimental results

3.1. Simulation setup

Currently, we have validated the method using SPICE simulation. (We are working on the hardware validation part.) As we have mentioned in Sec. 2.2, the value of Δd and positions of j_i's must be carefully selected to ensure high accuracy. In this experiment, the signal under test is a 1 GHz clock signal (whose rise and fall times are both 150 ps), and we choose 40 ps as the target RMS jitter value. Thus, the design goals of the variable delay are:

$$d_1 = T - RMS_J = 960 \text{ ps}$$

$$d_2 = T + RMS_J = 1,040 \text{ ps}$$

N is set to 1000. Thus, a total of 2,000 phase comparisons are made.

3.2. Simulation results

In the calibration mode, the measured $(d_1 + d_{inv})$ and $(d_2 + d_{inv})$ values are 1,152 ps and 1,230 ps, respectively. Thus, we have Δd = 78.7 ps which is quite close to desired value of 80 ps and the SPICE measurement result 76.74 ps.

The simulation results for different RMS jitter values are shown in Table 1. In Table 1, the first column lists the injected RMS jitter values, the second and third columns are n_1 and n_2 respectively, the fourth column is $\Delta x =$

Table 1. Simulation Results

RMS jjitter (ps)	n_1	n_2	Δx	Result (ps)	Error ps	Error %
30	99	866	2.395	32.8601	2.8601	9.53
40	154	813	1.9084	41.2387	1.2387	3.10
50	204	775	1.5828	49.7220	0.2780	0.56
60	239	712	1.2688	62.0271	2.027	3.38
70	293	684	1.0237	76.8780	6.878	9.82

$(x_1 - x_2)$, and the last two columns are the absolute and relative errors. From the n_1 and n_2 values, we can see that d_1 and d_2 are not symmetric about 1,000 ps. The RMS jitter measurement errors are within 5% for 40–60 ps RMS jitter.

4. Discussion

Both the Matlab and the spice simulation results show that the measurement errors of this technique increase if the actual RMS jitter value is far away from the target value, which seems to be a limitation. (Recall that the choices of d_1 and d_2 depend on the target RMS jitter value.) Indeed, this makes the proposed technique unsuitable for characterization testing. However, the technique can work well in pass/fail testing if one uses the jitter specification as the target RMS jitter value. This way, the accurate measurement around the test specification reduces the chance of mis-classifying devices close to the specification. On the other hand, for devices well above or below the test specification, the measurement error is small enough so that they won't be mis-classified, either.

Deviations of d_1 and d_2 from their desired values due to process and/or temperature variation can also lead to test inaccuracies. To solve this problem, we may modify the variable delay so that it has more than two different delay values. This way, if only two of the delay values are close to the desired values, the test accuracy can be ensured. (The quality of a delay value is judged by its corresponding p value which indicates its position in the CDF curve.)

Another design-related issue is the phase comparator and the counter when the signal under test is in the GHz range. To relieve the performance requirement, one can choose to make the phase comparison in every k signal periods. Notice that this is different from dividing the signal under test by k.

5. Conclusion

In this paper, we present an RMS period jitter measurement technique intended for BIST applications. By comparing the phases of the signal under test and two of its delayed versions, information about the jitter's CDF curve is extracted and RMS jitter can thus be derived. Since only two points on the CDF curve are needed, the test circuitry is quite simple. Spice simulation results show less than 5% error for RMS jitters ranging from 40 to 60 ps. We are currently designing a prototype chip to further validate the technique. In the future, we will develop a fully digital implementation of the proposed technique to further reduce the circuit complexity.

References

[1] A. H. Chan and G. W. Roberts. A synthesizable, fast and high-resolution timing measurement device using a component-invariant vernier delay line. In *International Test Conference*, pages 858–867, 2001.

[2] S. Cherubal and A. Chatterjee. A high-resolution jitter measurement technique using ADC sampling. In *International Test Conference*, pages 838–847, 2001.

[3] P. Dudek, S. Szczepanski, and J. V. Hatfield. A high-resolution CMOS time-to-digital converter utilizing a vernier delay line. *IEEE Transactions on Solid-State Circuits*, 35(2):240–247, February 2000.

[4] P. Z. Peebles. *Probability, Random Variables, and Random Signal Principles*. McGraw Hill, Inc., Hightown, New York, 2000.

[5] S. Sunter and A. Roy. BIST for phase-locked loops in digital applications. In *International Test Conference*, pages 532–540, 1999.

[6] S. Tabatabaei and A. Ivanov. Embedded timing analysis: A SoC infrastrcture. *IEEE Design & Test of Computers*, 19(3):22–34, May–June 2002.

[7] T. Yamaguchi, M. Soma, D. Halter, J. Nessen, R. Raina, M. Ishida, and T. Watanabe. Jitter measurements of a PowerPC^{TM} microprocessor using the analytic signal method. In *International Test Conference*, pages 955–964, 2000.

[8] T. Yamaguchi, M. Soma, M. Ishida, T. Watanabe, and T. Watanabe. Extraction of peak-to-peak and RMS jitter using an analytic signal method. In *VSLI Test Symposium*, pages 395–402, 2000.

[9] T. J. Yamaguchi, M. Soma, D. Halter, R. Raina, J. Nissen, and M. Ishida. A method for measuring the cycle-to-cycle period jitter of high-frequency clock signals. In *VLSI Test Symposium*, pages 102–110, 2001.