2.4 GHz offset-cancelling down-conversion mixer

Chih-Chun Tang, Kun-Hsien Li and Shen-Iuan Liu

A down-conversion mixer utilising the offset-cancelling technique to increase the carrier-to-noise ratio (CNR) is presented. The proposed offset-cancelling mixer has been fabricated in a 0.35 µm CMOS process and it can convert the 2.4 GHz RF signal to the 280 MHz IF one with 12 mW power consumption including the buffer. Compared with the non-offset-cancelling mixer, the proposed offset-cancelling mixer has the lower noise level. Experimental results show that the offset-cancelling mixer provides 45 dB CNR better than 34 dB CNR of the mixer without the offset-cancelling technique.

Introduction: Double-balanced mixers have been widely used in RF wireless transceivers. Owing to the fully differential structure, a double-balanced mixer has many advantages over a single-balanced mixer, e.g. higher port-to-port isolation, better common mode noise rejection. However, mismatches between the characteristics of the active devices in the signal paths lead to offset. Offset is troublesome in the mixer and may result in high noise level in the translation process. Unfortunately, the noise figure (NF) and the sensitivity of the receiver relate to the noise level, i.e. the higher the noise level, the higher the NF and the lower the sensitivity. Hence, it will be helpful to improve the performances of the receiver if an easy method could be utilised to reduce the noise level of the mixer.

Offset-cancelling technique: Offset can be considered as the low frequency noise source in the mixer. Conventional offset cancelling techniques can be divided into: auto-zero, correlated double sampling and chopper-stabilised techniques [1]. The correlated double sampling method and chopper-stabilised techniques require complex clocks, which may not be suitable for RF applications. One of the auto-zero techniques [2] can be modelled as shown in Fig. 1, where the G_{m1} and G_{m2} stages are the differential pairs and the R stage is the trans-impedance amplifier. V_{os1} and V_{os2} represent the offset voltages of G_{m1} and G_{m2} stages, respectively. The working principle of this technique can be divided into two phases. At phase one, switches S1–S4 are closed, and the offset voltages are stored in C_1 and C_2 capacitors. At phase two, switches S1–S4 are opened and the input switches are closed. The G_{m2} stage is responsible for adding the offset correction current at nodes X and Y. The total offset voltage, V_{os}, referred to the input is

$$V_{os} \simeq \frac{V_{os1}}{G_{m2}R} + \frac{V_{os2}}{G_{m1}R} \qquad (1)$$

where $G_{m2}R \gg 1$. If $G_{m1}R$ and $G_{m2}R$ are large, the resulting offset voltage V_{os} will be small.

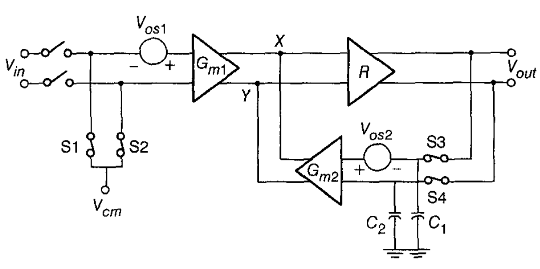

Fig. 1 *Concept of offset-cancelling technique*

Proposed offset-cancelling down-conversion mixer: Based on the double-balanced Gilbert cell [3] mixer, the simplified schematic diagram (ignoring the buffer and bias circuits) of the proposed offset-cancelling mixer is shown in Fig. 2. Note that the G_{m2} circuit consists of M_{g1} and M_{g2}, while the G_{m1} circuit consists of M_{n1} and M_{n2}. Before receiving the RF signal, switches S1–S4 are turned on, and the offset voltages caused by the differential pairs M_{n1}, M_{n2} and M_{g1}, M_{g2} are stored in capacitors, C_1 and C_2. To receive the RF signal, switches S1–S4 are turned off and the current in G_{m2} is added to correct the offset.

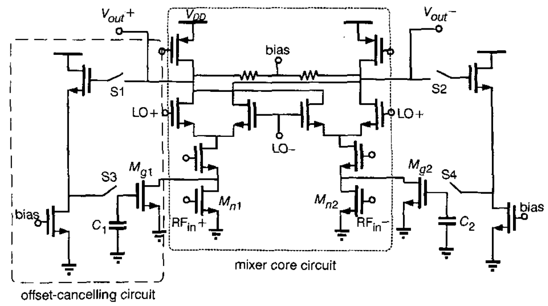

Fig. 2 *Simplified schematic diagram of proposed offset-cancelling down-conversion mixer*

Measurement results: The proposed offset-cancelling down-conversion mixer has been fabricated in a 0.35 µm 1P4M standard CMOS process. For comparisons, the conventional Gilbert cell down-conversion mixer without the offset cancelling also has been realised on the same die. Applying the −40 dBm 2.4 GHz RF signal and the 4 dBm 2.12 GHz LO signal, the measurement results show that the proposed offset-cancelling mixer improves 11 dB CNR, as shown in Fig. 3. However, the linearity of the proposed offset-cancelling mixer is slightly degraded because the excess nonlinearity is caused by the additional MOSFETs, which are employed by the offset-cancelling technique. The measured IIP3 of the proposed mixer is 11 dBm and the conventional mixer is 12 dBm. Table 1 summarises the comparisons between the proposed and the conventional mixers.

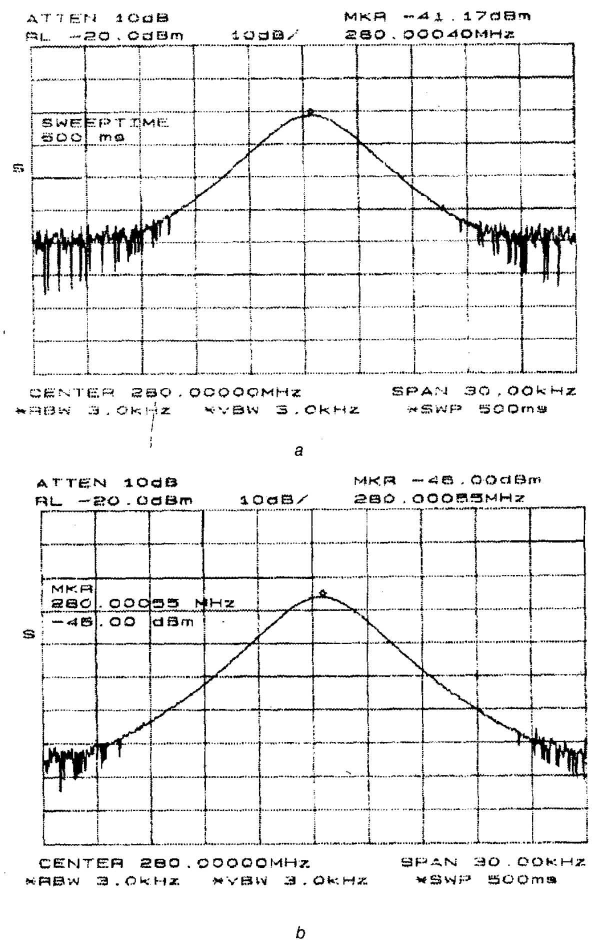

Fig. 3 *Output spectra*

a Conventional mixer without offset-cancelling technique
b Proposed mixer with offset-cancelling technique

Table 1: Comparisons between proposed offset cancelling and conventional down-conversion mixers

	Mixer without offset-cancelling	Mixer with offset-cancelling
RF frequency	2.4 GHz	
LO frequency	2.12 GHz	
LO power	4 dBm	
Conversion gain	−1 dB	−5 dB
IIP3	12 dBm	11 dBm
CNR	34 dB	45 dB
Power consumption	11 mW	12 mW
Process	TSMC 0.35 μm 1P4M CMOS	

Conclusion: An offset-cancelling down-conversion mixer has been realised and measured in a 0.35 μm 1P4M standard CMOS process. According to the measurement results, the proposed mixer could improve 11 dB CNR at the cost of slight linearity degradation.

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Robust and universal constant-g_m circuit technique

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A robust and universal circuit technique to maintain a constant transconductance, g_m, in rail-to-rail amplifiers based on input stages made up of parallel-connected complementary differential pairs, is presented. The technique is universal, since it is valid regardless of the g_m/I_D characteristic of input devices. Also, the accuracy does not depend on any condition for matching n- to p-channel input transistors, which makes the technique robust. Experimental results obtained from a 0.8 μm CMOS test-chip prototype, are given.

Introduction: Many circuit techniques, usually known as constant-g_m techniques, to maintain a constant transconductance (g_m) value over the entire common-mode (CM) voltage range in rail-to-rail operational amplifiers based on input stages made up of two parallel-connected complementary differential pairs (Fig. 1), have been proposed [1–3]. However, none of the previously reported techniques is simultaneously robust and universal. By the term robust, we mean that the accuracy of the circuit for maintaining the total amplifier transconductance constant does not rely on any condition for matching n- to p-channel input transistors (i.e. on scaling the geometries to compensate for the difference in mobility between electrons and holes). By the term universal, we mean that the accuracy is independent of the input transistor types and their operation regions. Thus, in this context, universal means that the technique is valid for any g_m/I_D characteristic of the amplifier input devices, and, hence, it also is compatible with modern submicron CMOS devices, in which the familiar square law is not completely satisfied. Therefore, the accuracy in the previously reported constant-g_m circuits is limited by the principle of operation itself.

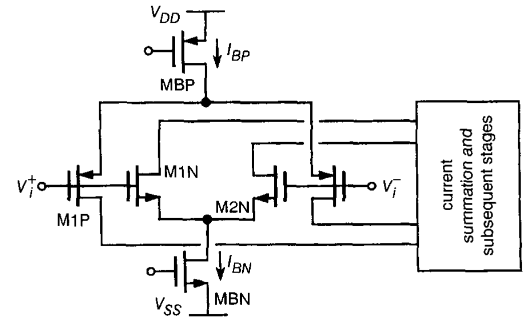

Fig. 1 *Typical rail-to-rail CMOS amplifier input stage*

In this Letter we introduce a robust and universal constant-g_m circuit technique for rail-to-rail input stages. The principle of operation is based on a direct sensing of the amplifier g_m and a comparison with a reference transconductance value. Experimental results demonstrate a better accuracy than in any other proposed technique.

Principle of operation: Fig. 2 shows a conceptual circuit schematic diagram to illustrate the principle of operation of the proposed constant-g_m technique. In this circuit, $T_{P,REF}$ and T_P represent simple p-channel differential pairs identical to the corresponding PMOS pair of the rail-to-rail amplifier input stage (M1P-M2P in Fig. 1). However, although $T_{P,REF}$ and T_P are nominally biased with the same current level (i.e. $I_B = I_{BP}$), I_{BP} is a replica of the tail current of the p-channel pair of the rail-to-rail input stage, and, therefore, it depends on the CM voltage ($V_{i,cm}$) of the amplifier input voltage signals (i.e. V_i^+ and V_i^-). Similarly, T_N is a replica of the NMOS amplifier input pair M1N-M2N. All the differential pairs in Fig. 2 are unbalanced by a DC input voltage V with the polarities shown, the value of which is assumed small enough so that they operate in the linear region. The differential output currents i_{REF}, i_P, and i_N are summed and the output voltage of this summing current section controls the biasing current I_{BN} of T_N, as indicated by the dashed line in Fig. 2. A replica of I_{BN} is used for biasing the n-channel pair of the rail-to-rail amplifier input stage. The negative feedback loop guarantees that the following equation is satisfied:

$$g_{m,p,ref} = g_{m,p} + g_{m,n} \qquad (1)$$

where $g_{m,p,ref}$, $g_{m,p}$, and $g_{m,n}$ account for the small-signal transconductances of $T_{P,REF}$, T_P, and T_N, respectively. Thus, when $V_{i,cm}$ is close to the negative supply voltage, the current source of the p-channel amplifier differential pair operates in saturation and I_{BP} is equal to I_B. Then, $g_{m,p,ref}$ and $g_{m,p}$ have the same value and the loop ideally generates a current I_{BN} equal to zero. Notice that if any mismatch between $T_{P,REF}$ and T_P exists, such as $g_{m,p,ref} > g_{m,p}$, I_{BN} is not equal to zero, however, it does not have any influence in the rail-to-rail amplifier, since its NMOS pair is cut off in this $V_{i,cm}$ range. For $V_{i,cm}$ values close to the positive supply voltage, the current I_{BP} is equal to zero, and the feedback loop adjusts the current I_{BN} so that $g_{m,p,ref}$ and $g_{m,n}$ coincide. When $V_{i,cm}$ takes the bias current source of the amplifier PMOS input pair out from saturation, I_{BP} decreases with respect to its nominal value I_B. Now, the current I_{BN} is increased by the negative feedback action so that $g_{m,p} + g_{m,n}$ is kept constant and equal to $g_{m,p,ref}$; i.e. the circuit in Fig. 2 not only ensures that $g_{m,p} + g_{m,n}$ is equal to $g_{m,p,ref}$ for $V_{i,cm}$ voltages close to the rails (i.e. when one of the amplifier input pairs is cut off), but also that the transition regions of the two amplifier differential pairs are perfectly overlapped so that (1) is satisfied even in such region. In the context of this work, the transition or takeover region of a differential pair means the input CM voltage range where the corresponding tail current source operates is in the triode region. Notice that $g_{m,n}$ and $g_{m,p}$ coincide at any moment with the transconductances of the n- and p-channel pairs of the rail-to-rail amplifier, respectively, since they arise from differential pairs with the same aspect ratios biased with the same current, also respectively. Therefore, (1) indicates that the transconductance ($g_{m,p} + g_{m,n}$) of the rail-to-rail