A Novel SiGe BiCMOS Variable-Gain Active Predistorter Using Current Steering Topologies

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Abstract **— This paper presents a novel design of 2.4-GHz variable-gain active predistorter (PD) using a 0.35-μm SiGe BiCMOS technology. The current steering topologies are selected for this design to provide dual functions of (1) an active predistorter for power amplifier linearization, and (2) a variable gain amplifier (VGA) for transmitter power control. Unlike other traditional "passive" predistorters, this active predistorter does not need an additional buffer amplifier to compensate the loss. Furthermore, through the bias voltage control at low current region, the amount of gain expansion from this predistorter becomes programmable to compensate the PA non-linearity. Finally, this variable-gain predistorter could be used as a VGA in a multi-stage power amplifier design and it is well suitable for the RF-SOC applications. The PA experimental results of 16-QAM modulated signals show that the compressed constellation can be uniformly spread out into a "square", the spectral re-growth is suppressed by 7-9 dB, and the EVM can be reduced from 9.9 % to 5.7 %.**

Index Terms **— Linearization, predistorter, nonlinear, power amplifier (PA), radio frequency integrated circuit (RFIC).**

I. Introduction

To enhance the spectral efficiency, modern digital communication systems tend to use complex digital modulation schemes, such as 16-QAM or 64-QAM, which requires a high-linearity power amplifier to reduce the spectral re-growth and EVM. To satisfy the stringent linearity requirements, there are many linearization techniques proposed in recent years, such as feedback, feed-forward, and predistortion.

Predistortion linearization has the advantages of smaller sizes, less complexity, lower costs than other techniques, which means more suitable for handset applications. However, the traditional "passive" predistorters [1]-[3], usually cause high insertion losses (IL). So we need an extra buffer amplifier to increase the predistorted signal level. To eliminate an additional buffer amplifier, an "active" predistorter using cascode FET structures in GaAs MMIC process has been proposed [4]. Instead of using GaAs process, this paper proposes a novel variable gain active predistorter in 0.35-μm SiGe BiCMOS technology at 2.4 GHz, which can be integrated with other digital circuits for RF-SOC applications.

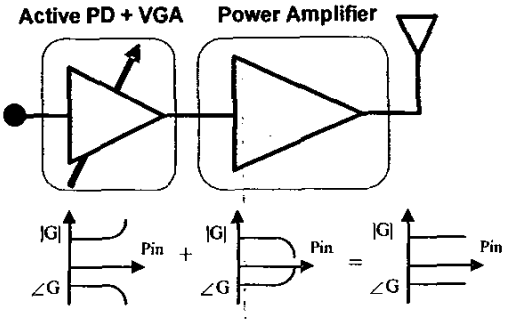

Fig. 1. Configuration of a multi-stage power amplifier block including a linearized variable-gain active predistorter.

The classical current steering topologies have been successfully implemented in the PA gain control [5]. Nevertheless, this paper utilizes similar topologies to generate not only the variable gain, but also the gain expansion for an active predistorter. When this predistorter is biased at low current region, it can provide up to 9 dB of gain expansion as the input power is increased. By adjusting the bias voltage, an appropriate gain expansion is achieved to compensate the gain compression near the PA non-linear region. When we use this variable-gain active predistorter to improve the power amplifiers linearity, we do not need any additional buffer amplifiers. Therefore, this predistorter is a dual-function driver amplifier, which provides both variable gain and predistortion functions. Consequently, this design can also reduce the complexity of the predistortion linearization techniques. Fig. 1 shows a block diagram of a multi-stage power amplifier whose driver-stage has been replaced by a variable-gain active predistorter, and it can be easily integrated with other DSP control circuits in silicon technology, which is attractive for handset applications.

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II. Technology

In the variable-gain active predistorter design, a 0.35-μm 3P3M SiGe BiCMOS process is used on 710-μm Si-substrate provided by TSMC. It provides a poly layer for the gates of the MOS, another two poly layers for the emitters and bases of the HBT, and three metal layers for inter-connection. The HBT device is selected for this design. This device exhibits Base-to-Collector breakdown voltage of 6 V, peak unit current gain frequency f_t around 27 GHz at Vce=1V. A MIM capacitor has been developed using oxide inter-metal dielectric whose unit capacitance is 1 fF/μm2. Two types of polysilicon resistors, with several Ω/□ and kΩ/□, are provided by choosing the individual dose of ion-implantation separately form the gate electrode doping process.

III. Circuit Design and Fabrication

The variable-gain active predistorter utilizes the classical current steering topologies, which is biased at low current region to produce gain expansion characteristics. The schematic shown in Fig. 2 was simulated with Agilent ADS. The common emitter (CE) connected transistor Q1 is the input transistor, and we can fix its collector current with a simple current mirror biasing by Q4 and a fixed regulated voltage Vg. The second stage transistors Q2 and Q3 act as common base (CB) which generate the gain expansion. The RF ground at Q2 and Q3 can be achieved by the on-chip capacitance. The total collector current of transistors Q2 and Q3 depend on the collector current of the input transistor Q1. The diode connected transistors Q5, Q6, Q7, and Q8 form the temperature compensation circuits. Two spiral inductors are chosen to be part of the input and output matching network. The inputs and outputs have on-chip DC-blocking capacitors that also take part in the impedance matching. This predistorter draws total 5 mA DC current from the 3 V supply voltage.

When we increase the bias control voltage Vgc, the collector current of the Q3 will raise; simultaneously, the collector current of Q2 would fall down. In this manner, we can bias Q2 near the low current region. As the input RF power is increased, there is a positive gain slope in Q2. We can use this gain expansion characteristic to compensate the gain compression of power amplifiers. Furthermore, the amount of gain and gain expansion can be adjusted by the control voltage Vgc in order to compensate the various nonlinearities of the power amplifier under different input power level.

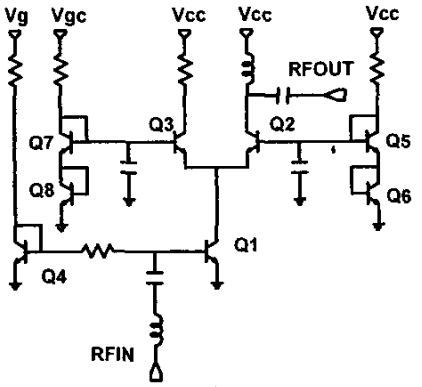


Fig. 2. Schematic of the active predistorter.

IV. Measurement Result

Fig. 3 illustrates the chip photo of the 2.4 GHz variable-gain predistorter. The physical size of this predistorter is 0.8 mm x 0.8 mm including on-wafer probing pads.

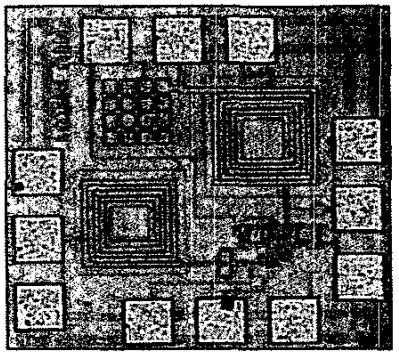


Fig. 3. Photograph of the variable-gain active predistorter.

Fig. 4 shows the simulated and measured S-parameter results. The measured results have an excellent agreement with the simulated results. It also demonstrates about 8 dB small signal gain at Vgc=2.7 V, and Vg=0.9 V. The input and output return loss has a value less than -15 dB at 2.4 GHz. It is also observed that an excellent matching condition is achieved throughout the VGA gain tuning range. Fig. 5 shows the gain expansion and variable-gain characteristics of the predistorter at 2.4 GHz for difference Vgc. At Vgc=3.35 V, it provides up to 9 dB of gain expansion as the input power is increased. Based on the simulated results, the gain control range from -20 dB to 7

dB is achieved through adjusting the bias control voltage Vgc.

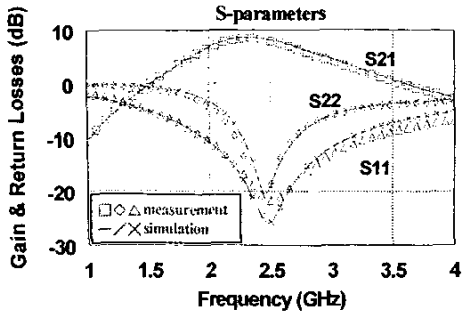


Fig. 4. S-parameter simulated and measured results at Vgc=2.7 V and Vg=0.9 V

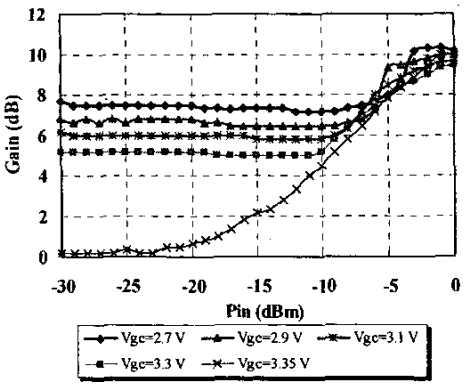


Fig. 5. Measured gain expansion and variable-gain characteristics of predistorter at 2.4 GHz for difference Vgc.

To verify the functions of the variable-gain active predistorter, we design a 2.4 GHz multi-stage hybrid power amplifier and fabricated on a FR-4 PCB, whose first stage has been substituted by the active predistorter. Then we adjust the control voltage Vgc to establish appropriate gain expansion to compensate the gain compression characteristics of power amplifier.

Fig. 6 shows the gain deviation of the hybrid power amplifier with and without predistorter, respectively, at 2.4 GHz. The power amplifier without predistorter shows gain compression as the amplifier enters the saturation region. To compensate the nonlinearities of this power amplifier, we add a variable-gain active predistorter biased at Vgc=2.9 V, which provides 7 dB power gain and 2 dB gain expansion for the output power at 15dBm. After linearization, the PA linear region is extended, but the PA linearity still needs to be measured under digital modulated signals.

To test this power amplifier under digital modulations, a 16 QAM signal at 2.4 GHz with the symbol rate of 24.3 kHz is used. Fig. 7 and Fig. 8 plot the measurement results including constellation display with symbol points only, output spectrum, and performance summary. Without predistorter, the constellation is not "square" in Fig. 7(a), which is due to the gain compression of the power amplifier. After adding the predistorter, the points in the constellation can be spread out uniformly into a "square" in Fig. 8(a), and the EVM can be reduced from 9.9 % to 5.7 %. In addition, the spectral re-growth is suppressed by 7-9 dB. The PA with predistorter in Fig. 8 has better linearity and higher linear output power, 1-dB higher, than the PA without predistorter in Fig. 7.

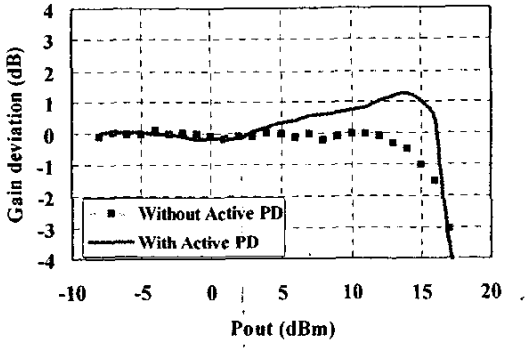
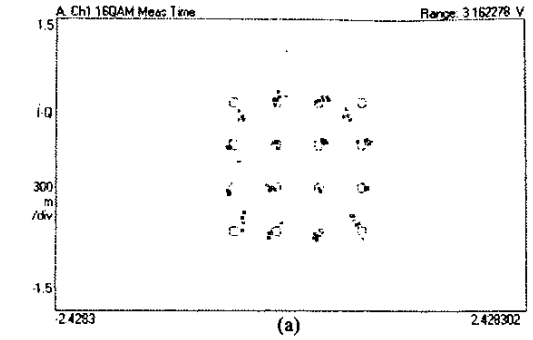


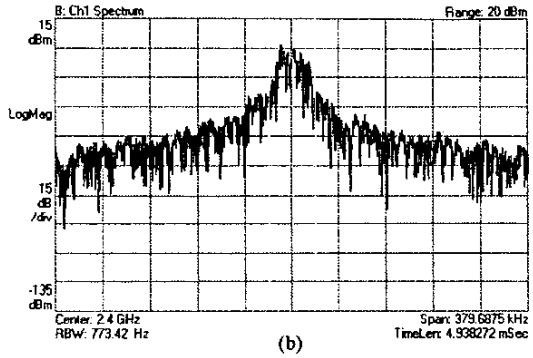
Fig. 6. Measured gain deviation of the hybrid power amplifier with and without variable-gain active predistorter at 2.4 GHz.

V. Conclusion

This paper demonstrates a 2.4GHz novel variable-gain "active" predistorter using current steering topologies in a 0.35-μm 3P3M SiGe BiCMOS technology. First of all, the proposed predistorter provides gain expansion to compensate the gain compression in PA non-linear region. Secondly, this predistorter can be used as a VGA in the multi-stage power amplifier design. This design can also reduce the complexity of the predistortion linearization techniques, which is attractive for handset applications. According to the experimental results, it is confirmed that the proposed predistorter improves the linearity through bias voltage control. The PA experimental results of 16-QAM modulated signals show that the constellation can be spread out uniformly into a "square", the spectral re-growth is suppressed by 7 – 9 dB, and the EVM can be reduced from 9.9 % to 5.7 %.



(a)

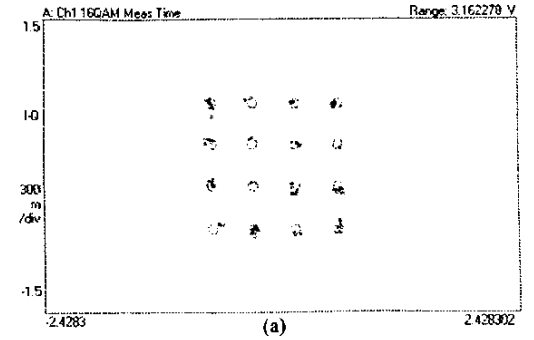


(b)

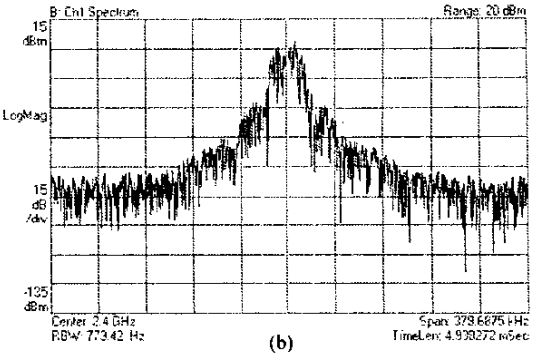
EVM	= 9.9524	%rms	24.348	% pk at sym		55
Mag Err	= 8.8691	%rms	-24.013	% pk at sym		55
Phase Err	= 3.7766	deg	-13.199	deg pk at sym		59
Freq Err	= 8.0843	Hz				
IQ Offset	= -26.833	dB	SNR(MER) = 17.202		dB	
Quad Err	= -2.8794	deg	Gain Imb = 0.09		dB	

(c)

Fig. 7. The measured 16 QAM modulation quality results at 2.4 GHz without predistorter, (a) constellation diagram, (b) output spectrum with a channel power of 14 dBm in 35 kMz channel bandwidth, (c) performance summary.



(a)



(b)

EVM	= 5.7774	%rms	15.789	% pk at sym		12
Mag Err	= 4.4644	%rms	-11.740	% pk at sym		67
Phase Err	= 3.5648	deg	-13.990	deg pk at sym		61
Freq Err	= 2.5747	Hz				
IQ Offset	= -27.152	dB	SNR(MER) = 22.674		dB	
Quad Err	= 3.3316	deg	Gain Imb = -0.01		dB	

(c)

Fig. 8. The measured 16 QAM modulation quality results at 2.4 GHz with predistorter, (a) constellation diagram, (b) output spectrum with a channel power of 15 dBm in 35 kMz channel bandwidth, (c) performance summary.

ACKNOWLEDGEMENT

This work is supported in part by National Science Council (NSC 92 - 2213 - E - 002 – 068). The RFIC chip is fabricated by TSMC through the Chip Implementation Center (CIC), Taiwan, ROC. The authors would like to thank Pei-Si Wu, Chia-Chi Chang, and Hong-Yeh Chang for their assistance on chip measurements.

REFERENCES

[1] G. Hau, T. B. Nishimura, N. Iwata, "A highly efficient linearized wide-band CDMA handset power amplifier based on predistortion under various bias conditions," *IEEE Trans. Microwave Theory & Tech*, vol. 49, no. 6, pp. 1194-1201, June 2001.

[2] H. S. Jang, Y. Kim, S. W. Kim, I. S. Chang, Y. C. Jeong, "Design of a new pre-distorter using low frequency second order inter-modulations of a harmonic generator," *Proceedings of International Conference APMC'02*, vol. 1, pp.149-152. 2002.

[3] S. W. Kim, H. T. Jeong, C. D. Kim, I. S. Chang, "A novel predistorter using a balanced type IM3 generator," *2003 IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 1, pp. 339-342, June 2003.

[4] J. Kim, M.-S. Jeon, J. Lee, Y. Kwon, "A new "active" predistorter with high gain and programmable gain and phase characteristics using cascode-FET structures," *IEEE Trans. Microwave Theory & Tech*, vol. 50, no. 11, pp. 2459-2466, November 2002.

[5] V. T. S. Vintola, M. J. Matilainen, S. J. K. Kalajo, E. A. Jarvinen, "Variable-gain power amplifier for mobile WCDMA applications," *IEEE Trans. Microwave Theory & Tech*, vol. 49, no. 12, pp. 2464-2471, December 2001.