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Architecture Design of MPEG-2 Decoder System

Yung-Pin Lee, Liang-Gee Chen, and Chung-Wei Ku

National Taiwan University, Taipei, Taiwan, R. O. C.

Abstract

An architecture for the VLSI Design of MPEG-2 video decoder is introduced to achieve the MP@ML (Main Profile, Main Level)[1]. Hardware complexity is analyzed, and decoding unit (VLD, IQ, IDCT, MC, etc.) is designed to reach the required performance.

1 Introduction

With the advance of image compression, various compression standards, such as H.261, JPEG, MPEG-1, are developed. MPEG-1[2] was optimized for a bitrate of about 1.5 Mbits/s and for a SIF (352×240×30) format. However, for the request of higher bitrate and resolution, the Moving Pictures Expert Group (MPEG) completed the committee draft of MPEG-2[1] in Nov. 1993. MPEG-2 serves a wide range of applications, bitrate, resolutions, qualities, and services. Applications cover digital storage media, television broadcasting, and communication. In order to serve various applications, a limited number of subsets of the MPEG-2 syntax are stipulated by means of "profile" and "level" (see Table 1). This paper mainly describes the MP@ML for its simplicity and completeness.

2 Architecture of MPEG-2

A MPEG-2 decoder system can be partitioned into four modules: host interface, memory interface, decoding unit, and display interface, which are all interconnected by a local bus (see Fig. 1)[3]. The maximum required memory bandwidth for local DRAM access is

$$720\times576\times30\times(\frac{81}{64}\times1.5\times2+1.5+1.5) = 84.56 \text{ Mbytes/s},$$

that is 11.8 ns. With 48-b data bus, the access time needs 71 ns which is hard to achieve by random access of DRAM. So page mode for memory access is needed. Memory size needs at least 10.2 Mbits which includes two pictures storage and output buffer. The VBV Buffer size for MP@ML is 1.8 Mbits, So 16 Mbits for total DRAM size will be enough.

3 Design of Decoder Unit

Decoding unit[4] includes VLD (variable length decoding), inverse scan, IQ (inverse quantization), IDCT, and MC (motion compensation). The area of MC and IDCT is more larger than other modules, so reduce the size of these two modules will have apparent effect on reducing the whole system size. Traditionally, Design of 2-D IDCT is splited into two 1-D IDCT's. With the consideration of hardware area and latency, we used direct 2-D IDCT method rather than row-column method. We proposed a more regular strcuture for direct 2-D IDCT. The input data reorder can be solved by arranging the output of inverse scan. Fig. 2 shows the architecture for IQ which has more regular scheme. MC is composed of motion vector decoder and predicted picture reconstructor. Motion vector decoder (Fig. 4) generates the motion vector and updates predicted motion vector. Predicted picture reconstructor (Fig. 3) reads previous reconstructed pixels to form current pixels with half-pel accuracy. The time for reading previous picture pixels from local bus and writing current constructed pixels to local bus is arranged carefully so as not to increase the latency.

4 Summary

After completing the design of MP@ML, there are two ways to continue this work:

HDTV: Speed up the architecture to achieve the HDTV level (MP@HL). Future HDTV system will be similar to our proposed architecture except it's faster. So experience of design on MP@ML can be directly applied on HDTV design.

Scalability: Scalability enable a decoder to reconstruct useful video from pieces of a total bitstream.

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Table 1: Profiles and levels for MPEG-2.

Profile / Level	Simple	Main	SNR Scalable	Spatial Scalable	High
High		MP@HL			HP@HL
High 1440		MP@H1440		SSP@H1440	HP@H1440
Main	SP@ML	MP@ML	SNP@ML		HP@ML
Low		MP@LL	SNP@LL		

So it makes MPEG-2 suitable for data transmission and multimedia applications. However, the architectures of both based layer and enhencement layer are similar to MP@ML, so it's easy to expand our architecture to scalable architecture.

References

[1] ISO/IEC 13818-2, "Information Technology - generic coding of moving pictures and associated audio," Committee Draft, Nov. 1993.

[2] MPEG, "ISO CD11172-2: Coding of moving pictures and associated audio for digital storage media at up to about 1.5Mbits/s", Nov.1991.

[3] T. Fautier, "VLSI implementation of MPEG decoders," *IEEE ISCAS'94 tutorials*, pp. 164-172, May 1994.

[4] T. Onoye, Y. Morimoto, T. Masaki, and I. Shirakawa, "Design of inverse DCT and motion compensator for MPEG-2 HDTV decoding," *APCCAS'94*, pp. 608-613, Dec. 1994.

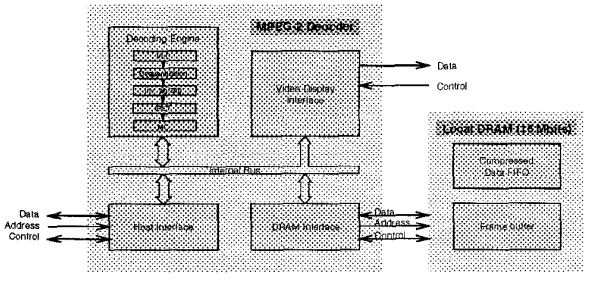
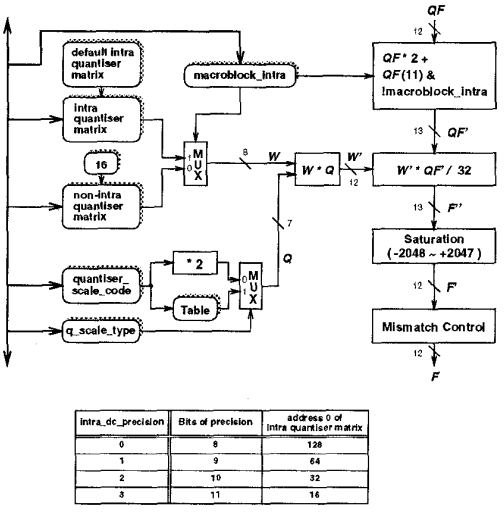


Figure 1: Architecture of MPEG-2 decoder system.



intra_dc_precision	Bits of precision	address 0 of intra quantiser matrix
0	8	128
1	9	64
2	10	32
3	11	16

Figure 2: Architecture of inverse quantization.

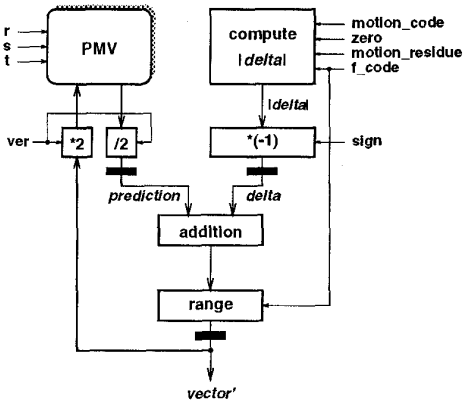


Figure 3: Architecture of motion vector decoder.

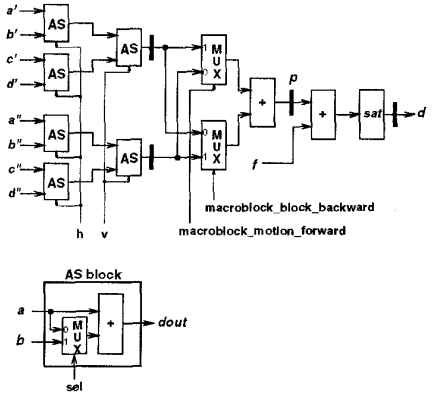


Figure 4: Architecture of Predicted picture reconstructor.