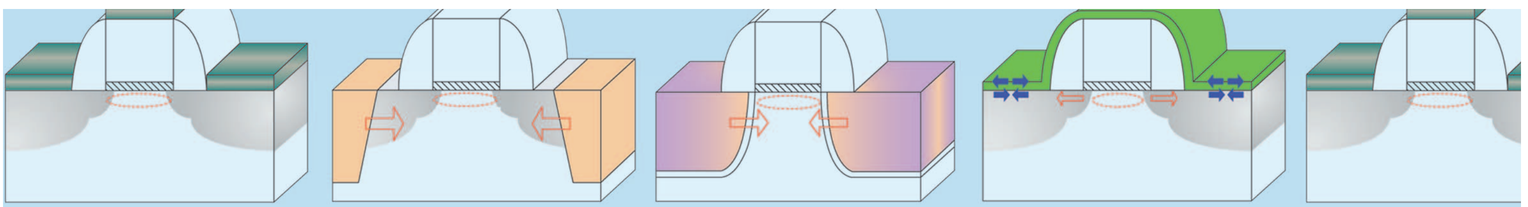


# Mobility-Enhancement Technologies

## Recent progress using new materials, process-induced strain, and package strain

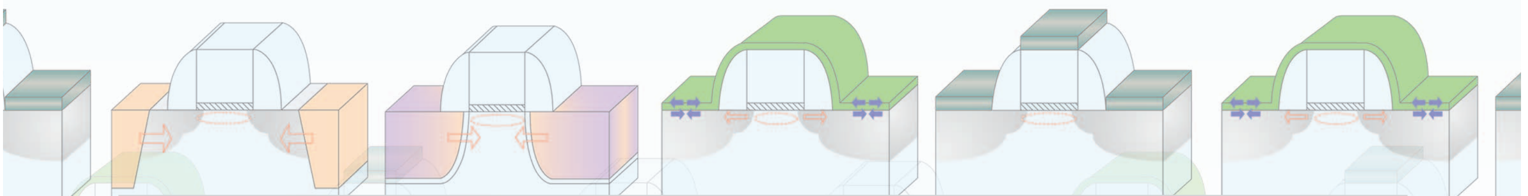
*Chee Wee Liu, S. Maikap, and C.-Y. Yu*

Aggressive scaling of complementary metal-oxide-semiconductor (CMOS) technology requires a high drive current to increase circuit speed. Both the gate capacitance $C_g$ and carrier mobility $\mu$ can improve the drive current $I_d \sim C_g \mu$. The ultrathin oxide, high-$\kappa$ dielectrics, and metal gate (to mitigate the poly-depletion effect) can increase gate capacitance. However, contamination issues, thermal budget, Fermi-level pinning, mobility degradation, and interfacial layer scalability delay the introduction of high-$\kappa$ dielectrics into industrial applications. The metal gate also suffers from work function availability, thermal budget, process compatibility, and contamination problems. The continuous scaling of the oxynitride films with increasing nitrogen content seems to be used down to the 22-nm technology node with an equivalent oxide thickness of $\sim 0.7$ nm for low operation power applications [1]. Mobility enhancement by strain, new materials such as Ge or SiGe channels, and new substrate orientation such as (110) and (111) offers alternative ways to increase drive current without suffering from gate current leakage due to gate dielectric scaling. The high mobility gives high source injection velocity into the quasi-ballistic transport channel of the advanced deca-nanometer devices [2], [3]. For large devices, the mobility itself has more impact on the drive current [4].

Applying stress to induce appropriate strain in the channel region of metal-oxide-semiconductor field effect transistors (MOSFETs) increases both electron and hole mobilities in the strained channel [5]–[8]. Furthermore, interest is driven by the possibility of creating novel electronic devices as well as integrating existing devices in different materials systems, leading to the production of integrated circuits with increased functionality and lower cost. In this article, we review various mobility enhancement techniques, such as substrate-enhancement, including stain, Ge/SiGe channels, orientations, process-induced strain, and package-strain (external mechanical strain).

## SUBSTRATE STRAIN

Si and Ge are completely miscible for a full range of composition with the lattice mismatch of $\sim$4.2%, which can be helpful for generating strain. A comprehensive review of SiGe can be found in [9]. When a thin film with a larger lattice constant, e.g., $Si_{1-x}Ge_x$ is grown on a substrate with smaller lattice constant, e.g., silicon, the film retains the in-plane lattice constant of the substrate and is under a biaxially compressive strain [Figure 1(a)] [8] if its thickness is under critical thickness. The strain condition depends on the Ge fraction and the process condition. Figure 1(b) shows the band offset of $\sim$7 meV/Ge% between the strained-$Si_{1-x}Ge_x$ epilayer and the relaxed Si substrate, and the offset is mainly on valence bands (conduction band offset is negligible) [10]. Due to the valence band modification in strained-$Si_{1-x}Ge_x$ layers, hole mobility can be improved in this structure as compared to the Si [11], [12]. Recently, the hole mobility of strained-$Si_{0.72}Ge_{0.28}$ pMOSFETs ($L_g = 55$ nm) with the TiN/$HfO_2$ gate stack is enhanced to be 58% as compared to the universal mobility at the effective field of 1 MV/cm [13]. Note that the 5–20% carrier mobility degradation for the high-$\kappa$/bulk Si channel is commonly reported,



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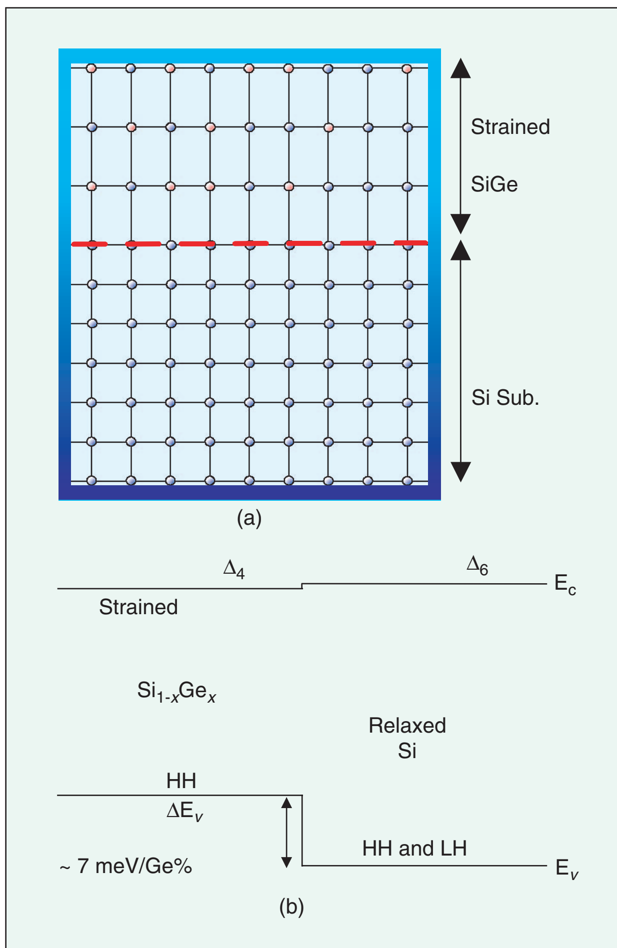
and the mobility degradation can be recovered using the strain technology.

The $Si_{1-x}Ge_x$ grown on Si can be relaxed if it is much thicker than critical thickness, and/or is annealed at high temperature to reach thermal equilibrium. However, the $Si_{1-x}Ge_x$ under stress may generate dislocations if relaxation occurs. Each misfit dislocation segment can possess two threading dislocation segments that extend to the wafer surface to satisfy the continuity of a Burgers circuit in a crystal [14]. The high threading dislocation densities in relaxed layers may be reduced by the virtual $Si_{1-x}Ge_x$ substrate structures by increasing the Ge concentration in steps (step grading) or linearly [Figure 2(a)] in buffer layers [5], [15], or the insertion of an Si layer in the relaxed $Si_{1-x}Ge_x$ [16]. The grading layers can force the misfit dislocation network to distribute along the graded layers, instead of all confined at the $Si_{1-x}Ge_x$/Si interface, as in the case of uniform buffers. This reduces the interaction between the misfit segments, where the interaction can produce threads toward the surface, and a typical threading density of $1 \times 10^5$ cm$^{-2}$ is commonly reported. When a thin film with a smaller lattice constant, e.g. silicon, is grown on a larger lattice constant substrate (e.g. relaxed $Si_{1-x}Ge_x$), the film retains the in-plane lattice constant of the




*1. A schematic diagram of lattice arrangement of (a) the pseudomorphic strained-$Si_{1-x}Ge_x$ grown on Si [8] and (b) the corresponding band alignment [10].*

substrate and is under a biaxially tensile strain if it is thinner than critical thickness. Figure 2(b) shows the corresponding band offset between the strained-Si and the relaxed $Si_{1-x}Ge_x$ buffer layers [17]. This is known as the Type-II band alignment, and a band offset of ~6 meV/Ge% is observed for both the conduction and valence bands, relative to the relaxed $Si_{1-x}Ge_x$ layer. Strain-induced band structure modification of Si/SiGe films is found to have a significant impact on the carrier transport properties [18]. This enhances both the electron and hole mobilities.

### Strained-Si Channel MOSFETs

This substrate strain technology works for long- and short-channel devices. Welser et al. [6] reported enhanced electron mobility of 1,620 cm$^2$/V-s with a channel length of 90 $\mu$m. For short-length devices ($L = 35$ nm), Goo et al. [19] reported that the drive current improvement of NMOS devices is ~45% compared to the bulk Si devices. To avoid Ge outdiffusion during the high temperature thermal oxidation process, a low-temperature ($<\sim 700\,^\circ$C) gate oxide is needed for strained-Si layers [20]. The threshold voltage ($V_t$) of strained-Si shows negative shift with respect to bulk Si, due to the lower conduction band edge of strained Si with respect to the bulk Si [21], [22]. The effective electron mobility ($\mu_{eff}$) can be calculated from the drain conductance ($g_d$) and split capacitance-voltage ($CV$) measurements on a large-area device ($L \times W = 100 \times 200\ \mu m^2$).

$$\mu_{eff} = \frac{L}{W} \cdot \frac{g_d}{Q_{inv}} \tag{1}$$

$$E_{eff} = \frac{1}{\varepsilon_s}(Q_b + \eta . Q_{inv}). \tag{2}$$

The inversion carrier concentration $Q_{inv}$ can be obtained from the integration of gate-to-channel capacitance ($C_{gc}$). The extracted $\mu_{eff}$ can be plotted with the effective vertical field, $E_{eff}$. $\varepsilon_s$ is the dielectric constant of the semiconductor. The factor $\eta$ is roughly 1/2 for electron and 1/3 for hole. The details of $\eta$ can be found in [23]. The bulk charge $Q_b$ can be extracted by integrating the body-to-gate capacitance $C_{gb}$. A typical mobility enhancement of strained Si compared to Si is shown in Figure 3 [22]. The enhanced electron mobility can be explained by the conduction band modification induced by the biaxial tensile strain, which lifts the six-fold degeneracy in the conduction band and lowers the energy of the two valleys along the growth direction (001) (Figure 4). The electrons occupy preferentially the two lower energy valleys, which has the low effective in-plane transport mass [24], [25]. Energy splitting also suppresses intervalley scattering. The mobility at the low field ($<\sim 0.4$ MV/cm) is dominated by impurity scattering (Coulomb scattering), the high field mobility ($>1$ MV/cm) is determined by the roughness scattering, and the intermediate field mobility is dominated by the phonon scattering [26]. Note that the effective electrical field is perpendic-



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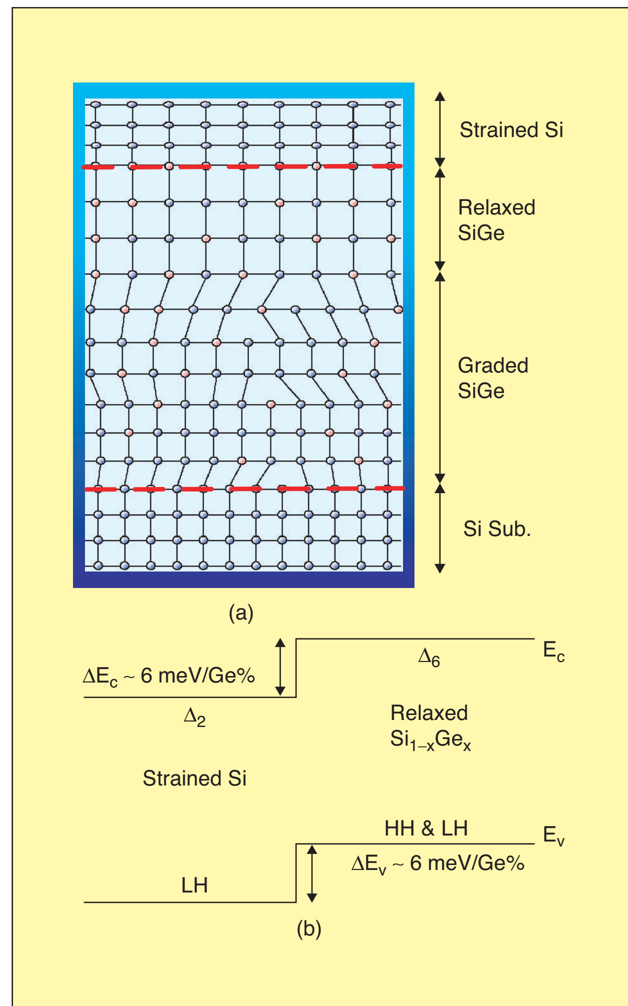
ular to the channel and is controlled by the gate voltage and device structure. Conventionally, the roughness scattering is originated from the oxide/Si interface.

Electron mobility enhancement of substrate-strained Si devices at high channel doping (up to $6 \times 10^{18}/\mathrm{cm}^3$) is reported by Hoyt et al. [26]. If the inversion layer carrier concentration is low, the strain-induced mobility enhancement decreases due to the ionized impurity scattering, but the enhancement recovers at higher inversion charge concentrations, where the screening is more efficient.

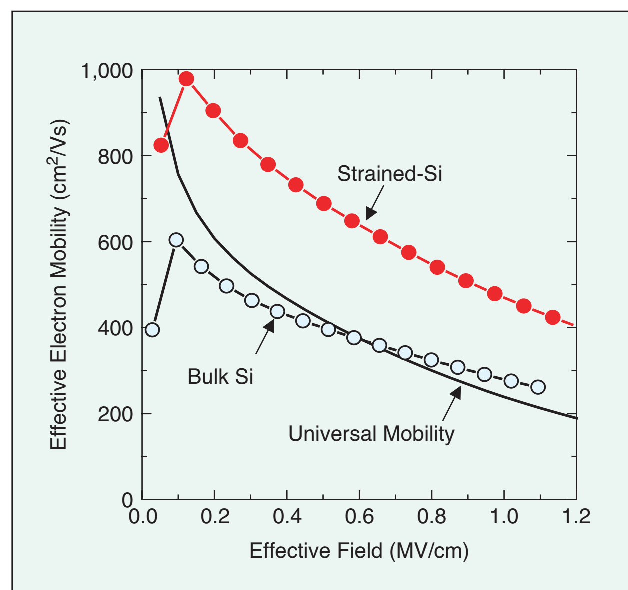
Typical peak hole mobility enhancement is 30–40% (Figure 5) [27]. It is noted that the hole mobility enhancement of strained-Si is mainly due to the large energy splitting $E_{\mathrm{LH-HH}}$ between the light hole (LH) and heavy hole (HH) bands under biaxially tensile strain (Figure 6) [28]. $E_{\mathrm{LH-HH}}$ energy splitting decreases at high effective field ($> 0.3$ MV/cm) due to the large quantum mechanical confinement effects in the inversion heavy holes, which reduces the $E_{\mathrm{LH-HH}}$ energy splitting. Therefore, at the high field (0.6 MV/cm), the hole mobility of substrate-strained Si devices is almost same as that of the bulk Si PMOS devices [29]. Although the mobility of substrate strained-Si is not enhanced at high field, the current-drive enhancement can be attained due to the enhanced boron activation and the reduced boron diffusion in the relaxed SiGe source/drain (S/D) region for the small devices ($L_g = 40$ nm) [30]. Figure 7 shows hole-mobility enhancement versus the effective electrical field as a parameter of Ge fraction (strain) [26]. It is noted that a large Ge fraction ($> 30\%$) is required to improve the hole mobility at the high field of 1 MV/cm [31]–[36].

To maximize both the electron and hole mobilities, strained-Si/-SiGe(Ge) dual-channel structure has been proposed by the MIT group [37], [38]. The NMOS channel forms within the tensile strained-Si layer, while the PMOS channel resides primarily in the compressive strained-$\mathrm{Si}_{1-x}\mathrm{Ge}_x$ layer, as shown in Figure 8 [38]. The tensile strained-Si and compressive strained-$\mathrm{Si}_{1-x}\mathrm{Ge}_x$ layers can be simultaneously grown on the relaxed $\mathrm{Si}_{1-y}\mathrm{Ge}_y$ with $x > y$. The strained-Si surface layer allows the formation of a high-quality interface with a standard-gate dielectric and can serve as a high-mobility electron channel at oxide/strained Si interface. The underneath $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ or Ge layer can provide the buried channel at Si/$\mathrm{Si}_{1-x}\mathrm{Ge}_x$ (Ge) interface for holes, due to higher valence band edge of strained-$\mathrm{Si}_{1-x}\mathrm{Ge}_x$ (Ge) than relaxed $\mathrm{Si}_{1-y}\mathrm{Ge}_y$. The compressive strain gives a lower effective mass and splits the valence band degeneracy. By optimizing the layer thickness and strain of strained-Si/-Ge dual layers on $\mathrm{Si}_{0.5}\mathrm{Ge}_{0.5}$ virtual substrate, the hole and electron mobility can be enhanced by 10 and 1.8 $\times$, respectively [37].

Due to the threads in the channel, the flicker noise $1/f$ can be also increased. For the average distance of the threading dislocations penetrating into the strained-Si channel of $\sim 10$ $\mu$m, the strained-Si device with large area ($> 100$ $\mu\mathrm{m}^2$) has larger flicker noise with respect to control devices due to the penetration of threading dislocation into the channel. The substrate-strained Si devices with the small area ($< 100$ $\mu\mathrm{m}^2$)




*2. The lattice arrangement of (a) strained Si layer on the virtual $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ sustrate structures with increasing the Ge concentration in steps or linearly [5], and (b) the band alignment of the strained-Si on relaxed-SiGe layers [17].*




*3. The effective electron mobility of the substrate strained-Si with the thickness of 20 nm is enhanced ~65 % at the field of 1.0 MV/cm [22].*



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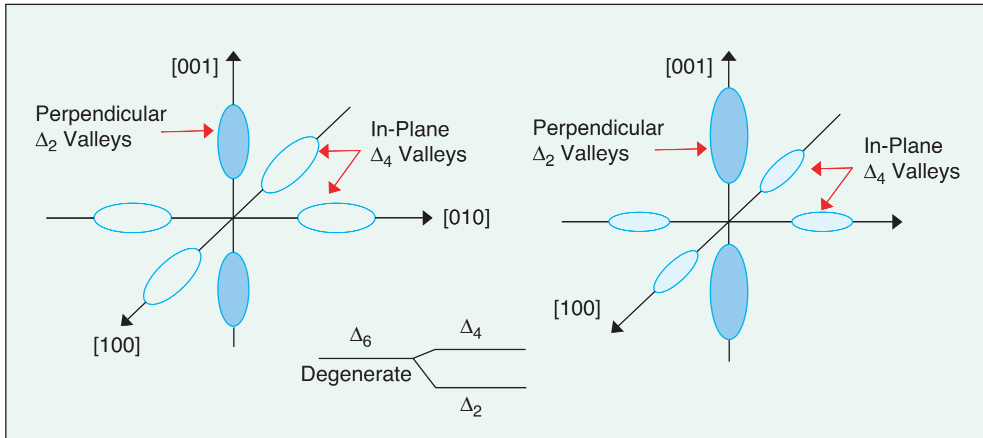
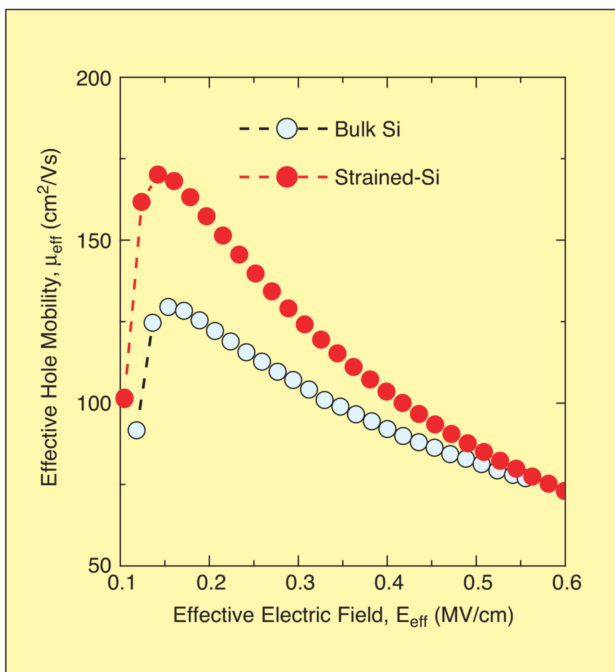
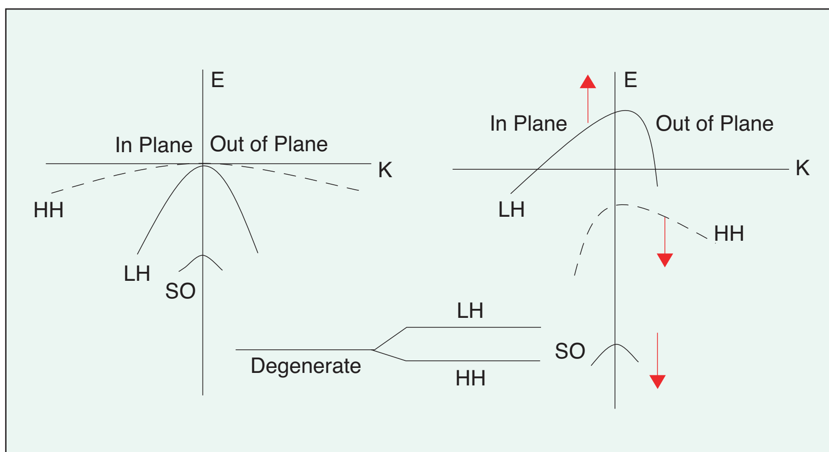



*4. The six-fold degeneracy of electron, before and after biaxially tensile strain [24], [25].*




*5. Hole mobility enhancement is found to be ~30% at the low field under the biaxially tensile strain with the $Si_{0.8}Ge_{0.2}$ buffers, and no enhancement is observed at high field (0.6 MV/cm) due to the quantum confinement effect [27].*




*6. The HH and LH splitting under the biaxial tensile substrate strain [28].*

show the similar flicker noise of the drain current noise $S_{ID}$ to the bulk Si devices. The significant flicker noise is generated by the threads [22], [27].

## Sidewall Strained-Si Channel MOSFETs

Biaxial tensile strained-Si is generally grown on thick relaxed/graded $Si_{1-x}Ge_x$ virtual substrate, but the relaxed $Si_{1-x}Ge_x$ buffer is full of threading dislocations. To solve this problem, Liu et al. [39] proposed a vertical strained-Si MOSFETs. The strained-$Si_{1-x}Ge_x$ below the critical layer thickness is grown on Si substrate. Then, a heavily doped n-type Si layer is grown on the wafer to form the source (or drain). After formation of the Si/SiGe pillar, a 12-nm-thick tensile strained-Si is grown on the sidewall of the pillar (Figure 9). As the lattice constant of Si is adjusted with the lattice constant of the tetragonal $Si_{1-x}Ge_x$ layer, the lattice constant parallel to the sidewall of the pillar is stretched larger than that of bulk Si. The lattice constant perpendicular to the sidewall Si is reduced due to the enlarged Si unit cell in the other directions, resulting in an orthorhombic unit cell instead of a tetragonal unit cell of the strained-Si on the $Si_{1-x}Ge_x$ buffer. Due to the lower symmetry, the band degeneracy is split for holes and electrons. By simulation, the simple orthorhombically-strained-Si grown on the $Si_{0.6}Ge_{0.4}$ sidewall has a $\sim 2\times$ enhancement of electron mobility [40] and a $\sim 3\times$ enhancement of hole mobility [41] compared to bulk Si.

## SGOI MOSFETs

Strained-Si on relaxed SiGe-on-insulator (SGOI) is a promising technology for high-speed and low-power consumption applications because of the combinational advantages of the carrier mobility enhancement and the advantages of Si-on-insulator (SOI), such as low parasitic junction capacitance [34], [42], and fully-depleted devices. The SGOI structure has been demonstrated by separation-by-implanted-oxygen (SIMOX) technology [43] for the buried oxide formation in the implanted region. However, it is difficult to achieve high Ge content (>30%) in SGOI substrates due to the SiGe thermal instability for the high-temperature ($>1,300\,^\circ$C) annealing to form the buried oxide. The wafer bonding and layer transfer technique (also called Smart-cut [44]–[47]) can transfer the relaxed buffer layer onto oxidized Si wafer, and after chemical mechanical polishing (CMP),



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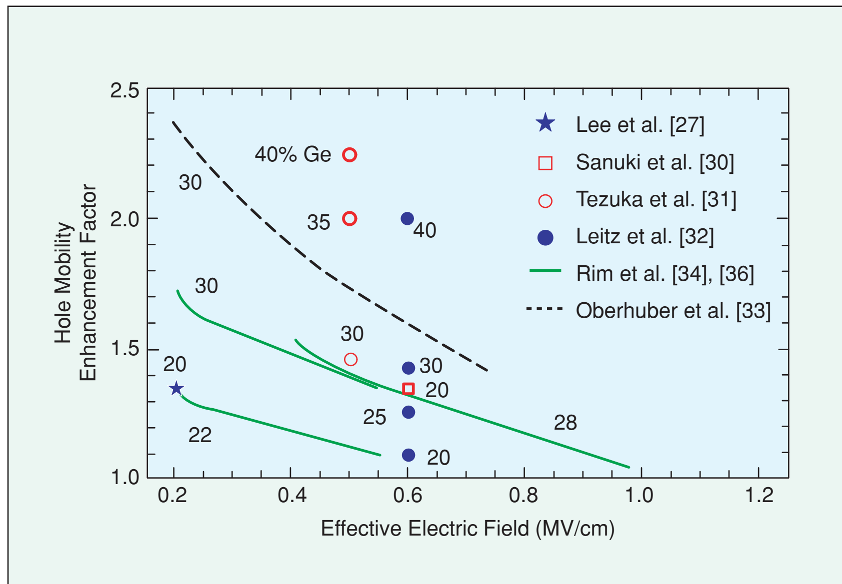
strained Si can be regrown on SiGe buffer layers to form SGOI [33], [48]. The flow diagram of the Smart-cut process is shown in Figure 10.

Fully depleted strained-Si-, N-, and PMOSFETs have been demonstrated on bonded-SGOI substrates with the electron and hole mobility enhancements of 85 and 53%, respectively, and the speed improvement of ring oscillator is 63% compared to control-SOI devices [49]. The hole mobility can be severely reduced due to the Ge diffusion from the SiGe buffer layers to form interface states and fixed-oxide charges [48], [50]. It is important to optimize the thermal budget during the device process to retard the Ge diffusion. Another advantage of SOI devices is that they operate in the lower effective electrical field as compared to bulk devices, resulting to higher mobility enhancement [48].

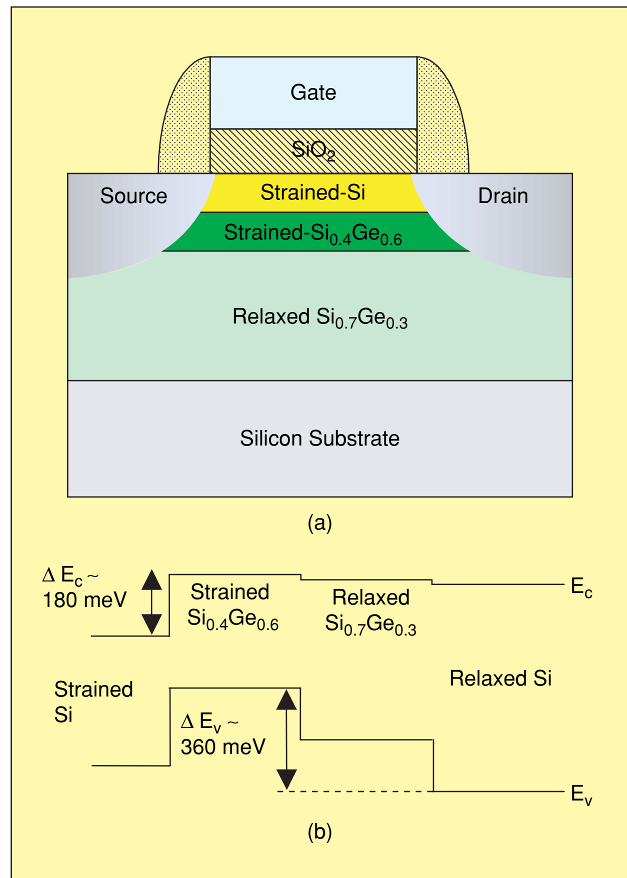



*7. The hole mobility enhancement factor versus effective field. The hole mobility decreases with increasing the effective field. The high-field hole mobility can be increased for the Ge concentration more than 30% in SiGe relaxed buffer layer. The number besides the data corresponds to the Ge fraction in the buffer layers [26].*

## SSDOI MOSFETs

For strained-Si MOSFETs fabricated on bulk substrates (strained-Si/relaxed $Si_{1-x}Ge_x$) and on SGOI substrates, S/D junctions are formed within the SiGe layer, the leakage current increases due to the small bandgap and the defects in $Si_{1-x}Ge_x$. To overcome this issue, an ultra-thin substrate-strained Si can be fabricated directly on insulator with the advantage to suppress the short-channel effects [51] by limiting the path for sub-surface leakage current. The bond and etch-back [52] or smart-cut [51] technique can be used to bond strained-Si directly on oxide-capped Si to SSDOI (strained Si directly on insulator) after removing the residual relaxed SiGe buffer. The SSDOI has high thermal stability up to 1,000 °C.

The electron and hole mobility enhancement of SSDOI with the strain equivalent to $Si_{0.65}Ge_{0.35}$ relaxed buffers are ~125 and ~42%, respectively, as compared with bulk SOI devices [51]. Figure 11 shows the electron and hole mobility of SSDOI devices fabricated by the Bond and Etch-back technique [52]. The electron mobility can be enhanced ~100% as compared with the bulk SOI devices, independent of electric field. Hole mobility can be improved ~50% for the SSDOI with strain equivalent to $Si_{0.6}Ge_{0.4}$ at the electric field of 0.5 MV/cm. The absence of a $Si_{1-x}Ge_x$ layer underneath the strained-Si layer is beneficial, since the Ge-containing structures have shown mobility degradation associated with Ge outdiffusion at comparable strained-Si thickness [48]. Furthermore, the elimination of the SiGe layer yields a thin body, which makes possible the fully depleted devices, double-gate devices, and FinFETs using strained Si.




*8. (a) A typical MOSFET structure of the dual channel FET and (b) the corresponding band alignment of the dual channel structure [38].*

### Hetero-Orientation Technology

The drive current can be enhanced using the different crystal orientation other than conventional (100) substrate [53]. The PMOS and NMOS devices can be fabricated on (100), (110) and (111) substrates with the channels at different crystal directions such as <111>, <112>, <110> and <100>, shown in



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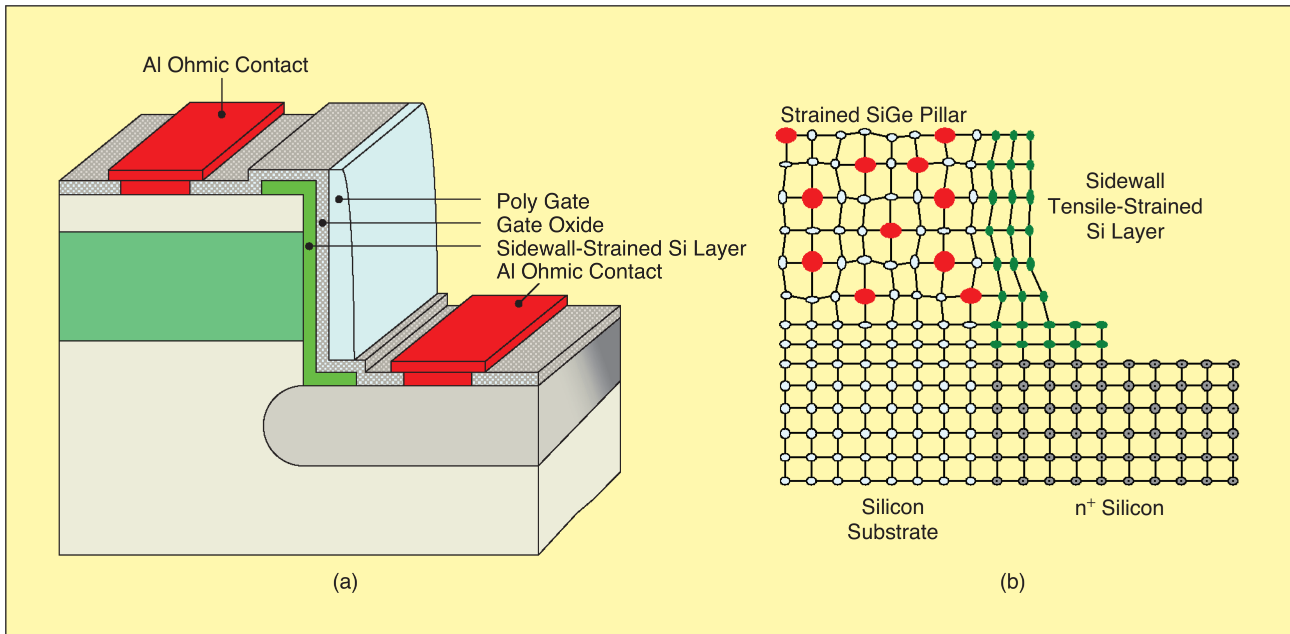
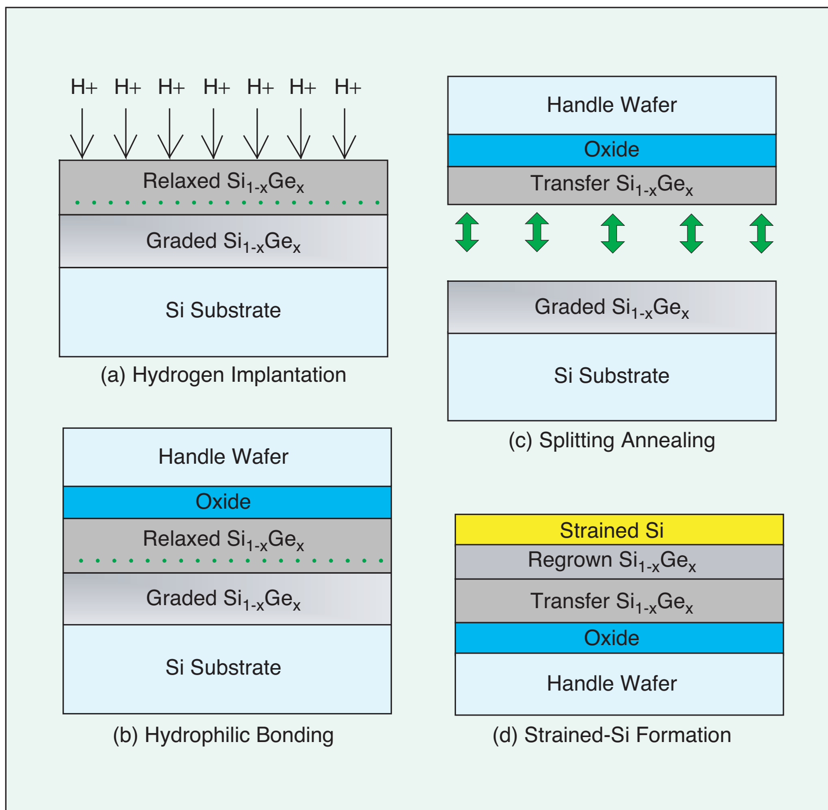



*9. (a) Schematic diagram and (b) lattice structure for sidewall strained-Si MOSFETs [39].*




*10. Process flow for the fabrication of strained-Si on SiGe-on-insulator substrates by wafer bonding and layer transfer techniques. First, hydrogen ions are implanted into the relaxed $Si_{1-x}Ge_x$ layer to form a deep weakened layer. Hydrophilic bonding with a $SiO_2$-capped wafer is carried out, followed by a high temperature (≥ 800 °C) to induce layer transfer along the weakened hydrogen-implanted regions by H2 blistering. Finally, strained-Si is grown after regrowth of the second SiGe buffer layer [44].*

Figure 12 [54], [55]. The PMOS ($L_g = 45$ nm) can have 30% improvement of the drive current for the channel along <110> direction on (110) substrate as compared with the channel <110> on (100) substrates [54]. The highest electron mobility with the oxynitride gate dielectric is reported along the <110> channel on (100) substrate [Figure 13(a)] [56]. The highest hole mobility is observed along the <110> channel on (110) substrate. At the inversion charge density of $\sim 6 \times 10^{12}$ cm$^{-2}$, the hole mobility of <110>/(110) devices is increased by ~160% as compared with the <110>/(100) device [Figure 13(b)] [56]. Channel directions affect both hole and electron mobility dramatically on (110) substrate but relatively little on (111) substrate. The orientation dependence of mobility is caused by the anisotropy of the band structure.

The drive current of n-channel MOSFET on (100) substrate is two times higher with respect to the p-channel MOSFET with the same channel width on the same substrate due to the lower hole mobility. To match the current drive of NMOS and PMOS devices on (100) substrates, the channel width of PMOS should be at least two times larger in logic circuit applications. The electron and hole mobilities on (110) substrates are almost equal when the channel is along <110> direction. However, gate oxide grown on (110) substrate has a rough Si/$SiO_2$ interface and larger thickness variation. This detrimental orientation dependence of gate dielectric reliability might be reduced for high-$\kappa$ gate materials. The similar trend of the mobility enhancement is observed for the devices with $HfO_2$



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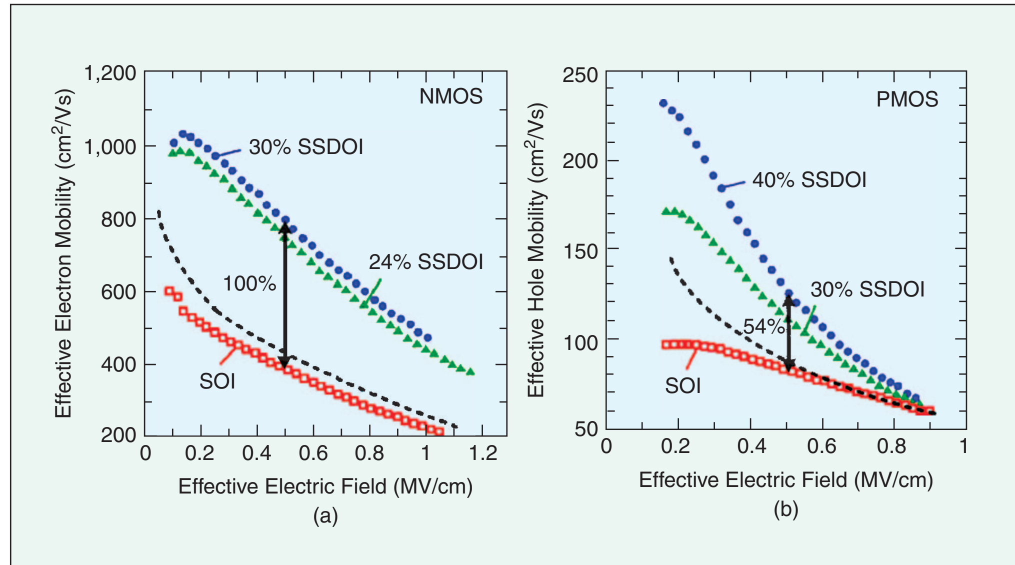
gate dielectrics, where the mobility degradation due to the high-$\kappa$ is about 5–10% compared with oxide [57]. To take the maximum advantage of crystal orientation dependence on carrier mobility, NMOS should be fabricated on (100) surfaces while PMOS should be fabricated on (110) surfaces.

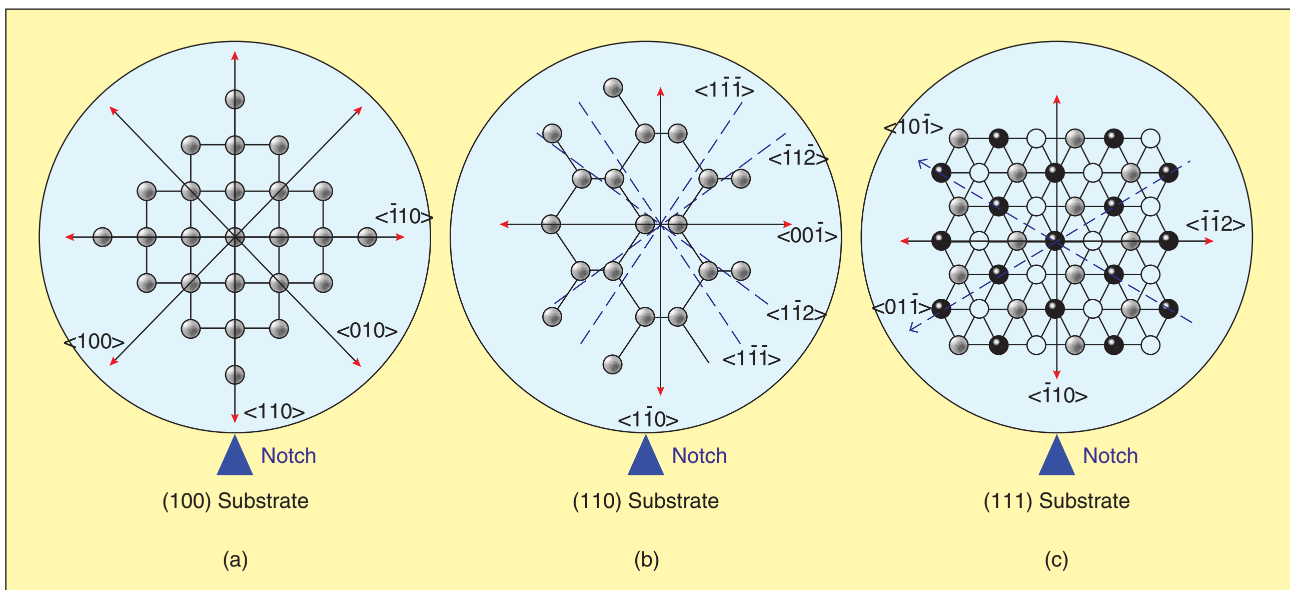
To integrate the NMOS on (100) substrates and PMOS on (110) substrates, the hybrid substrate on SOI is used by IBM [56]. A schematic cross-section of CMOS on hybrid substrate is shown in Figure 14. The PMOS on (110) SOI and NMOS on (100) Si epitaxial layer or NMOS on (100) SOI and PMOS on (110) Si epitaxial layer can be fabricated by layer transfer technique through wafer bonding or smart-cut process. The electron mobility on (100) epitaxial Si is slightly better than that on (100) control substrate, the hole mobility on (110) epitaxial Si is 2.5 times higher than that of (100) control substrate, and the gate delay has been improved by 21% [58]. To investigate the RF performance of CMOS ($L_g = 80$ nm) devices on Si substrates with various orientations, the cut-off frequency $f_T$ is observed to be 157 GHz for NMOS on (100) substrate, and 107 GHz for PMOS on (110) substrate at the $V_{ds}$ of 1.5 V. The $f_T$ enhancement of PMOS on (110) substrate is ~40% compared with the (100) substrate [56].




*11. The (a) electron and (b) hole mobility of strained-Si directly on SOI by bond and etch-back technique. The electron mobility is enhanced 100% and relatively independent on the electric field. The highest hole mobility of 127% is observed at the electric field of 0.2 MV/cm. The universal mobility is also plotted (dash line) [52].*

## Germanium Channel on Bulk and Virtual Substrate

Germanium MOSFET is a one of the promising candidates to increase both the electron and hole mobilities. Ge MOSFET technology can be useful for mobility improvement and can be suitable for integration of the monolithic optical fiber receivers as well [59]. The Ge NMOSFET ($W \times L = 110 \times 6\ \mu\text{m}^2$) fabricated on <111> p-type Ge wafer with a 25-nm-thick nitrided gate oxide has an effective mobility of ~940 cm$^2$/V-s in 1988 [60]. However, the high mobility obtained by Rosenberg et al. [60] in the late-1980s is not reproduced in more recent work on Ge MOSFETs with high-$\kappa$ gate dielectrics. The reason for this is still not completely understood. The hole mobility on the <100> p-type Ge wafer is ~770 cm$^2$/V-s with gate width of 40 $\mu$m and gate length of 7 $\mu$m [61]. To prevent Ge diffusion into the gate




*12. The different channel orientations on (a) (100) substrate, (b) (110) substrate, and (c) (111) substrates [54], [55].*



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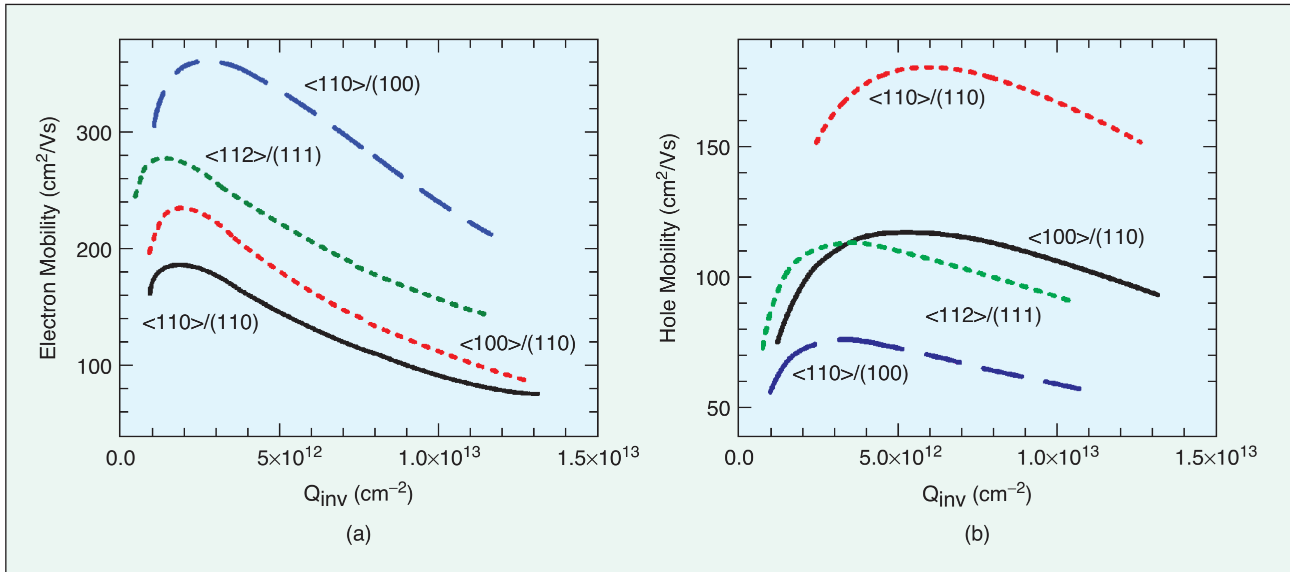
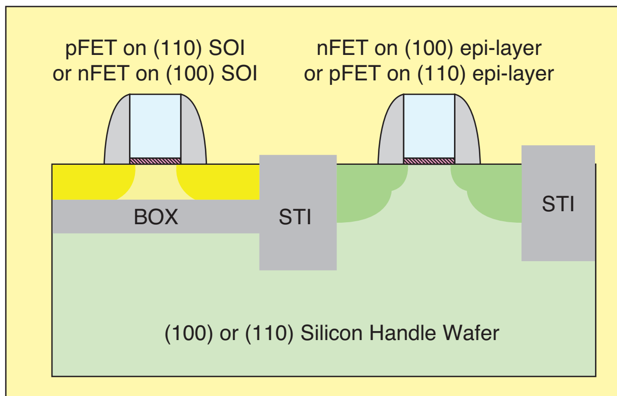



*13. (a) Electron and (b) hole mobilities in the inversion layers with the substrate orientations. The electron mobility is highest on <110>/(100) substrate while hole mobility is highest on <110>/(110) substrates [56].*




*14. Schematic cross section of CMOS on a hybrid-substrate with PMOS on (110) SOI (or NMOS on (100) SOI) and NMOS on (100) substrate (or PMOS on (110) substrate) orientation [56].*

dielectrics, nitridation on the Ge surface is used. Then, the high-$\kappa$ gate dielectric $ZrO_2$ [62] or $HfO_2$ [63] is deposited on bulk Ge wafers to reduce the thermal budget (400 °C). Due to the small abundance of Ge in the nature, it is not practical to have mass production of bulk Ge VLSI, while Ge epi on Si substrate or Ge on insulator seem to be more promising for mass production. The Ge channel PMOSFET with biaxial compressive strain is fabricated on $Si_{1-x}Ge_x$ ($x = 0.7$ to 1) buffers on Si substrate. To avoid the germanium oxide and to improve the oxide/semiconductor interface, a thin Si cap layer is used, and the hole mobility can be improved 8× compared to the bulk Si devices [64]. The germanium PMOSFETs fabricated on $Si_{0.3}Ge_{0.7}$ buffers with a direct high-$\kappa$ $HfO_2$ dielectric has the hole mobility enhancement of 2× with respect to bulk Si devices [65].

### Germanium Channel on GOI

The combination of the high mobility Ge channel and ultra-thin Ge-on-insulator (GOI) structure is expected to improve device performance with similar advantages to the SOI [66]. The Ge has a lower band gap, resulting in the large off-current. Therefore, it is more realistic to use the Ge channel only where high-performance transistors are needed in an integrated circuit (IC), rather than to use a blanket SiGe buffer or bulk Ge. The condensation of strained SiGe-on-insulator (SGOI) can produce a compressively strained Ge-on-SOI substrate. The process of condensation technique is shown in Figure 15 [67].

The $Si_{1-x}Ge_x$ layer with a low Ge fraction of 0.15 is grown on an SOI. Then, the thermal oxidation is performed at lower temperature than the melting point of SiGe. In the oxidation process, Ge atoms are bound between the top and bottom $SiO_2$ layers and stay in the SiGe layer after oxidation. By proper oxidation process, the total amount of Ge in the SiGe layer is preserved. The Si and SiGe layers are merged together, resulting in the increase of Ge fraction and the decrease of SGOI thickness. Local condensation can be obtained by a nitride mask outside the channel region, similar to local oxidation (LOCOS). Local condensation can also partially reserve the compressive strain in the resulting Ge layers. In this structure, the peak hole mobility is observed to be 1,590 $cm^2$/V-s (Ge = 93%, strain = 1.3%), which corresponds to 10× the Si universal hole mobility (Figure 16) [68]. This high hole mobility is due to the combination of the compressive strain and the high Ge fraction in the channel. The local condensation can avoid the buckling of the thin Ge films [69] and can be compatible with the strained-Si n-channel devices on the same substrates. Another potential advantage of LOCOS is to reduce off-current by the large bandgap Si at S/D, as compared with Ge S/D. A key challenge to fabricate Ge NMOS devices is that the S/D regions cannot be doped sufficiently heavily due to low solid-solubility for the n-type impurities if Ge S/D is used [70].



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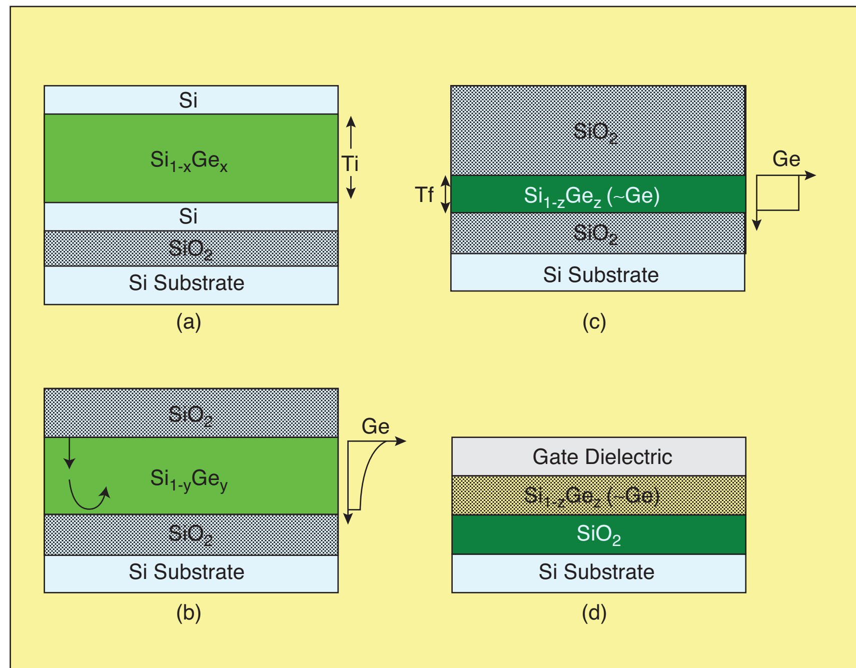
### Ge Transistors with Different Orientation

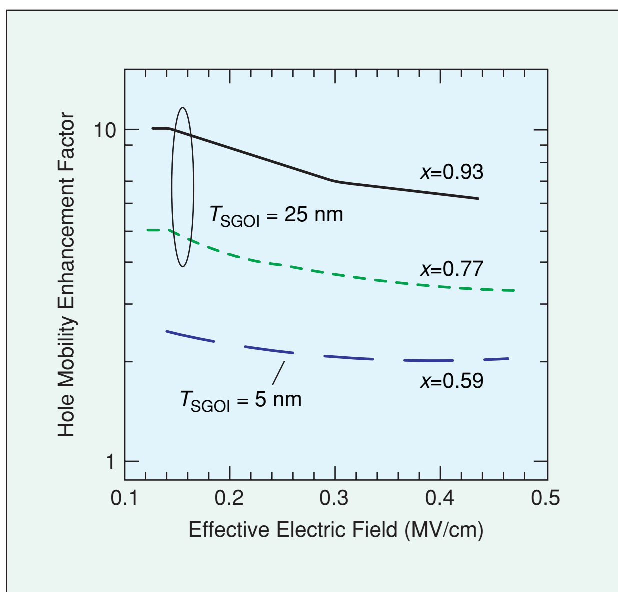
The 8-L conduction valleys and a highly warped valence band of Ge result in significant effects of substrate orientation and channel direction on Ge device performance. In general, the L valleys have smaller transport effective mass than Δ valleys, and more population in L valleys can have higher electron mobility [71]. Both the vertical field (controlled by gate voltage) and the film thickness determine the carrier population in the channel. The theoretical prediction of electron mobility in the literature for different Ge orientation is summarized in the following. For the bulk Ge, the phonon-limited (low field mobility) is higher on (111) substrate than (100) substrate for the carrier concentration larger than $2 \times 10^{12}$ cm$^{-2}$, the order is reversed for less carrier concentration [72]. Note that the higher carrier concentration indicates the higher vertical field in the channel. For GOI with the constant carrier concentration of $2 \times 10^{12}$ cm$^{-2}$, (111) substrate has a higher phonon-limited mobility than (100) substrate for GOI thickness less than 10 nm, and the order is reversed if the Ge thickness more than 10 nm [72]. For the ballistic transport ($L_g < 30$ nm) in double gate devices, (110) substrate has the highest drive current as compared with (111) and (100) substrate [71]. For the surface-roughness limited mobility (high field mobility), (111) substrate is better than (110) and (100) substrate [71]. More results on this issue are expected in the near future. There is limited literature regarding the Ge PMOS on different orientations. Due to the similar valence band structure between Si and Ge, it is expected that <110> channel direction on (110) substrate has the highest hole mobility, similar to Si PMOSFET. The strain in Ge can also change the mobility and has not been considered in the previously mentioned literatures.

## PROCESS-INDUCED STRAIN

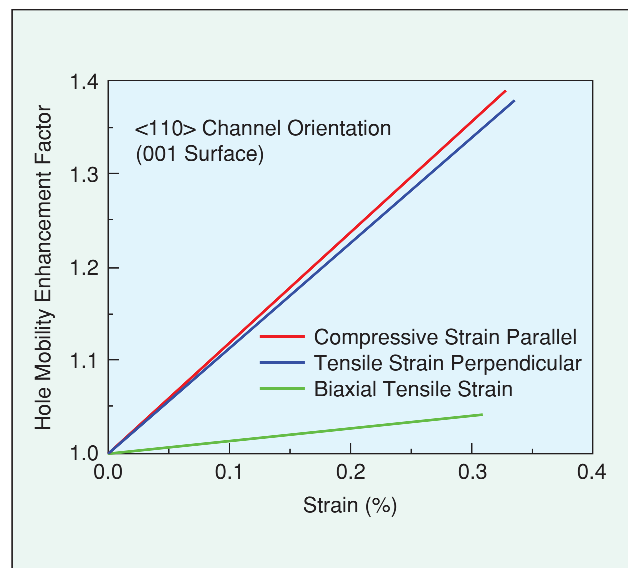
Substrate-strain results in biaxial strain to channel and enhances electron and hole mobilities. However, cost,




*15. Process flow for Ge condensation method. During the oxidation process, the SiGe layer thickness decreases and Ge concentration increases. Finally, the top $SiO_2$ is etched and gate oxide or high-κ can be deposited on the strained-Ge layer for FET process ("Ti" and "Tf" are the initial and final thickness of SiGe layer, respectively) [67].*




*16. The increasing hole mobility enhancement factor with the increasing Ge fraction in the buffers [68].*




*17. The hole mobility enhancement vs strain. The mobility enhancement is higher for the uniaxial compressive strain parallel to the channel [73].*



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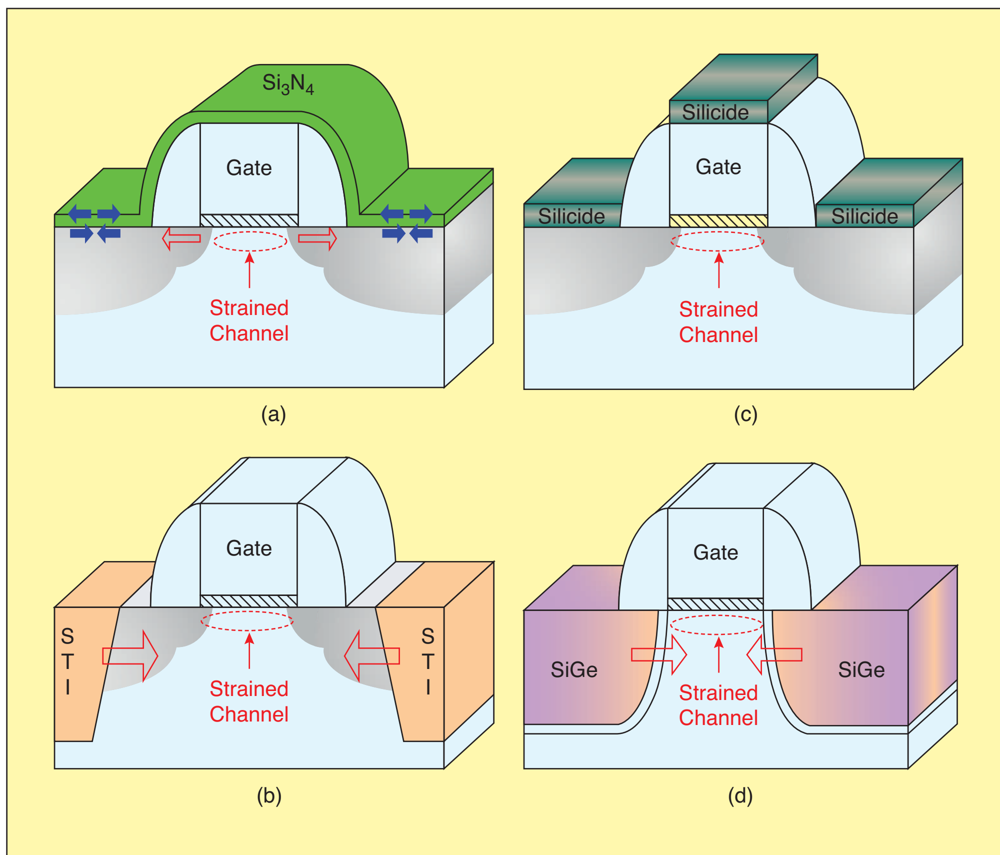
scalability, and complexities such as low-defect $Si_{1-x}Ge_x$ buffers, low thermal budget, and integration, remain issues for production. Moreover, the hole mobility of the Si channel at high fields is not improved significantly except at the Ge or dual channel because the energy separation between light and heavy hole bands is not enough due to the quantization effect. In contrast, uniaxial strain offers similar electron mobility enhancement compared with biaxial strain, while the hole mobility improvement is more significant at high field (Figure 17) [73]. For <110> channel orientation on (100) substrates, the uniaxial compressive strain parallel to the channel and the uniaxial tensile stress transverse to the channel result in larger hole mobility enhancement than biaxial tensile strain at the same stress level. Hole mobility enhancement with these uniaxial stresses is mainly due to band warping, resulting in the decrease of the transport effective mass along the <110> direction [74]. Furthermore, these uniaxial strains may have lower surface roughness scattering due to the large out-of-plane effective mass (less wave function penetration into dielectrics) [73]. Process-induced strain has been used to produce the desired uniaxial strain [75], [76]. Several approaches (Figure 18) such as silicon nitride ($Si_3N_4$) cap layer, shallow-trench isolation (STI), silicidation processes, and embedded SiGe S/D have been utilized to realize the local strain [77]–[79].

> Applying stress to induce appropriate strain in the channel region of MOSFETs increases both electron and hole mobilities in the strained channel.

Silicon nitride film is well-known to produce a high level of stress [Figure 18(a)]. $Si_3N_4$ film can have either tensile or compressive strain depending on the deposition conditions, and the drive currents of both n- and p-channel MOSFETs can be improved by controlling the stress of the $Si_3N_4$ layer selectively. The tensile cap layer deposited by thermal chemical vapor deposition (CVD) can improve the performance of NMOS due to the induced tensile strain in the channel region, while the compressive cap layer deposited by plasma-enhanced CVD can improve the PMOS due to the induced compressive strain in the channel region [77]–[80]. Shimizu et al. reported that a highly tensile strained $Si_3N_4$ cap layer can improve NMOS performance but degrade PMOS performance [77]. Capping a highly-tensile $Si_3N_4$ layer shows 25% NMOS drain current improvement [81], while selective Ge implanted into the capping layer can recover the degradation of PMOS devices [82].




*18. Schematic features of the various process strain: (a) silicon nitride capping layer to create a tensile channel [77], (b) STI to create a compressive channel [75], (c) silicide strain, and (d) embedded SiGe S/D process strain to create a compressive strain [79].*

STI is frequently used for lateral isolation in deep submicrometer technology. With the scaling down of CMOS technology, MOS devices become more sensitive to device layout patterns. STI-induced compressive strain in the channel region increases rapidly with decreasing distance between the STI edge and the transistor region [Figure 18(b)], [83], [84]. Sanuki et al. reported [30] that the drive current of PMOS devices with 40-nm gate length and S/D length of 240 nm can be improved by 11%, and the ring oscillator delay is improved by 18%. The high halo dose and high



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parasitic resistance can offset the current enhancement by the local strain benefits [85].

> To be practical for VLSI applications, mobility-enhancement technology has to be low cost and high performance.

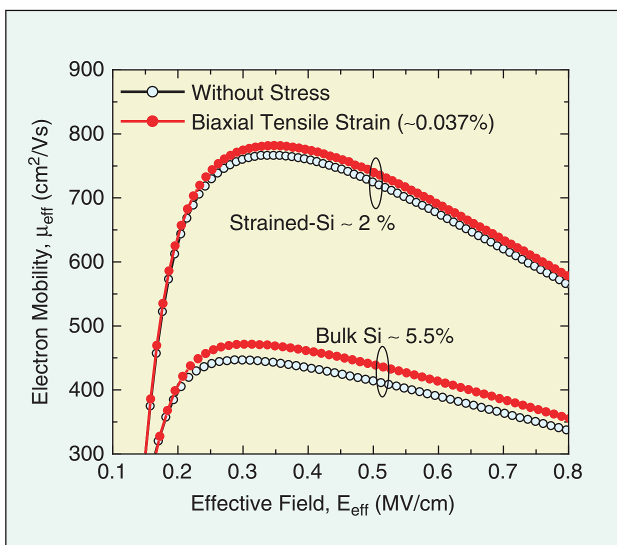
Mechanical stress exceeding 400 MPa can be obtained in the patterned silicide structures, due to the difference in thermal expansion coefficient between the silicide and silicon, and lattice mismatch between the silicide and Si in case of epitaxial alignment [86], [87]. Note that the common silicides ($TiSi_2$, $CoSi_2$, and NiSi) have larger thermal expansion coefficient than Si and yield compressive Si underneath. However, when the stress exceeds the critical shear stress, the dislocations detrimental to the devices can be generated. A typical silicide structure is shown in Figure 18(c). The combinational effects of STI, cap-layer, and silicide for both PMOS and NMOS devices are reported by Ge et al. [78]. With optimized stress engineering of these three processes, both N- and PMOSFET improvements up to 15% are reported with the ring oscillator speed enhancement of 5–10% [78].

The strained PMOS transistor features an epitaxially grown strained SiGe film embedded in the S/D regions using a selective epitaxial growth was reported by Intel [Figure 18(d)] [79]. The source and drain regions, made of an alloy of $Si_{1-x}Ge_x$, are deposited in the recessed source and drain region. The lattice constant of the SiGe alloy is larger as compared to the bulk Si due to the inclusion of Ge. The larger lattice constant of $Si_{1-x}Ge_x$ creates a compressive stress in the channel of a 45-nm gate length transistor between the source and drain regions, thereby resulting in significant hole mobility improvement (>50%) with 17% Ge incorporation. It is interesting to note that hole mobility is also enhanced at the high field region for the uniaxial compressive strain parallel to the channel. By integrating and taking advantage of aforementioned strain engineering techniques, CMOS performance can be further improved.

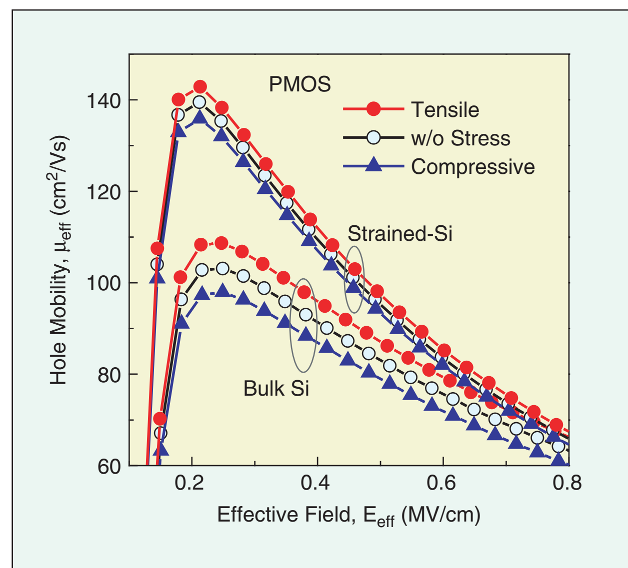
As a final note for process-induced strain, the process strain is effective for the 90-nm node and beyond, but its enhancement effect diminishes for large channel devices.

## PACKAGE STRAIN

Substrate-strained Si (strained Si on SiGe buffer) shows significant electron mobility improvement at low and high fields, but hole mobility is only improved at low field. Furthermore, the $Si_{1-x}Ge_x$ buffer suffers the threading defects, thermal budget, and production cost. Process-strain technology can improve the current drive and the mobility of NMOS and PMOS devices at low and high field regions due to the appropriate local strain, but it can be only applied to short channel devices ($L_g < \sim 100$ nm). Alternatively, strain on the Si channel can be induced by bending the Si wafer directly (mechanical strain) or by bending a package substrate with an Si chip glued firmly on its surface (package strain). Package-strain (mechanical strain) can improve the NMOS and PMOS device performance after the fabrication of VLSI. Package strain can be applied to both short- and long-channel devices, and the cost is relatively low. Package-strain can be applied uniaxially by one-end-bending method [88], [89] or four-point-bending method [90], [91]. Biaxial strain can be produced by the displacement of the center of the wafers [92]. This biaxial package strain is similar to the strain produced by relaxed SiGe virtual substrate. For practical applications, the IC package can produce the external mechanical strain to the devices, therefore, the term "package strain" is used.




*19. The mobility enhancement of the bulk Si and substrate-strained Si NMOS devices under the biaxial tensile package strain. The bulk Si NMOS shows the higher mobility enhancement as compared to the substrate-strained Si devices [97].*




*20. The change of hole mobility for bulk Si and substrate-strained PMOS devices under the uniaxial strain (0.097%) perpendicular to the channel [97].*



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In 1954, Smith [93] reported that the piezoresistance effect in Si and Ge is about 100× higher compared to metallic conductors. This effect is applied popularly in mechanical sensor devices. The uniaxial bending of p-type inversion layers was reported by Colman et al. [88] in 1968, and the n-type inversion layer was reported by Dorda [89] in 1971. The effective electron mobility of the short channel NMOS devices ($L_g = 45$ nm) is enhanced by ~5% under the uniaxial tensile strain (~0.12%) parallel to the channel [94]. It indicates that MOS devices are very sensitive to mechanical stress [95]. Electron mobility for long-channel devices ($L_g = 20\ \mu$m) can be improved ~15% with the uniaxial tensile strain (~0.031%) perpendicular to the channel [96]. Short-channel devices show lower mobility enhancement compared with long-length devices [97]. The electron mobility of NMOS devices is enhanced under all tensile conditions. Drive-current enhancement under the uniaxial tensile strain parallel to the channel is higher than that under the uniaxial tensile strain perpendicular to the channel. The drive current of NMOS devices is reduced under compressive strain conditions [98]. Mobility enhancement by the package strain is also observed for substrate-strained NMOS devices [97]. The electron mobility of bulk Si and substrate-strained Si NMOS devices increases under the biaxial tensile package-strain (Figure 19) [97]. Electron mobility enhancement of bulk Si devices under biaxial tensile package-strain is 2–3× higher than that of the substrate-strained Si devices, since the slope of the electron mobility enhancement factor at low tensile strain (<0.1%) is almost 2.5× of that at high substrate-strain at 0.64% [99].

**Table 1. The package-strain effect on the NMOS and PMOS device performances.**

| Package-strain | NMOS | PMOS |
|---|---|---|
| Strain parallel to channel | | |
| Tensile | Improve | Degrade |
| Compressive | Degrade | Improve |
| Strain perpendicular to channel | | |
| Tensile | Improve | Improve |
| Compressive | Degrade | Degrade |
| Biaxial strain | | |
| Tensile | Improve | Improve* |
| Compressive | Degrade | Improve |

*degraded at small strain.

The effective hole mobility of bulk Si PMOS devices increases with the uniaxial tensile (compressive) strain perpendicular (parallel) to the channel, while the mobility decreases under the compressive (tensile) strain perpendicular (parallel) to the channel. The similar trend of mobility change is observed for both bulk and substrate-strained PMOS devices with the strain (~0.097%) perpendicular to the channel (Figure 20) under the tensile and compressive conditions [97]. The biaxial mechanical strain has different response from bulk Si and substrate-strained Si devices due to the strain compensation of package strain and substrate strain and the abnormal dependence of conduction effective mass on biaxial strain [100]. The uniaxial compressive

**Table 2. The improvement of the mobility and drive current of MOSFET devices as compared to bulk Si using the substrate-strain, process-strain and package-strain technologies.**

| Strain technology | Strain mechanism [strain (%)] | Gate length | Enhancement (%) Mobility | Enhancement (%) Drive current | Device | Reference |
|---|---|---|---|---|---|---|
| Substrate-strain | Virtual substrate (~1.2) | 300 nm | 120 | 70 | NMOS | [35] |
| | | | 42 | 50 | PMOS | [35] |
| | | 300 nm | — | 90 | PMOS | [101] |
| | | 100 nm | 110 | — | NMOS | [36] |
| | | | 45 | — | PMOS | [36] |
| | | 60 nm | — | 15 | NMOS | [102] |
| | | 40 nm | — | 19 | PMOS | [30] |
| | Strained-Si/strained -Ge dual channel (~2) | 50-200 $\mu$m | 80 | — | NMOS | [37] |
| | | | 900 | — | PMOS | [37] |
| | SGOI (~1.0) | 65 nm | 85 | — | NMOS | [49] |
| | | | 53 | — | PMOS | [49] |
| | SSDOI (1.67) | 100 $\mu$m | 100 | — | NMOS | [52] |
| | | | 140 | — | PMOS | [52] |
| | Orientation effect on bulk Si | 80 nm | 90 | — | NMOS | [56], [57] |
| | | 40 nm | 160 | 45 | PMOS | [56], [57] |
| | Bulk Ge channel | 2–200 $\mu$m | ~100 | — | PMOS | [62] |
| | Strained-Ge (~0.8) | 3–100 $\mu$m | 100 | — | PMOS | [65] |
| | Ge channel on SOI (~1.3) | 20 nm | 900 | — | PMOS | [68] |
| Process-induced strain | $Si_3N_4$ Capping layer | 65 nm | — | 25 | NMOS | [81] |
| | | 40 nm | — | 60 | PMOS | [103] |
| | Ge implantation | 70 nm | — | 20 | PMOS | [77] |
| | STI | 40–45 nm | — | 11–20 | PMOS | [30], [85] |
| | $Si_3N_4$, STI, and silicide | 90 nm | — | 15 | NMOS | [78] |
| | | | 45 | 45 | PMOS | [78] |
| | $Si_3N_4$ capping layer | 45 nm | — | 10 | NMOS | [73] |
| | SiGe in S/D | 50 nm | 55 | 60 | PMOS | [73] |
| Package-strain | Uniaxial tensile strain perp. to channel (0.039) | 0.25 $\mu$m | ~15 | 15 | NMOS | [96] |
| | Uniaxial comp. strain parallel to channel (0.2) | 25 $\mu$m, 0.6 $\mu$m | 20 | 30 | PMOS | [100] |



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(tensile) parallel (perpendicular) to the channel is more preferable to improve hole mobility than that of biaxial tensile strain. To improve CMOS circuit performance, uniaxial tensile package-strain can be applied along the NMOS channel direction, and all the PMOS channels are perpendicular to NMOS channels in the circuit layout [100]. A 7% speed enhancement is obtained for the ring oscillator. A summary of mobility enhancement and degradation under six strain conditions for NMOS and PMOS is given in Table 1.

## CONCLUSION

To be practical for VLSI applications, mobility-enhancement technology has to be low cost and high performance. The new material and new substrate orientation approaches offer mobility enhancement, but process complexities, such as thermal budget, contamination, and new material process, can lead to a high cost. However, exploiting processes available in current VLSI fabrication to produce desired strain can be cost-effective with reasonable enhancement. Package-strain is modular technology, which is applied after the ICs fabrication without the introduction of new process, and the enhancement is satisfactory for most applications. The combination of new material (new orientation), process-induced strain, and package strain continues to improve future performance. Table 2 summarizes the results of all the technologies described in this review.

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*Chee Wee Liu* (chee@cc.ee.ntu.edu.tw), *S. Maikap*, and *C.-Y. Yu* are with the National Tawain University in the Republic of China.

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