

A Linear-Approximation Technique for Digitally-Calibrated Pipelined A/D Converters

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Abstract—Open-loop amplifiers enrich high-speed capability of pipelined analog-to-digital converters (ADCs). Because both finite gain and circuit nonlinearity limit the accuracy of this approach, a linear-approximation calibration technique is proposed to compensate such non-ideal effects. Due to the nature of two phase requirements, double sampling technique is applied to achieve continuous-time on-line calibration without interrupting the normal data conversion. Pushing the complexity of calibration into the digital domain relaxes the stringent design requirements of analog circuits.

I. INTRODUCTION

High-speed ADCs are dominated by flash or folded architecture [1], [2]. For their exponential growth of complexity and parallel conversion, both approaches consume much power and occupy more chip area. Pipelined architecture is popular in the medium to high-speed data converters. Linear growth of circuits complexity makes pipelined ADCs more efficient in power consumption and circuit area. Conventional pipelined stages consist of closed-loop amplifiers which must meet both high-gain and wide-bandwidth requirements [3]. This approach consumes much power and increases circuit complexity. And the adjoint parasitic elements of complex circuits limit the conversion rate of such architecture. Recently, open-loop residue amplification method is applied to ease such limitation. Simple structure of open-loop amplifier [4] achieves high speed conversion rate. Without using feedback mechanism to linearize the amplification, the non-linearity effect of the amplifier must be compensated. Statistic digital calibration technique is adopted to overcome the effects of non-linearity. But this technique needs large number of data and longer time to get the correct parameters.

Digital circuits are efficiently scaled down and speed up by the advance of chip fabrication technology, while analog circuits suffer from the shrunk voltage head room of descendant supply voltage in deep-submicron technology. The size and speed of analog circuits can not benefit from the advanced process. With the aid of calibration and pushing the complexity of calibration into the digital domain can ease these stringent requirements of analog circuits.

In this paper, a linear-approximation technique is proposed to compensate the circuit nonlinearity in digital domain. This technique ensures the improvement of linearity

and continuous-time calibration without interrupting normal conversion. Section II introduces the linear approximation calibration method. In Section III, the implementation of digital background calibration is described. Simulation results are presented in Section IV, and Section V summarizes with a conclusion.

II. LINEAR APPROXIMATION

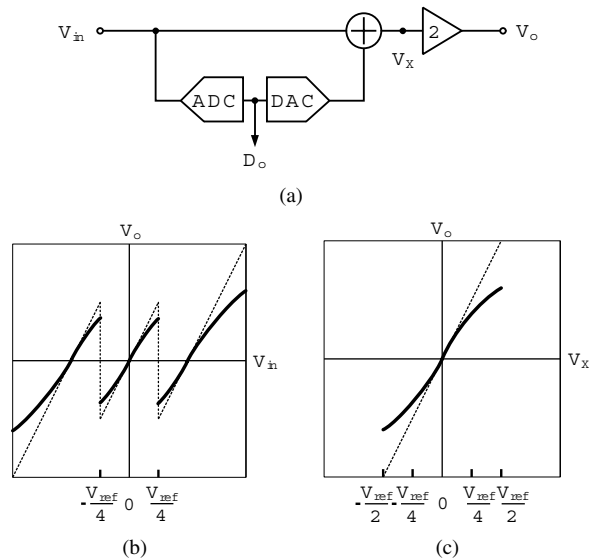


Fig. 1. (a) 1.5-b pipelined ADC stage. (b) Stage transfer curve. (c) Amplifier transfer curve.

A. Transfer Function Estimation

The basic stage architecture of 1.5-b/stage pipelined ADC is shown in Fig. 1(a). Conventional approaches use multiplier DAC (MDAC), consisting of a coarse DAC and a feedback amplifier, to provide interstage gain. The open-loop amplifier architecture separates multiply-by-2 amplifier stage from DAC. To increase the immunity of comparator offset and operate in high speed, 1.5-b/stage is selected. The transfer characteristic between V_{in} and V_o is shown in Fig. 1(b). The dotted line denotes the ideal curve. In high-speed data converters, their nonlinearity mainly arises from the amplifier

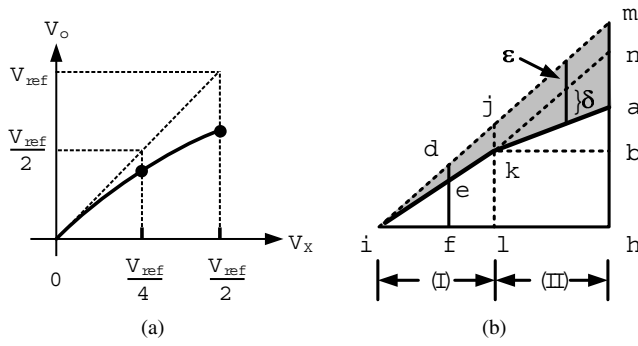


Fig. 2. (a) Amplifier transfer curve between origin and $V_{ref}/2$. (b) Linear approximation.

distortion. Because of gain compressing and nonlinearity, the actual curve is denoted by the solid line. Because the multiply-by-2 amplifier simply multiplies the input, V_X , by two, the transfer curve between V_X and V_o can be illustrated in Fig. 1(c). The nonlinearity becomes more serious for larger input. Because the transfer curve of differential circuits is symmetric to origin, only the positive input needs to be considered. Furthermore, focusing on the input range from origin to $V_{ref}/2$ in Fig. 1(c), we obtain the transfer curve as shown in Fig. 2(a). It is observed that the transfer curve can be approximated by two linear regions. In Fig. 2(b), by connecting the end points of each segment, two straight lines \overline{ik} and \overline{ka} can be used to linearly approximate the original transfer curve.

From Fig. 2(b), to calibrate the error caused by nonlinearity, the distance between ideal curve and approximated line has to be compensated. In region (I), by simple math, the following equations can be obtained.

$$\begin{aligned} \frac{\overline{ef}}{\overline{df}} &= \frac{\overline{kl}}{\overline{jl}} \\ \frac{\overline{ef}}{\overline{de + ef}} &= \frac{\overline{kl}}{\overline{jl}} \\ \text{Let } \frac{\overline{kl}}{\overline{jl}} &= x, \Rightarrow \overline{de} = \frac{1-x}{x} \times \overline{ef}, \end{aligned} \quad (1)$$

where k has to be measured in advance based on input $l (= \frac{V_{ref}}{4})$, j represents $\frac{V_{ref}}{2}$, and f is the normal input value. Therefore, \overline{de} is the corresponding compensation for input f . Because triangle $\triangle ilj$ is identical to $\triangle kbn$, the same calibration techniques can be applied to region (II) except measurements of a and b have to be performed in advance. Because b and k are equivalent, one measurement can be done for b and k simultaneously. Furthermore, the compensation term needs to include $\overline{jk} (= \varepsilon)$ in addition to δ , where ε can be found as follows:

$$\varepsilon = \overline{jl} - \overline{kl}. \quad (2)$$

B. Offset considerations

In high-speed and medium resolution pipelined ADCs, their offset mainly arises from comparator offset and amplifier

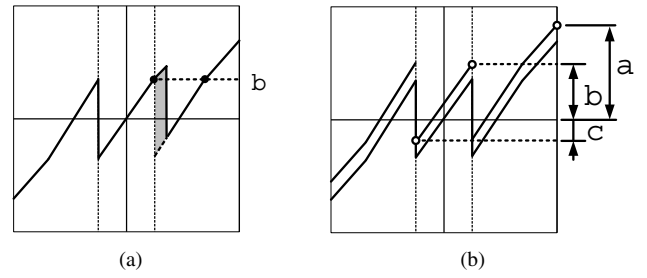


Fig. 3. (a) Comparator offset. (b) Amplifier offset.

offset. As shown in Fig. 3(a), if comparator offset causes the shift of the decision level, the output voltage above point b will enter the region (II) corresponding to Fig. 2(b). Therefore, the former offset does not affect this calibration algorithm. Since 1.5-b/stage pipelined ADCs can tolerate wider range of comparator offset, its output data will be corrected by the error correction logic. However, when the offset is arisen from the open-loop amplifier, the offset can affect the measured values for calibration. To overcome the error induced by amplifier offset, one more point c in Fig. 3(b) is measured. The offset value can be calculated by the following equation:

$$offset = (b - c)/2. \quad (3)$$

To avoid the information missing at the end point, the gain of the amplifier must be chosen smaller than 2 to tolerate more offset without losing calibration information [5].

III. DIGITAL BACKGROUND CALIBRATION

A. Digital calibration block

To linearly approximate the transfer curve to two segments, the parameters a and b in Fig. 4(a) must be known. The way to obtain parameters a , b , and c is to apply the reference voltages $V_{ref}/2$, $V_{ref}/4$, and $-V_{ref}/4$ respectively to the input and is measured by the following ADC stages. In Fig. 4(b), a' is $a - offset$ and b' is $b - offset$. When the converted digital code subtracts offset and compares with a' , b' , and $2h - 2b'$, the original input region is known. For example, if the converted digital code is greater than h and less than b' , the original input region is 3 in Fig. 4(b). Figure 4(c) shows the digital calibration block (*CAL*). D_{org} represents the converted digital code of following ADC stages before calibration. Because the representation of actual converted data is unsigned digital code, the offset h arising from code 0 to half of the full code region must be taken into consideration. The result of digital comparator circuit (*CMP*) indicates the D_{org} location as mentioned in Fig. 4(b). The value \overline{ef} corresponding to Fig. 2(b) is selected by the comparator result. Since the relation between \overline{kl} and $\frac{1-x}{x}$ is one-to-one mapping, to avoid division arithmetic, value $\frac{1-x}{x}$ is pre-computed in the look-up-table (*LUT*). Therefore, the compensation value is available from $\overline{kl} \times \frac{1-x}{x}$. If input code is located in region 1 and 4 of Fig. 4(b), the compensation value must be added with ε . Finally, the compensation value is added to D_{org} to derive the calibrated code D_{cal} .

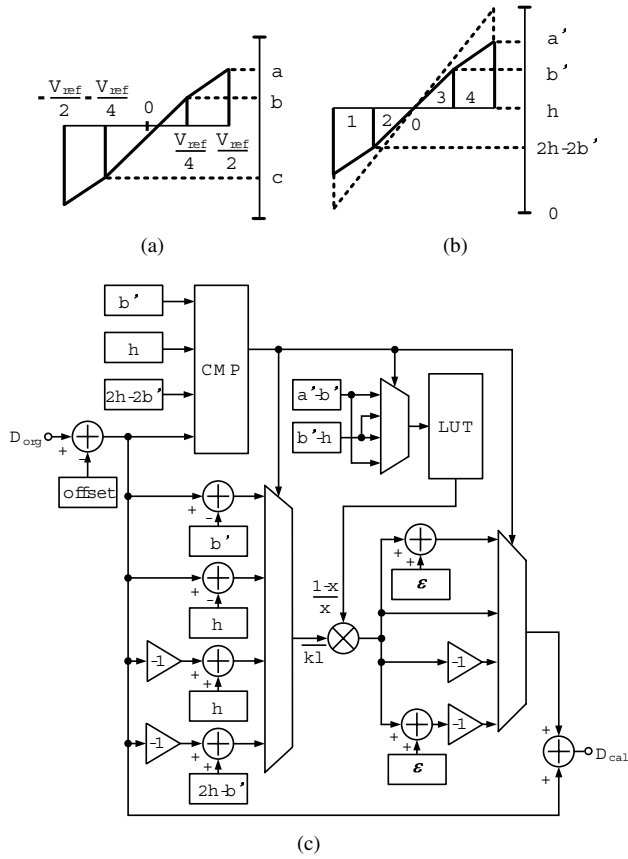


Fig. 4. (a) Parameters measurement. (b) Digital comparator locations. (c) Digital calibration block (CAL).

B. Background calibration

Conventional pipelined ADCs need two non-overlap clocks to operate in different phase. The amplifier is in amplifying action in the first phase and in reset state in the second phase. The amplifier is idle when it resets in the second phase. By double sampling technique [6], the normal conversion block converts generic input in the first phase and the additional part of block is obtained to measure parameters for calibration in the second phase. In open-loop amplifier application, parameters may vary with temperature or aging. It is necessary to continuously track these variations. Measuring parameters on the other phase of pipelined ADC forms a continuous-time background calibration without interrupting normal conversion. The detail connection of this pipelined stage is indicated in Fig. 5. The shaded part represents normal conversion block, and the middle dotted part represents calibration block. The dotted block in lower part represents the inputs of calibration voltage. When measuring the amplifier nonlinearity parameter a , b , and c , S_{c0} is *ON* and S_{20} , S_{22} are *OFF*. Reference voltage $V_{ref}/2$, $V_{ref}/4$, and $-V_{ref}/4$ are used to measure the raw parameter a , b , and c respectively.

IV. SIMULATION

Differential circuits exhibit an “odd-symmetric” input/output characteristic [7]. The Taylor expansion of the

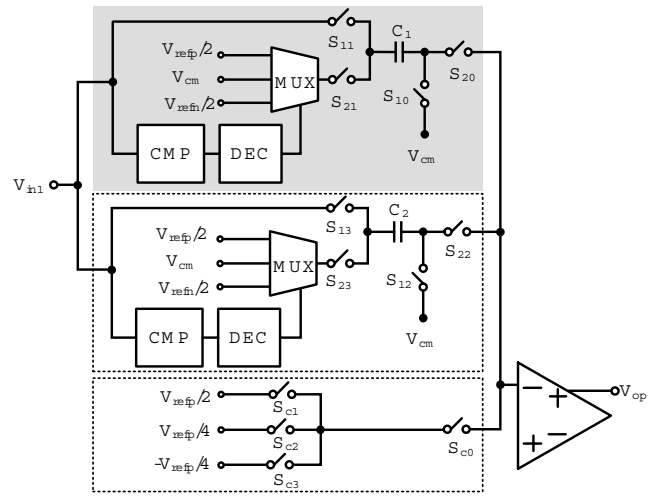


Fig. 5. Stage circuits.

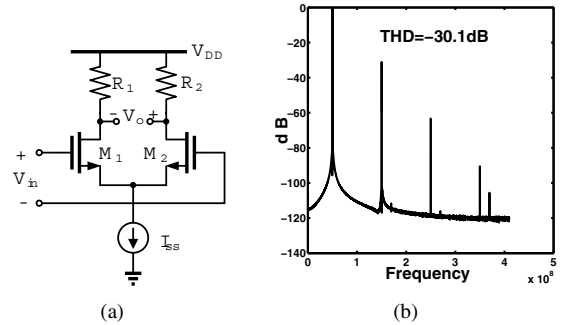


Fig. 6. (a) Simple open-loop amplifier. (a) Total harmonic distortion (THD).

characteristic in the range of interest can be expressed as :

$$y(t) = \alpha_1 x(t) + \alpha_3 x^3(t) + \alpha_5 x^5(t) + \dots \quad (4)$$

As shown in Fig. 6(a), this typical differential amplifier performs THD about -31.1 dB (Fig. 6(b)) under the circumstance of $0.5V_{pp}$ input swing, $I_{ss} = 1mA$, $V_{DD} = 1.8V$ and the maximum gain equals about 2. It is observed that the third harmonic dominates the performance of THD. The 5th harmonic is below -60 dB. Therefore, the behavioral simulations focus on the distortion caused by α_1 and α_3 , which dominate the nonlinearity of open-loop amplifiers.

The system architecture of pipelined ADC for simulation is shown in Fig. 7. This ADC is designed for 8-bit 500 MS/s conversion. Stage 1 to stage 8 are 1.5-b per stage, and end with a 2-b flash stage. In order to increase the accuracy of measurement, two extra bits are included. Shaded blocks represent the parameter measurement parts of the ADC. Data alignment blocks are not shown in the figure. Because the front stages of pipelined ADC dominate the performance of conversion result, only two stages at the beginning of the ADC are calibrated for simplicity. Stage 3 to Stage 9 are regarded as ideal pipelined stages. Since every 1.5-b per pipelined stage has one overlapped digit, the *CMB* blocks combine the converted data for the following applications.

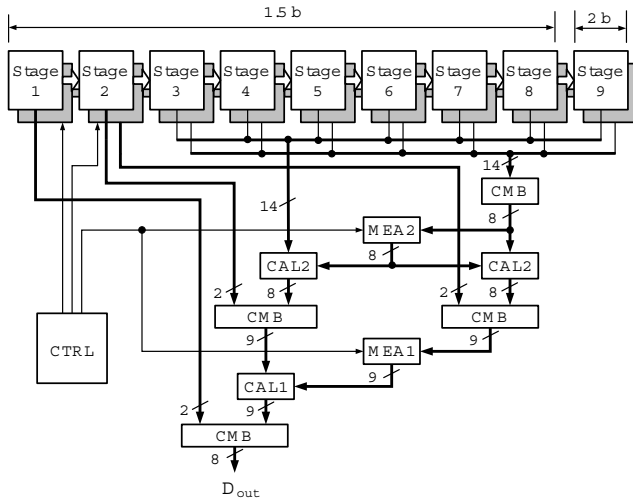


Fig. 7. System Architecture.

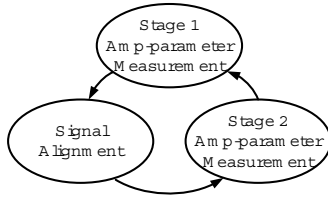


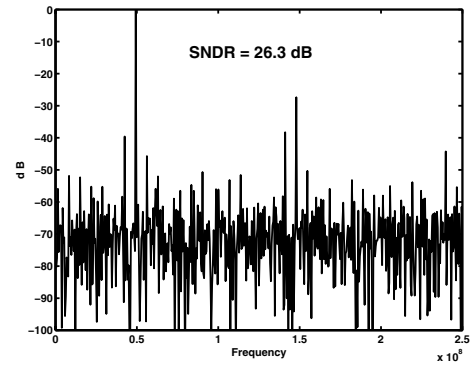
Fig. 8. Control state.

The control circuit (*CTRL*) controls the sequence of actions on switches S_{c0} , S_{10} , S_{20} of Fig. 5 and the calibration state. As shown in Fig. 8, stage 2 parameters are measured in *Stage 2 Amp – parameter Measurement* state at first. Then, stage 1 parameters are measured in *Stage 1 Amp – parameter Measurement* state. Since the latency between stage 1 and stage 2 is a half clock cycle, the action has to stay in *Signal Alignment* state before going back to *Stage 2 Amp – parameter Measurement* state. Once the parameters of stage 2 amplifier are measured, the value will stay in *MEA2* for using by two calibration circuits, *CAL2*. Then parameters of stage 1 amplifier are measured and these values stay in *MEA1* for using by calibration circuit *CAL1*. Normal conversion result will be calibrated by left *CAL2* and *CAL1* to get the output data D_{out} .

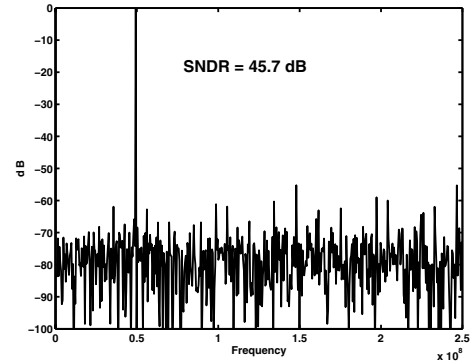
An 8-bit ADC illustrated in Fig. 7 has been simulated in MATLAB. When the input signal is 50 MHz ± 1 magnitude sinusoidal signal, amplifier offset error is 0.01, gain error is 0.15 and the coefficient of cubic term is -0.3 corresponding to THD -30 dB on the open-loop amplifier, the output spectrum without calibration is shown in Fig. 9(a). The signal-to-noise ratio (SNDR) is 26.3 dB. The output spectrum with calibration is shown in Fig. 9(b). The SNDR is improved to 45.6 dB.

V. CONCLUSION

This paper proposes a linear approximation technique to improve the linearity of open-loop amplifier in pipelined ADC. This technique compensates the gain error, offset, and



(a)



(b)

Fig. 9. Simulated SNDR: (a) without calibration, (b) with calibration.

nonlinearity of the analog circuit in digital domain. Digital calibration and double sampling techniques achieve background calibration without interrupting normal conversion. The calibration algorithm is illustrated by using an 8-b ADC in MATLAB simulation.

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